FT6116

2K X 8 CMOS SRAM

FORCE
TECHNOLOGIES LTD

Features

- **High-speed access and chip select times**
  - *Military: 120/150ns (max.)*

- **Low-power consumption**
- **Battery backup operation**
  - *2V data retention voltage (Low power version only)*
- **Produced with advanced CMOS high-performance technology**
- **CMOS process virtually eliminates alpha particle soft-error rates**
- **Input and output directly TTL-compatible**
- **Static operation: no clocks or refresh required**
- **Available in ceramic and plastic 24-pin DIP, 24-pin Thin Dip,**
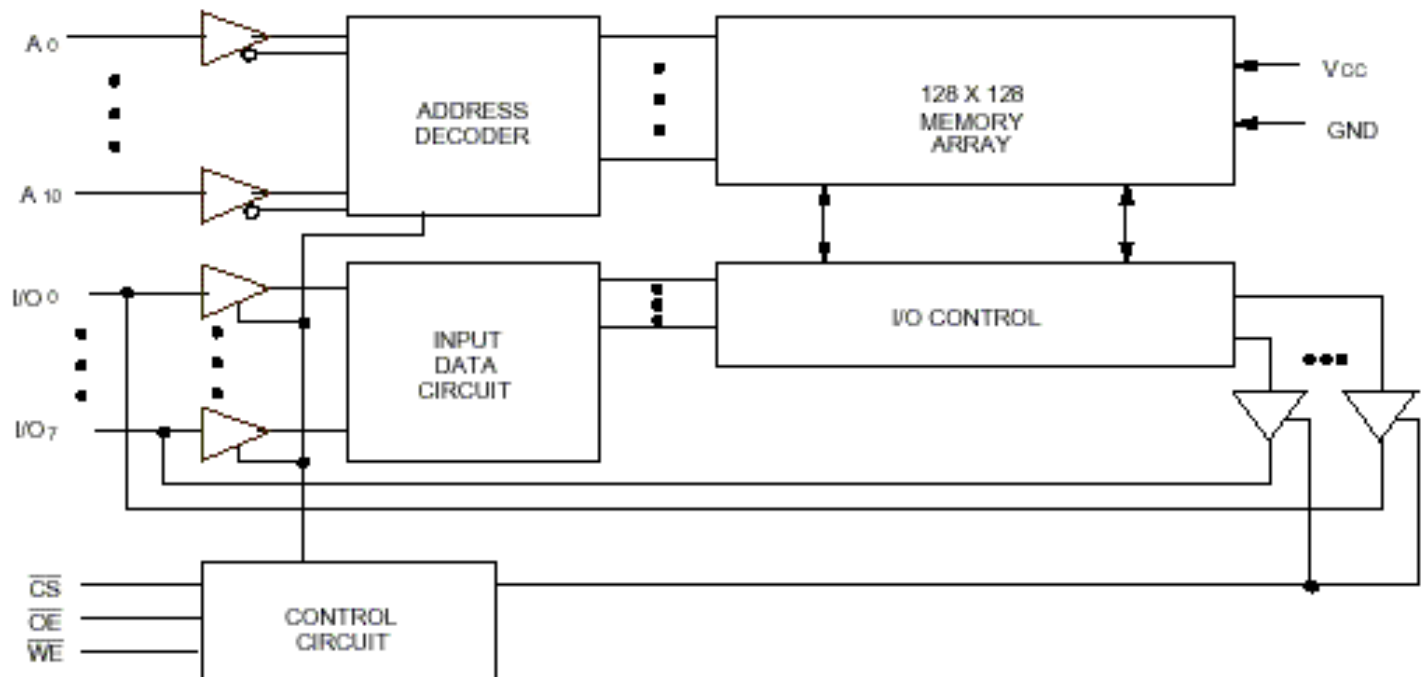
Description

The FT6116 is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using FT's high-performance, high-reliability CMOS technology.

Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as $\overline{CS}$ remains HIGH. This capability provides significant system level power and cooling savings. The low-power version also offers a battery backup data retention capability where the circuit typically consumes only 1μW to 4μW operating off a 2V battery.

All inputs and outputs of the FT6116 are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The FT6116 is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP
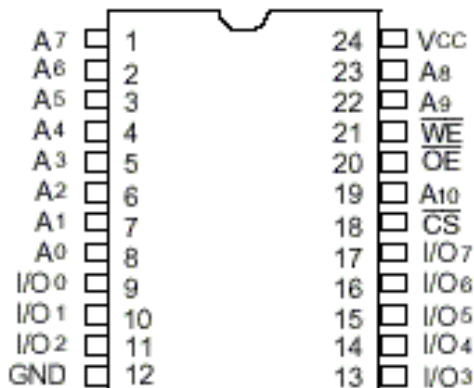
Functional Block Diagram

FT6116
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Pin Configurations

```
      A7  ▢ 1        24 ▢ VCC
      A6  ▢ 2        23 ▢ A8
      A5  ▢ 3        22 ▢ A9
      A4  ▢ 4        21 ▢ WE
      A3  ▢ 5        20 ▢ OE
      A2  ▢ 6        19 ▢ A10
      A1  ▢ 7        18 ▢ CS
      A0  ▢ 8        17 ▢ I/O7
     I/O0 ▢ 9        16 ▢ I/O6
     I/O1 ▢ 10       15 ▢ I/O5
     I/O2 ▢ 11       14 ▢ I/O4
     GND  ▢ 12       13 ▢ I/O3
```

DIP
Top View

Pin Description

Name	Description
A0 - A10	Address Inputs
I/O0 - I/O7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power
GND	Ground

Capacitance (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
CIO	I/O Capacitance	VOUT = 0V	8	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

Absolute Maximum Ratings[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC +0.5V.

Truth Table[1]

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High-Z
Read	L	L	H	DATAOUT
Read	L	H	H	High-Z
Write	L	X	L	DATAIN

NOTE:
1. H = VIH, L = VIL, X = Don't Care.

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Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Industrial	-45°C to +85°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5[2]	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	Vcc +0.5	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTES:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.
2. V_{IH} must not exceed Vcc +0.5V.

DC Electrical Characteristics
(Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions				FT6116 Min.	FT6116 Max.	Unit
$|I_{LI}|$	Input Leakage Current	Vcc = Max., V_{IN} = GND to Vcc	MIL. COM'L.			— —	5 2	µA
$|I_{LO}|$	Output Leakage Current	Vcc = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to Vcc	MIL. COM'L.			— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, Vcc = Min.					0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, Vcc = Min.				4		V

DC Electrical Characteristics[1] (continued)
(Vcc = 5.0V ± 10%, VLC = 0.2V, VHC = Vcc - 0.2V)

Symbol	Parameter	Power						FT6116 120	FT6116 150	Unit
								Mil Only	Mil Only	
ICC1	Operating Power Supply Current, $\overline{CS} \leq V_{IL}$, Outputs Open Vcc = Max., f = 0							90	90	mA
ICC2	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open Vcc = Max., f = fMAX[2]							100	90	mA
ISB	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open Vcc = Max., f = fMAX[2]							25	25	mA
ISB1	Full Standby Power Supply Current (CMOS Level), $\overline{CS} \geq V_{HC}$, Vcc = Max., VIN $\leq$ VLC or VIN $\geq$ VHC, f = 0							10	10	mA

NOTES:
1. All values are maximum guaranteed values.
2. fMAX = 1/tRC, only address inputs are toggling at fMAX, f = 0 means address inputs are not changing.

Data Retention Characteristics Over All Temperature Ranges
(LA Version Only) (VLC = 0.2V, VHC = Vcc – 0.2V)

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @		Max. Vcc @		Unit
					2.0V	3.0V	2.0V	3.0V	
VDR	Vcc for Data Retention	—		2.0	—	—	—	—	V
ICCDR	Data Retention Current	MIL. COM'L.		— —	0.5 0.5	1.5 1.5	200 20	300 30	μA
tCDR[3]	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ VIN $\geq$ VHC or $\leq$ VLC		—	0	—	—	—	ns
tR[3]	Operation Recovery Time			tRC[2]	—	—	—	—	ns
|ILI|	Input Leakage Current			—	—	—	2	2	μA

NOTES:
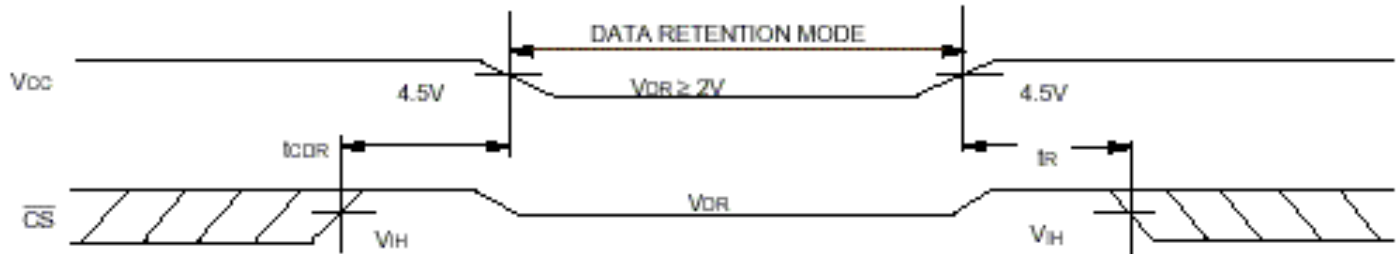1. TA = + 25°C
2. tRC = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

Low Vcc Data Retention Waveform

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

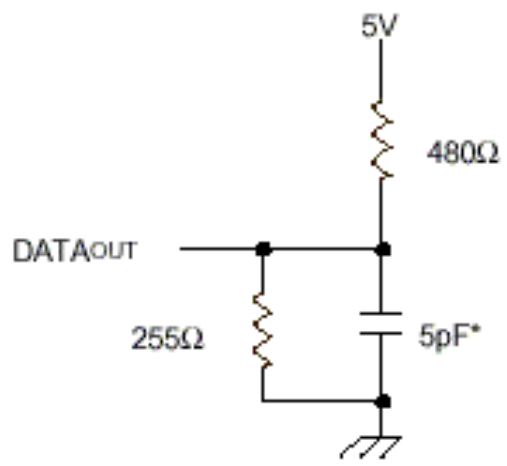
Figure 1. AC Test Load

3089 drw 04

Figure 2. AC Test Load
(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{BHZ}, t_{CHZ} & t_{OW})

*Including scope and jig.

AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges) (continued)

Symbol	Parameter									FT6116 120[2]		FT6116 150[2]		Unit
										Min.	Max.	Min.	Max.	
Read Cycle														
tRC	Read Cycle Time									120	—	150	—	ns
tAA	Address Access Time									—	120	—	150	ns
tACS	Chip Select Access Time									—	120	—	150	ns
tCLZ[3]	Chip Select to Output in Low-Z									5	—	5	—	ns
tOE	Output Enable to Output Valid									—	80	—	100	ns
tOLZ[3]	Output Enable to Output in Low-Z									5	—	5	—	ns
tCHZ[3]	Chip Deselect to Output in High-Z									—	40	—	40	ns
tOHZ[3]	Output Disable to Output in High Z									—	40	—	40	ns
tOH	Output Hold from Address Change									5	—	5	—	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
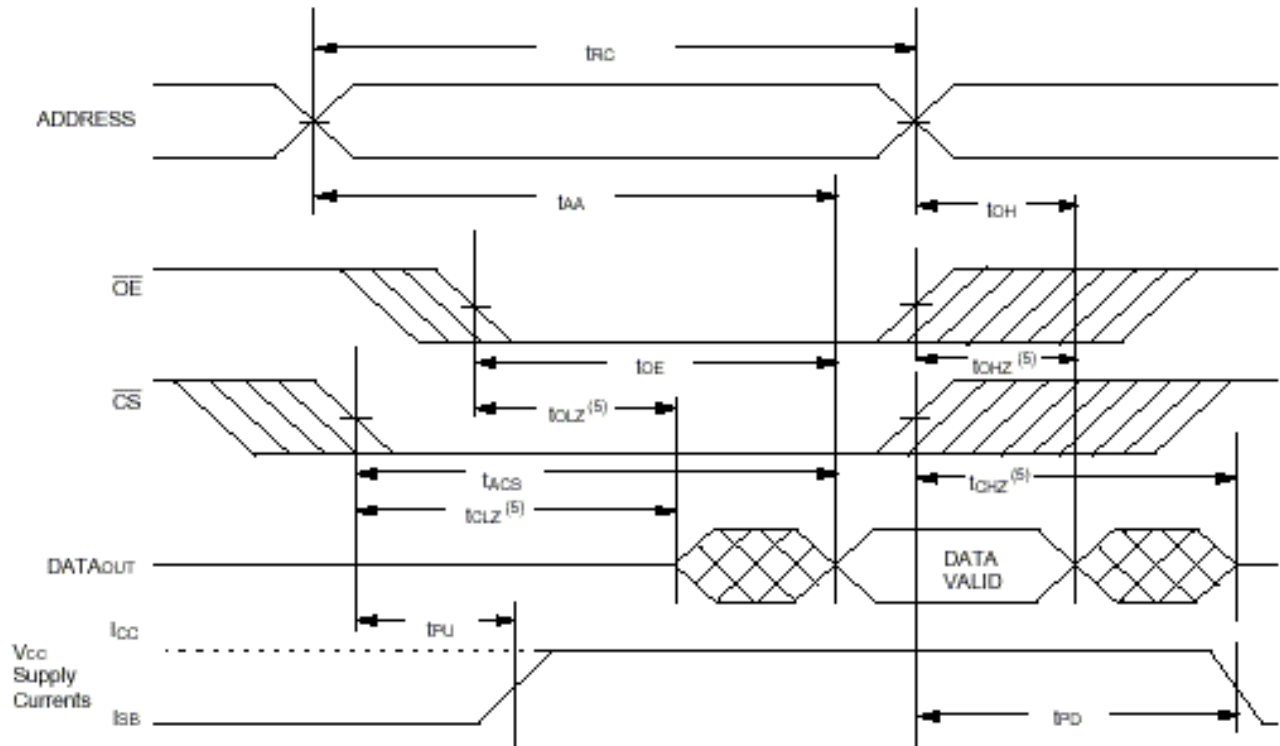3. This parameter guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
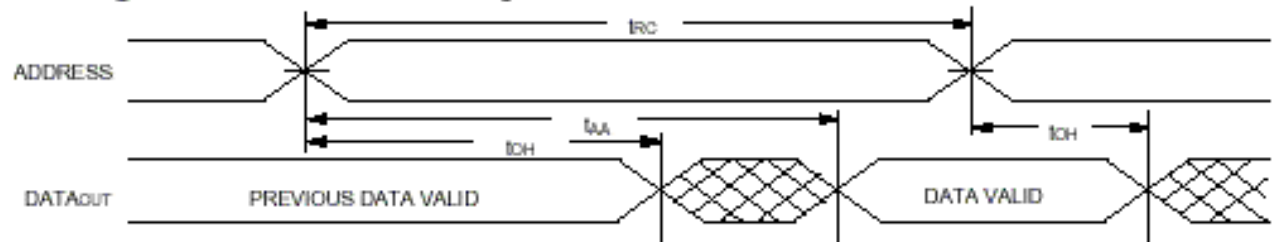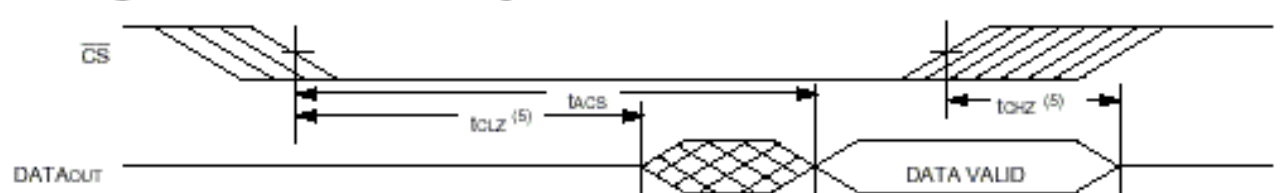
Timing Waveform of Read Cycle No. 1[1,3]

Timing Waveform of Read Cycle No. 2[1,2,4]

Timing Waveform of Read Cycle No. 3[1,3,4]

NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±500mV from steady state.

AC Electrical Characteristics (Vcc = 5V ± 10%, All Temperature Ranges)

Symbol	Parameter								FT6116 120[2] Min.	FT6116 120[2] Max.	FT6116 150[2] Min.	FT6116 150[2] Max.	Unit
Write Cycle													
twc	Write Cycle Time								120	—	150	—	ns
tcw	Chip Select to End-of-Write								70	—	90	—	ns
taw	Address Valid to End-of-Write								105	—	120	—	ns
tas	Address Setup Time								20	—	20	—	ns
twp	Write Pulse Width								70	—	90	—	ns
twr	Write Recovery Time								5	—	10	—	ns
twhz[3]	Write to Output in High-Z								—	40	—	40	ns
tdw	Data to Write Time Overlap								35	—	40	—	ns
tdh[3]	Data Hold from Write Time								5	—	10	—	ns
tow[3,4]	Output Active from End-of-Write								0	—	0	—	ns

NOTES:

1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. This parameter guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.
4. The specification for tdw must be met by the device supplying write data to the RAM under all operation conditions. Although tdh and tow values will vary over voltage and temperature, the actual tdh will always be smaller than the actual tow.
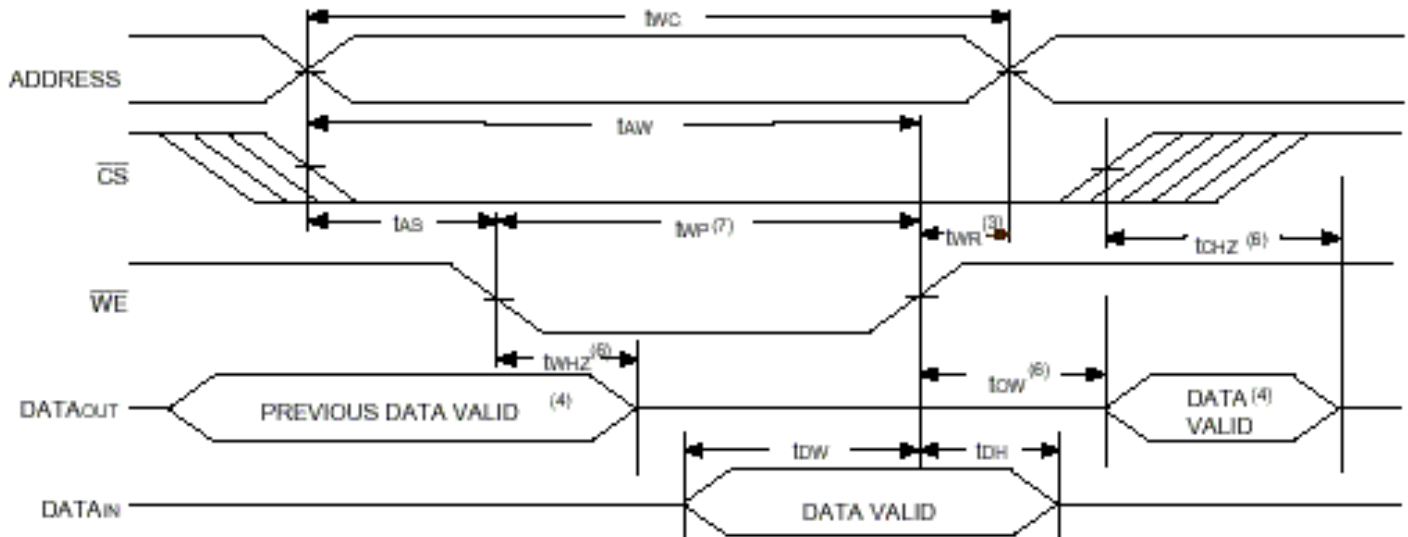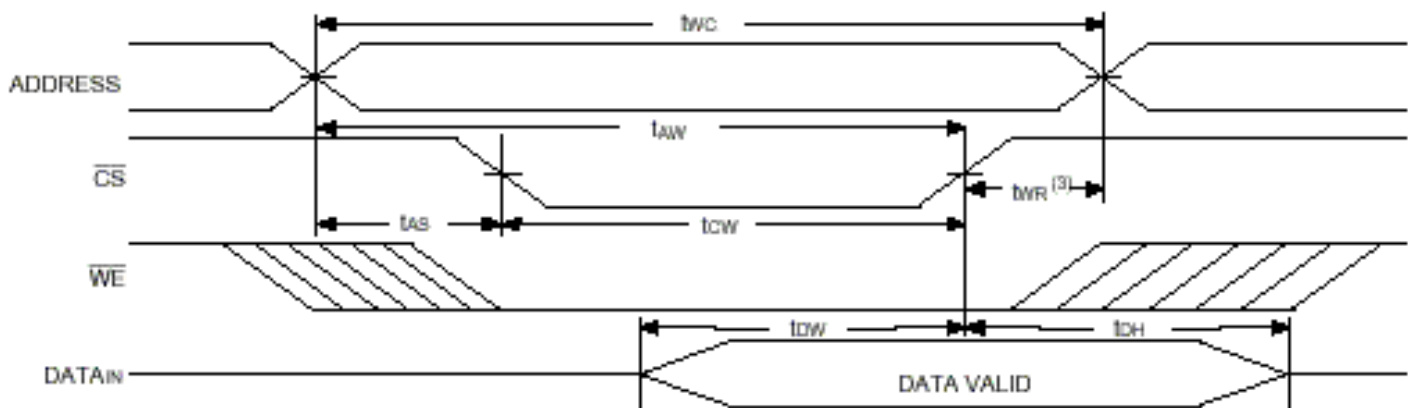
Timing Waveform of Write Cycle No. 1 (WE Controlled Timing)[1,2,5,7]

Timing Waveform of Write Cycle No. 2 (CS Controlled Timing)[1,2,3,5,7]

NOTES:

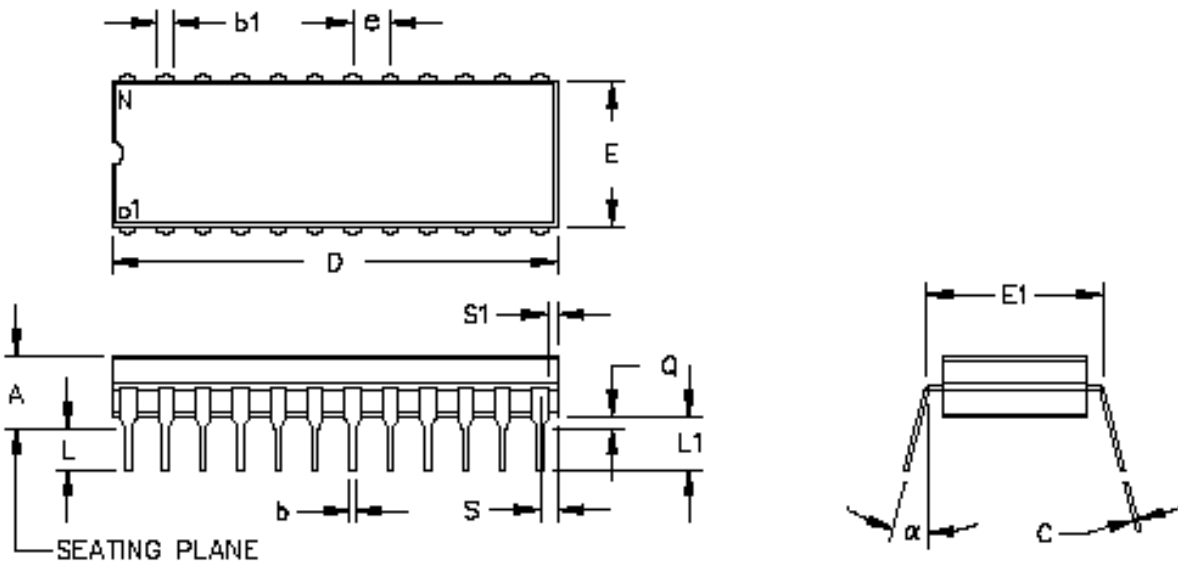1. WE or CS must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW CS and a LOW WE.
3. t_{WR} is measured from the earlier of CS or WE going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and the input signals must not be applied.
5. If the CS LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±500mV from steady state.
7. OE is continuously HIGH. If OE is LOW during a WE controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{OW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW}. If OE is HIGH during a WE controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP}. For a CS controlled write cycle, OE may be LOW with no degradation to t_{CW}.

REV	DCN	DESCRIPTION	DATE	APPROVED
06	17517	UPDATED TO STANDARDIZE DWG		

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC — BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	D24—1	
SYMBOL	MIN	MAX
A	.140	.200
b	.015	.021
b1	.045	.065
C	.009	.014
D	1.240	1.280
E	.285	.310
E1	.300	.320
e	.100 BSC	
L	.125	.175
L1	.150	—
Q	.015	.060
S	.030	.080
S1	.005	—
α	0°	15°
N	24	

CONFIGURATION	EXCEPTIONS
D—9	NONE
MO—058—AA	NONE

MIL—M—38510
JEDEC

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC DEC ANGLES
± –   ± –   ± –

APPROVALS | DATE
DRAWN
CHECKED

24 LD CERDIP MKT DWG
(300 MIL)

SCALE	SIZE	DRAWING NO.	REV
N/A	A		06

DO NOT SCALE DRAWING   SHEET 2 OF 2

FT6116
2K X 8 CMOS SRAM

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REV	DCN	DESCRIPTION	DATE	APPROVED
06	17514	UPDATED TO STANDARDIZE DWG		
07	22234	CHANGED b1 MIN DIM		

NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC — BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	D24-2	
SYMBOL	MIN	MAX
A	.090	.190
b	.014	.023
b1	.045	.060
C	.008	.012
D	1.230	1.290
E	.500	.610
E1	.590	.620
e	.100 BSC	
L	.125	.200
L1	.150	—
Q	.015	.060
S	.030	.080
S1	.005	—
α	0°	15°
N	24	

CONFIGURATION	EXCEPTIONS
D-3	NONE
NOT REGISTERED	

MIL-M-38510
JEDEC

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC DEC ANGLES
± — ± — ± —

APPROVALS	DATE
DRAWN	
CHECKED	

24 LD CERDIP MKT DWG (600 MIL)

SCALE	SIZE	DRAWING NO.	REV
N/A	A		07

DO NOT SCALE DRAWING   SHEET 2 OF 2