TEXAS INSTRUMENTS

THS8083

Triple 8-Bit, 80/95 MSPS, 3.3-V Video and Graphics Digitizer With Digital PLL

Data Manual

June 2000

AAP Data Conversion

SLVS233B

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Contents

List of Illustrations

List of Tables

1 Introduction

The THS8083 is a solution for digitizing video and graphic signals in RGB or YUV/YCbCr color spaces. The device supports pixel rates up to 80 MHz or 95 MHz, depending on the speed-grade of the device (THS8083 vs THS8083-95). Therefore, it can be used for PC graphics digitizing up to the VESA standard of XGA (1024 X 768) resolution at 75 Hz respectively, 85-Hz screen refresh rate, and in video environments for the digitizing of digital TV formats, including HDTV.

The THS8083 is powered from a single 3.3-V supply and integrates a triple high-performance A/D converter with clamping functions and variable gain, independently programmable for each channel. Separate clamping ranges are provided for RGB and YUV operation modes of the device. The clamp timing window is provided by an external pulse or can be generated internally.

The programmable gain amplifiers consist of coarse and fine gain control blocks. The THS8083 includes slicing circuitry on the Y or G input to support sync-on-green or sync-on-luminance extraction. The THS8083 further contains a completely digital PLL block, consisting of phase-frequency detector (PFD), discrete time oscillator (DTO) and programmable divider to generate the (sampling) clock from the incoming horizontal sync (HS) signal, depending on the incoming video resolution. Any pixel rate can be generated in the 10-80/95 MHz range. Moreover, the output phase of the synthesized clock can be controlled with sub-pixel accuracy (31 uniform settings).

Programmable time constants allow the PLL loop bandwidth to be changed by the integrated PLL loop filter. Alternatively, the user may bypass the PLL when an external pixel clock is available. Even then the DTO synthesized clock is still available externally and can therefore be used in other parts of the (graphics) system. Extensive PLL and input monitoring functions are integrated for typical functionality required in LCD/DMD monitor/projection systems (input format detection, autocalibration).

All programming of the part is done via an industry-standard normal/fast I^2C interface, which supports both reading and writing of register settings. The THS8083 is available in a space-saving TQFP 100-pin PowerPAD™ package.

NOTE: THS8083-95 available from 4Q 2000.

1.1 Features

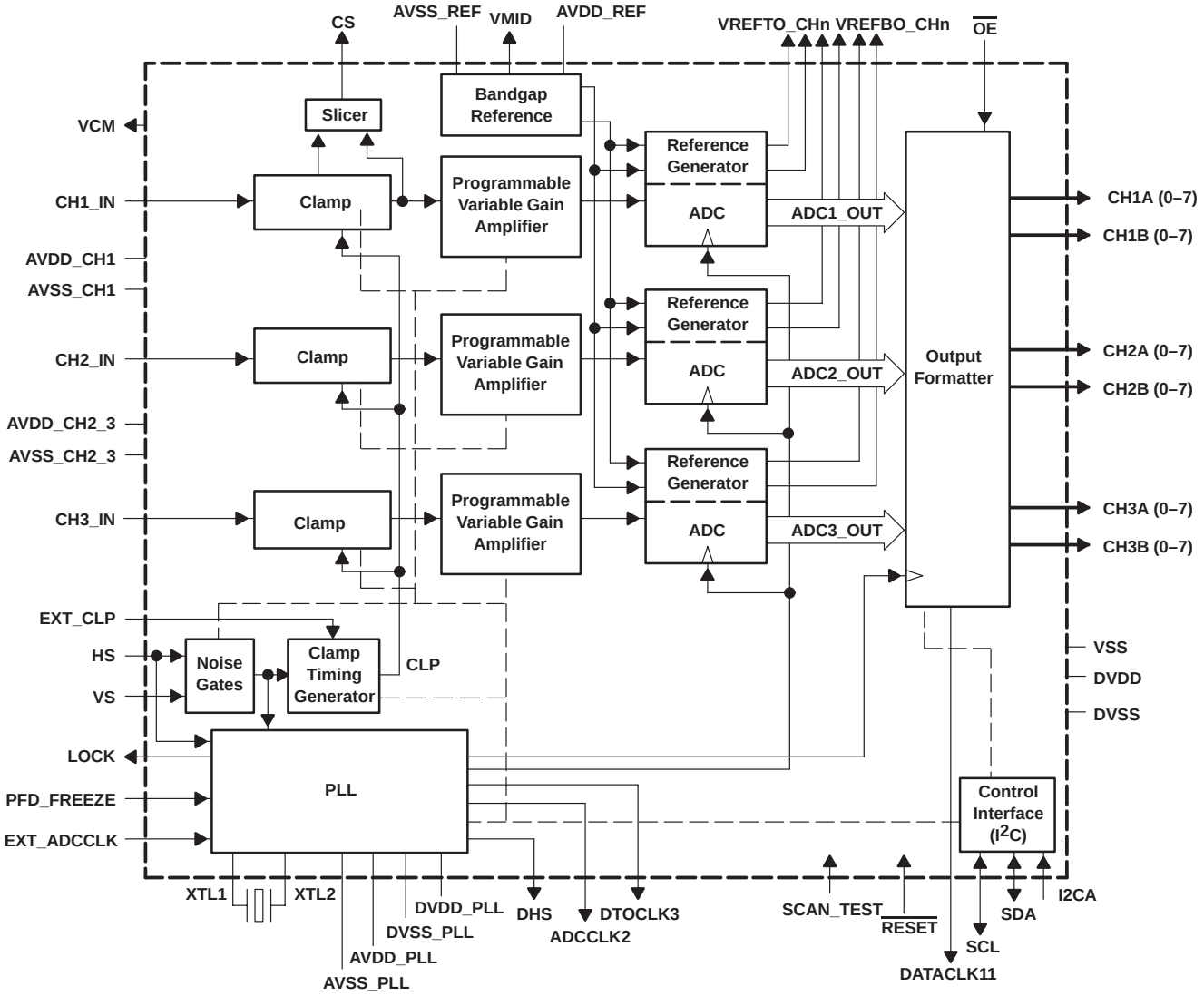
The THS8083 supports the following features:

- Analog Channels – Three digitizing channels, each with independently controllable clamp, PGA, and ADC.
  - Clamp: 256-step programmable RGB or YUV clamping during external or internal clamp timing window
  - PGA: 6-bit coarse/5-bit fine programmable gain amplifier
  - ADC: 8 bit 80 MSPS (THS8083) or 95 MSPS (THS8083-95) A/D converter
  - Composite Sync: Integrated sync-on-green/sync-on-luminance extraction
  - Support for ac-coupled input signals
- PLL
  - Fully integrated digital PLL (including loop filter) for pixel clock generation
  - 10-80 MHz (THS8083) or 10-95 MHz (THS8083-95) pixel clock generation from reference input
  - Adjustable PLL loop bandwidth for minimum jitter or fast acquisition/wide capture range modes
  - 5-bit programmable subpixel accuracy positioning of sampling phase
  - Noise gates on HS input to avoid false PLL updating

PowerPAD is a trademark of Texas Instruments.

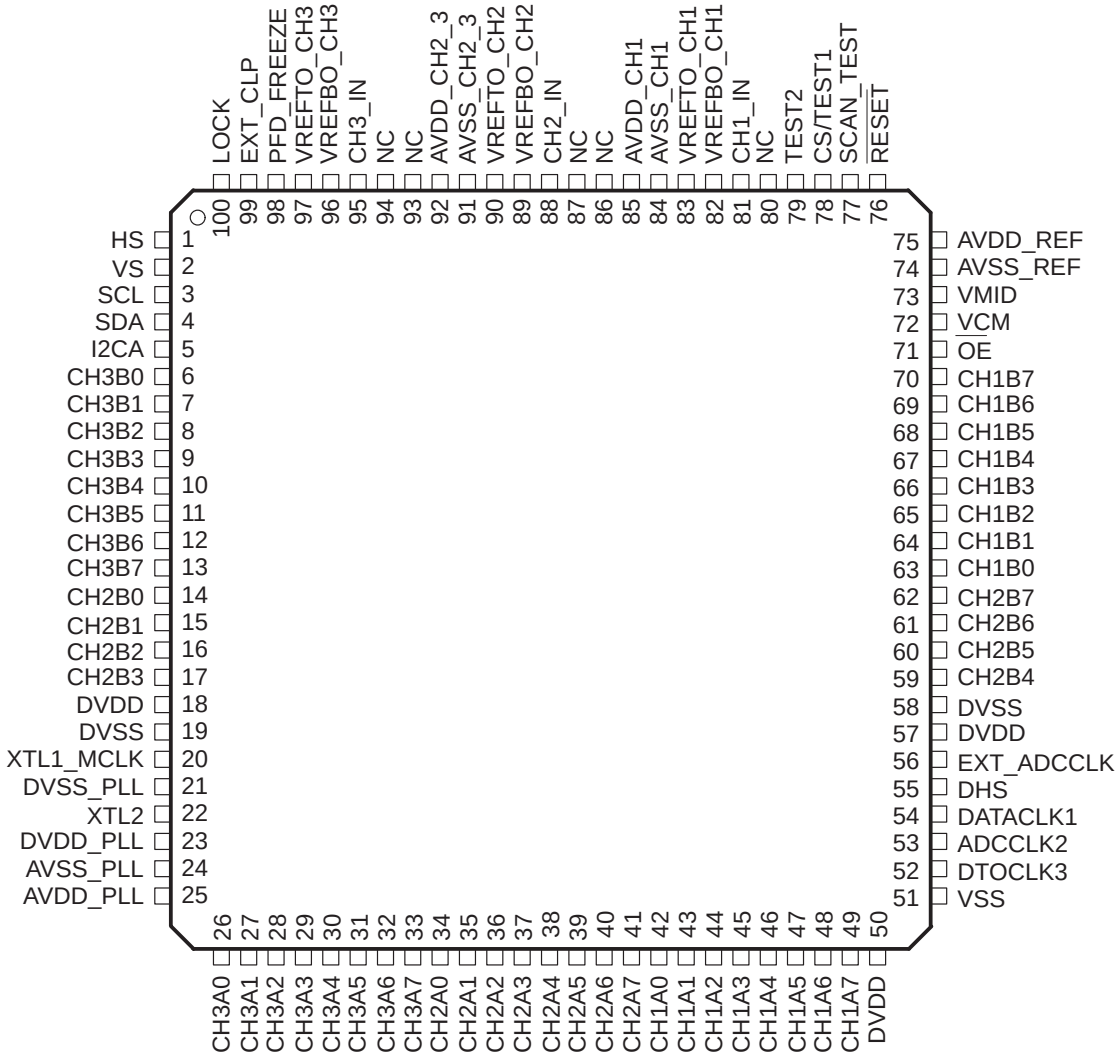
- Output Formatter
  - Single and double pixel width output data bus for reduced board clock frequency and EMI
  - Support for 4:4:4 and 4:2:2 (ITU.BT–601 style) output modes to reduce board traces to video ASICs
  - Dedicated DATACLK1 output for easy latching of output data
- System
  - Industry-standard normal/fast I^2C interface with register readback capability
  - Support for input format detection via integrated monitoring of HS, VS, and pixel clock frequencies
  - Support for multidevice operation (master/slave operation for SXGA resolution)
  - Space-saving TQFP-100 pin package
  - Thermally-enhanced PowerPAD™ package for better heat dissipation
- Applications
  - LCD desktop monitors and LCD or DMD-based projection systems
  - Videoconferencing
  - PCTV set-top boxes, digital TV sets, and multimedia cards
  - Scan rate/image resolution converters
  - Video/graphics digitizing equipment (RGB or YUV-based)

1.2 Functional Block Diagram



1.3 Terminal Assignments

TQFP PowerPAD™ PACKAGE
(TOP VIEW)



1.4 Ordering Information

T_A	PACKAGED DEVICES	
	TQFP–100	
Maximum clock frequency	80 MSPS	95 MSPS†
0°C to 70°C	THS8083CPZP	THS8083-95CPZP

† 95 MSPS speedgrade to be released. Limited samples available.

1.5 Abbreviations Used in This Document

PGA	Programmable gain amplifier
PLL	Phase-locked loop
I^2C	Inter-IC interface
EMI	Electro-magnetic interference
NTSC	National Television Systems Committee
PAL	Phase alternating line
DTV	Digital TV
VBI	Vertical blanking interval
CS	Composite sync

1.6 Conventions

Throughout this document, the term YUV refers to a video/graphics signal, consisting of three components, of which one component (Y) has its blanking level corresponding to the bottom level of the video signal range. The other two components (U&V) have their blanking level at the mid-scale of the video signal range (since U&V are color difference signals and thus, can go positive or negative with respect to blanking).

YUV, therefore should not be restricted to NTSC/PAL component formats, but also includes baseband component video formats used in DTV that should in a strict sense be denoted as analog YCbCr or YPbPr.

The term RGB refers to a video/graphics signal, consisting of three components, of which all components have their blanking level corresponding to the bottom level of the video signal range. Therefore, it relates to both RGB PC formats as well as red-green-blue video component signals, sometimes denoted as GBR instead of RGB in video broadcast environments.

1.7 THS8083 Terminal Functions Order

TERMINAL		I/O/B†	TYPE‡	DESCRIPTION
NAME	NO.			
POWER SUPPLIES				
AVSS_PLL	24	I	A	Analog ground for PLL (XTL oscillator and analog PLL)
AVDD_PLL	25	I	A	Analog supply (3.3 V) for analog PLL
DVSS_PLL	21	I	A	Digital ground for digital PLL
DVDD_PLL	23	I	A	Digital supply (3.3 V) for digital PLL
AVSS_CH1	84	I	A	Analog ground for A/D channel 1
AVDD_CH1	85	I	A	Analog supply (3.3 V) for A/D channel 1
AVSS_CH2_3	91	I	A	Analog ground for A/D channel 2 and channel 3
AVDD_CH2_3	92	I	A	Analog supply (3.3 V) for A/D channel 2 and channel 3
DVDD	18, 50, 57	I	A	Digital supply for all logic, except digital PLL
DVSS	19, 58	I	A	Digital ground for all logic, except digital PLL
VSS	51	I	A	Substrate ground
AVDD_REF	75	I	A	Analog supply (3.3 V) for voltage and current reference generator
AVSS_REF	74	I	A	Analog ground (3.3 V) for voltage and current reference generator

† I = input to device: O = output from device B = bidirectional
‡ A = analog pin: D = digital pin

1.7 THS8083 Terminal Functions Order (Continued)

TERMINAL NAME	TERMINAL NO.	I/O/B†	TYPE‡	DESCRIPTION
CLOCK I/O				
XTL1_MCLK	20	I	A	Master crystal connection 1 (connects 14.318-MHz crystal) or master clock input (at 14.318 MHz)
XTL2	22	O	A	Master crystal connection 2 (connects 14.318-MHz crystal)
DATACLK11	54	O	D	1st clock output: DATACLK1 This is a clock of which the rising edge can be used by an external device to clock in THS8083 output data in all modes (see output timing diagrams in Section 4 for more details).
ADCCLK2	53	O	D	2nd clock output: ADCCLK This clock output is equal to the clock of the ADC converter, optionally inverted and/or divided-by-2.
DTOCLK3	52	O	D	3rd clock output: DTOCLK. This clock output is the output of the DTO
EXT_ADCCLK	56	I	D	External clock input for A/D channels, at pixel clock frequency
ANALOG SIGNAL I/O				
CH1_IN	81	I	A	Analog input channel 1. Since this channel includes the composite sync slicer and is not downsampled in 4:2:2 mode, this channel should be used for green or luminance input, if any of these features are used.
CH2_IN	88	I	A	Analog input channel 2. In YUV 4:2:2 sampling mode, Pb should be connected to this input to generate a ITU.BT-601 style output.
CH3_IN	95	I	A	Analog input channel 3. In YUV 4:2:2 sampling mode, Pr should be connected to this input to generate a ITU.BT-601 style output.
VREFBO_CH1	82	B	A	Reference voltage bottom output channel 1. In normal operation: output. For a specific configuration, this terminal becomes an input terminal (see Powerdown section in Functional Description).
VREFTO_CH1	83	B	A	Reference voltage top output channel 1. In normal operation it is an output. For a specific configuration, this terminal becomes an input terminal (see Powerdown section in Functional Description).
VREFBO_CH2	89	B	A	Reference voltage bottom output channel 2. See VREFBO_CH1.
VREFTO_CH2	90	B	A	Reference voltage top output channel 2. See VREFTO_CH1.
VREFBO_CH3	96	B	A	Reference voltage bottom output channel 3. See VREFBO_CH1.
VREFTO_CH3	97	B	A	Reference voltage top output channel 3. See VREFTO_CH1.
VMID	73	B	A	Midlevel input range (input common mode). In normal operation it is an output. For a specific configuration, this terminal becomes an input terminal (see Powerdown section in Functional Description).
VCM	72	O	A	Common mode voltage output (approximately 1.5 V)
DIGITAL SIGNAL I/O				
CH1A0	42	O	D	Display output channel 1, bus A, bit 0 (LSB)
CH1A1	43	O	D	Display output channel 1, bus A, bit 1
CH1A2	44	O	D	Display output channel 1, bus A, bit 2
CH1A3	45	O	D	Display output channel 1, bus A, bit 3
CH1A4	46	O	D	Display output channel 1, bus A, bit 4
CH1A5	47	O	D	Display output channel 1, bus A, bit 5
CH1A6	48	O	D	Display output channel 1, bus A, bit 6
CH1A7	49	O	D	Display output channel 1, bus A, bit 7 (MSB)
CH1B0	63	O	D	Display output channel 1, bus B, bit 0 (LSB)
CH1B1	64	O	D	Display output channel 1, bus B, bit 1

† I = input to device: O = output from device B = bidirectional
‡ A = analog pin: D = digital pin

1.7 THS8083 Terminal Functions Order (Continued)

TERMINAL NAME	TERMINAL NO.	I/O/B†	TYPE‡	DESCRIPTION
DIGITAL SIGNAL I/O (Continued)				
CH1B2	65	O	D	Display output channel 1, bus B, bit 2
CH1B3	66	O	D	Display output channel 1, bus B, bit 3
CH1B4	67	O	D	Display output channel 1, bus B, bit 4
CH1B5	68	O	D	Display output channel 1, bus B, bit 5
CH1B6	69	O	D	Display output channel 1, bus B, bit 6
CH1B7	70	O	D	Display output channel 1, bus B, bit 7 (MSB)
CH2A0	34	O	D	Display output channel 2, bus A, bit 0 (LSB)
CH2A1	35	O	D	Display output channel 2, bus A, bit 1
CH2A2	36	O	D	Display output channel 2, bus A, bit 2
CH2A3	37	O	D	Display output channel 2, bus A, bit 3
CH2A4	38	O	D	Display output channel 2, bus A, bit 4
CH2A5	39	O	D	Display output channel 2, bus A, bit 5
CH2A6	40	O	D	Display output channel 2, bus A, bit 6
CH2A7	41	O	D	Display output channel 2, bus A, bit 7 (MSB)
CH2B0	14	O	D	Display output channel 2, bus B, bit 0 (LSB)
CH2B1	15	O	D	Display output channel 2, bus B, bit 1
CH2B2	16	O	D	Display output channel 2, bus B, bit 2
CH2B3	17	O	D	Display output channel 2, bus B, bit 3
CH2B4	59	O	D	Display output channel 2, bus B, bit 4
CH2B5	60	O	D	Display output channel 2, bus B, bit 5
CH2B6	61	O	D	Display output channel 2, bus B, bit 6
CH2B7	62	O	D	Display output channel 2, bus B, bit 7 (MSB)
CH3A0	26	O	D	Display output channel 3, bus A, bit 0 (LSB)
CH3A1	27	O	D	Display output channel 3, bus A, bit 1
CH3A2	28	O	D	Display output channel 3, bus A, bit 2
CH3A3	29	O	D	Display output channel 3, bus A, bit 3
CH3A4	30	O	D	Display output channel 3, bus A, bit 4
CH3A5	31	O	D	Display output channel 3, bus A, bit 5
CH3A6	32	O	D	Display output channel 3, bus A, bit 6
CH3A7	33	O	D	Display output channel 3, bus A, bit 7 (MSB)
CH3B0	6	O	D	Display output channel 3, bus B, bit 0 (LSB)
CH3B1	7	O	D	Display output channel 3, bus B, bit 1
CH3B2	8	O	D	Display output channel 3, bus B, bit 2
CH3B3	9	O	D	Display output channel 3, bus B, bit 3
CH3B4	10	O	D	Display output channel 3, bus B, bit 4
CH3B5	11	O	D	Display output channel 3, bus B, bit 5
CH3B6	12	O	D	Display output channel 3, bus B, bit 6
CH3B7	13	O	D	Display output channel 3, bus B, bit 7 (MSB)

† I = input to device: O = output from device B = bidirectional
‡ A = analog pin: D = digital pin

1.7 THS8083 Terminal Functions Order (Continued)

TERMINAL		I/O/B†	TYPE‡	DESCRIPTION
NAME	NO.			
DIGITAL CONTROL I/O				
SCL	3	B	D	Clock for I^2C. Although the device is an I^2C slave, this signal can be held low by the device to signal contention, therefore it is flagged bidirectional.
SDA	4	B	D	Serial data for I^2C
I2CA	5	I	D	Address select for I^2C 0 = LSB of device address 0 1 = LSB of device address 1
EXT_CLP	99	I	D	External clamp timing pulse. Positive polarity required.
HS	1	I	D	Reference clock input for PLL (horizontal sync input). Polarity selectable via I^2C register <HS_POL>. 5 V tolerant input
VS	2	I	D	Vertical sync input. Polarity selectable via I^2C register <VS_POL>. 5 V tolerant input
DHS	55	O	D	Display horizontal sync. This output can be generated as either a delayed version of input HS or as output pulse from the PLL feedback divider. See Display Horizontal Sync section in Functional Description.
CS/TEST1	78	O	A/D	Composite sync output. This output will produce a 3-V logic-compatible sliced output of CH1. When present and enabled, CS will carry the composite sync embedded in Ch1. See Composite Sync Slicer section in Functional Description. For TI internal testing, this pin can also be configured as a test pin. Leave unconnected when CS output signal is not used.
LOCK	100	O	D	Lock detect output 0 = unlocked 1 = locked
PFD_FREEZE	98	I	D	Freezes the PLL output frequency by stopping the PFD output (i.e., keeping last increment to DTO). See section 2.3 *Composite Sync Slicer*. 0 = updating 1 = frozen
$\overline{OE}$	71	I	D	Output enable for data output busses A and B. Data outputs are active only when $\overline{OE}$ = L and the corresponding bus is active for the current output formatter mode (register OFM_CTRL). When data outputs are not active or when DVDD = 0 V, data output is Hi-Z. The clock outputs are not affected by $\overline{OE}$. 0 = enabled 1 = disabled
$\overline{RESET}$	76	I	D	General chip reset (active low). The reset is a synchronous reset. Therefore, a master clock on XTL1–MCLK needs to be present for proper reset.
TEST I/O				
CS/TEST1	78	O	A/D	See description for this terminal under DIGITAL CONTROL I/O higher.
TEST2	79	O	A/D	Test mode analog output 2. Leave unconnected for normal use.
SCAN_TEST	77	I	D	Input for scan-path activation: 0 = disabled 1 = enabled. This pin MUST be tied low for normal operation and is of use for TI internal testing only.
UNUSED PINS				
NC	80, 86, 87, 93, 94	I	A	Not connected. Tie to a fixed high or low level on board.

† I = input to device: O = output from device B = bidirectional
‡ A = analog pin: D = digital pin

2 Functional Description

2.1 Analog Channel

The THS8083 contains three identical analog channels that are independently programmable. Each channel consists of a clamping circuit, a programmable gain amplifier, and an A/D converter.

2.2 Clamping Circuit

The purpose of clamping is to provide the input signal with a known dc-value. Typically, video signals will be ac-coupled into the part. The signal needs to be level-shifted to fall in the reference voltage range (VREFB...VREFT) of the A/D converter. By supplying a programmable clamp, the user can shift the input signal with respect to the A/D range. This has the same effect as keeping the input signal constant and applying offset to both A/D reference voltages while keeping the VREFT–VREFB difference equal. However, no external adjustments are needed with this implementation.

For video, the clamping circuit can only be active during the non-active video portion of each line to avoid changes in brightness along the line. Clamping is done during the horizontal blanking interval, either on the backporch of sync or during the sync tip (in the case of a sync present on at least one of the video channels). If HS is carried on a separate line, as is typically the case for PC graphics, clamping is done during blanking. When the Y or G input channel contains an embedded sync, then alternatively clamping can be done during the sync-tip. This is not supported on the THS8083, since it is expected that the input signal level during clamping (of which position and width are determined by the clamp timing pulse, see later) corresponds to the blanking level. Since (for RGB type inputs) the blanking level will correspond to a low output code of the A/D, it makes sense to center the clamp range around an A/D output code of 0. The user can adjust this level up or down, symmetrically around 0. If the clamping is set such that the blanking level corresponds to a level below 0, the A/D output is clipped at code 0.

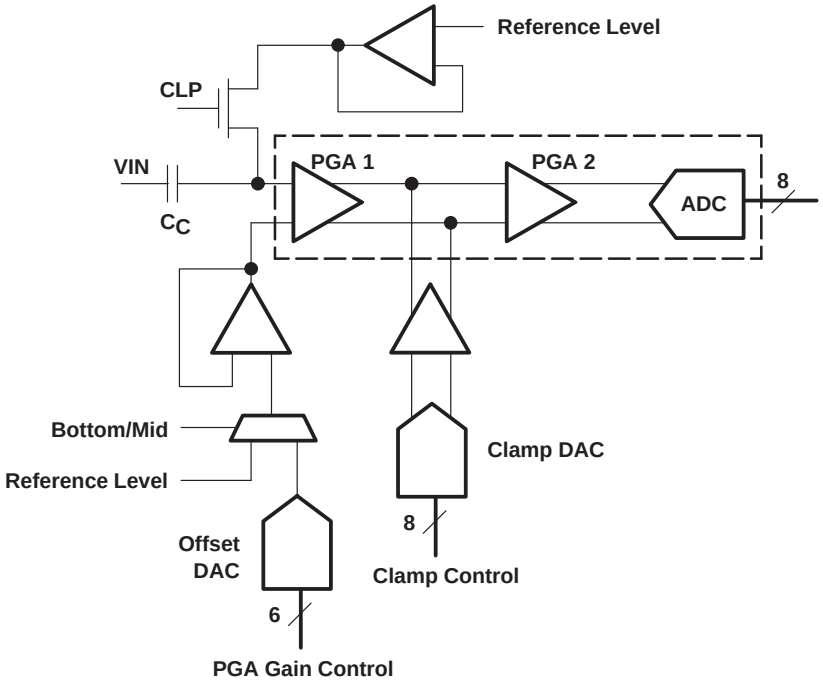


Figure 2–1. Analog Channel Architecture

In the case of YUV input signals, blanking levels for U and V correspond to the mid-level analog input. To handle these signals the clamping range should be centered on the mid-level output code of the A/D.

The clamp code is 8 bits wide and spans 128 ADC output codes (a 2 LSB change to clamp code corresponds nominally to 1 LSB change in ADC output). The programmed clamp code is independent of the PGA setting (see later). This ensures independent brightness/clamping control.

The clamp pulse defines the timing window during which the clamp circuit is internally enabled, and is either generated externally and supplied to the device, or it can be internally generated. In the latter case, the user can program both the position and width of the clamp pulse with respect to the horizontal sync (HS) input.

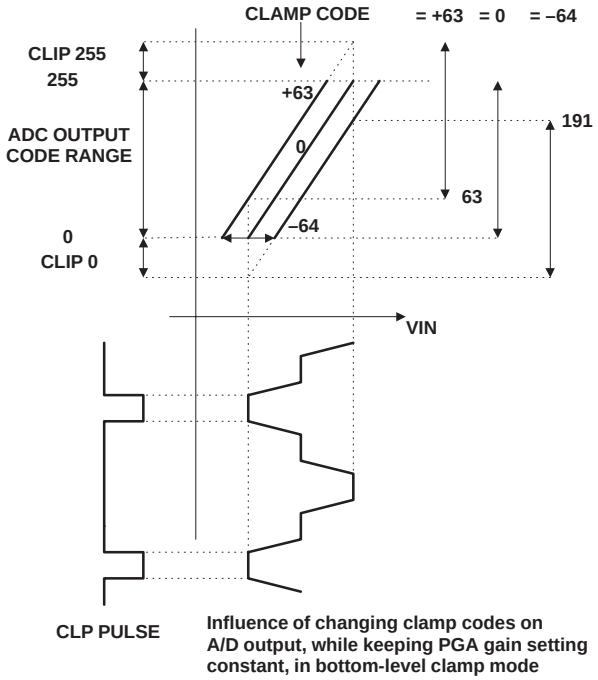


Figure 2–2. Bottom-Level Clamping

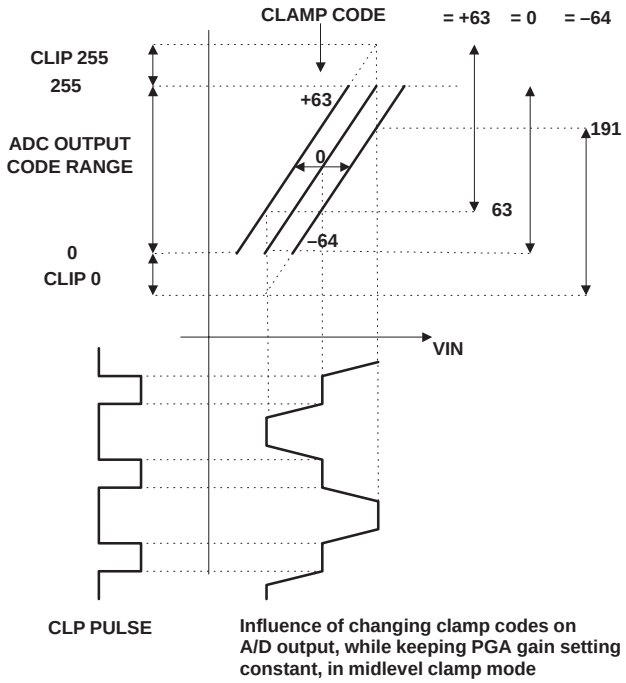


Figure 2–3. Mid-Level Clamping

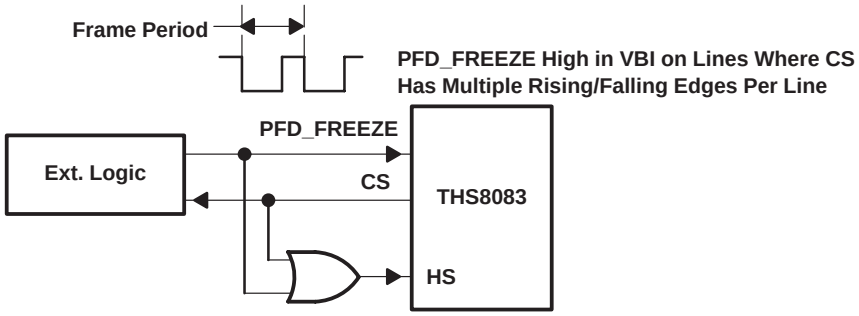
2.3 Composite Sync Slicer

The THS8083 includes a circuit that will compare the input signal on Ch.1 to a level 150 mV below the blanking level. This slicer will output on the composite sync (CS) pin a 3-V compatible digital output. The intended use of this circuit is for input video signals that have an embedded (negative or trilevel) sync. This is the case for workstation-type input signals or the DTV analog interface that mandates sync-on-Y. Since the sync amplitude is ~300 mV, the slicing level is at about 50% of the sync level. When enabled, the CS output is available even when the device is powered down.

CS will output the extracted composite sync. Since the PLL will be prevented from updating its phase detector while the PFD_FREEZE pin is kept high, the user asserts PFD_FREEZE during the VBI (when CS has multiple transitions per line). This puts the PLL in free-run. While it cannot be guaranteed with devices that have analog PLL's, the digital PLL in the THS8083 is assured to keep a constant output frequency and avoid frequency drift while the PLL is in free-run. There is also no maximum on the time that PFD_FREEZE can be kept asserted to still keep a stable PLL output frequency. In this case, the CS output can be directly connected to the THS8083's HS input for purposes of locking the PLL. However, the frequency monitoring of HS, that works off signal edges, will produce invalid numbers on those lines where CS is present because of the multiple low-high transitions on these lines.

Alternatively, if an external sync separator is present that generates HS and VS from CS, the separated signals can be fed to the corresponding inputs on the THS8083 and PFD_FREEZE can be left unused. As long as both signals generate only 1 pulse per line respectively frame, the PLL will lock correctly and HS/VS frequency monitoring will be accurate. Both options are shown in Figure 2–4.

Option 1: Using PFD_FREEZE



Option 2: Using HS Derived From CS

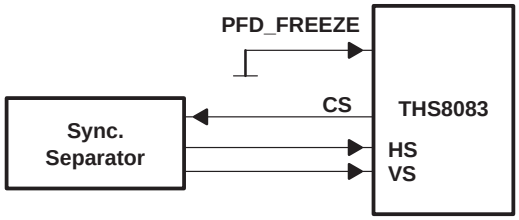


Figure 2–4. Using THS8083 With a Composite Sync

Note that the slicer will only work when no video levels are lower than the blanking level and when the internal clamp circuit is used. This is normally satisfied for G and Y channels, but not for U and V channels. To prevent unnecessary toggling of the CS output signal, the CS output is switched off automatically when mid-level clamping is chosen for channel 1 (i.e., CLP1_RG=1 in register <CLP_CTRL>). CS can be permanently disabled by setting CS_DIS=1 in register <AUX_CTRL>. So the state of CS is determined as follows:

CS_ENABLED = NOT (CS_DIS) AND NOT (CLP1_RG).

When CS_ENABLED=0, the CS output will be Hi-Z.

NOTE:

While PFD_FREEZE keeps the DTO output frequency constant, it does not disable the phase/frequency detector (PFD) from internally updating its error value at every active edge on HS. Therefore, when deasserting PFD_FREEZE and no external sync separator is used, a discontinuity on the frequency increment to the DTO occurs which will cause an instantaneous frequency shift. To prevent this, the user should gate the CS signal externally with the PFD_FREEZE signal as shown in Figure 2.4. This will keep the PFD from updating during PFD_FREEZE high, since HS will remain low during the VBI. By using both PFD_FREEZE and gating during the vertical blanking interval, THS8083 can be locked to signals with a composite sync.

To support sync-on-Y/sync-on-G extraction, the user should provide an external dc biasing to the Y/G channel. This can be done by establishing a dc clamp through a diode with its cathode connected to the ac-coupling capacitor (at the side of THS8083) on the AGY channel and anode connected to a dc level. Since the slicing level is around 1.35 V and the sync amplitude is ~300 mV, the negative sync-tip should be clamped by the diode to a level of approximately 1.2 V. For example, using a Schottky switching diode (type 1N5711) with a low forward voltage drop of maximum 0.4 V, the dc level at the anode can be approximately 1.6 V. This level can be derived through a resistive voltage divider off the power supply.

2.4 Programmable Gain Amplifier (PGA)

Each video channel is passed through a programmable gain amplifier, to provide a full-scale signal to each A/D. The user can change this gain via register programming. A gain change becomes effective immediately.

The range of the PGA is such that an input ac range from 0.4 Vpp to 1.2 Vpp can be scaled to ADC full scale, by maximum gain and minimum gain settings respectively.

The PGA is split into a 6-bit coarse gain control and 5-bit fine gain control. Their combination leads to a PGA resolution of better than 1 LSB on the ADC output code.

The bandwidth of the PGA is by design constant, resulting in a constant analog video input bandwidth.

The coarse PGA, with its 64 settings, covers a 4/3 x to 4x gain change, used for a 0.4 V (0.4 Vpp $\times$ 4 = 1.6 Vpp) respectively 1.2 Vpp (1.2 Vpp $\times$ 4/3 = 1.6 Vpp) input range swing.

While an amplifier with variable gain implements the coarse PGA, the fine PGA is implemented by slightly changing the top and bottom reference levels that are also independently controllable for each ADC channel. The fine range, with its 32 settings, covers a range of 16 LSBs.

The fine and coarse PGA settings can be combined into a single PGA gain formula as follows:

$$\text{GAIN} = (4/3 + C/24)(1 + (F–15)/512)$$

Where C is the coarse gain setting (0..63) and F the fine gain setting (0..31).

2.5 A/D Converter

The A/D converter is based on the core used in the TLV5580 (single 8-bit 80 MSPS A/D). The switched-capacitor single-pipeline CMOS architecture combines excellent signal-to-noise characteristics with a very wide 3-dB analog input bandwidth of typically 500 MHz. The A/D block contains an internal reference voltage generator, providing stable bottom and top references derived from an internal bandgap reference. The reference voltages are made available externally. The THS8083 supports ac-coupled input (clamping circuit).

The A/D converter will have no missing codes up to 80 MSPS (THS8083) or 95 MSPS (THS8083-95) if used as defined in section 5, *Electrical Specification*. The sampling clock of the A/D converter is either fed from external or generated internally by the PLL.

2.6 PLL

The PLL is a fully contained functional block consisting of:

- An analog PLL operating at a fixed output frequency of N times the master (crystal) clock frequency;
- A digital PLL containing a digital phase-frequency detector (PFD), a discrete time oscillator (DTO), a digital loop filter, a feedback divider, a programmable clock output divider, and a programmable phase shifter.

2.6.1 Analog PLL

The analog PLL generates a high-frequency internal clock that will be used by the DTO in the digital PLL to derive the pixel output frequency with programmable phase. The reference signal for this PLL is the master clock frequency supplied on the XTL1-MCLK terminal.

Two options exist for connecting a master clock:

- A crystal can be connected between the XTL1-MCLK and XTL2 terminals. The device provides internal oscillator circuitry.
- A 3.3-V CMOS/TTL clock signal can be connected to XTL1-MCLK from an external oscillator. In this case XTL2 must be left unconnected.

The port is designed to operate from a master clock frequency of 14.31818 MHz, which is a standard frequency in video applications: 4x the subcarrier frequency for NTSC. Many low-cost crystals are available for this frequency. Default the internal oscillator will operate at 8x the master clock frequency, so about 114 MHz. This setting of 8x, which is the value of the feedback divider in the analog PLL loop, is programmable (VCODIV register value). The user can change this value when a master clock of a different frequency is connected. In this case care should be taken to keep the internal high-frequency clock (i.e., master clock frequency x analog feedback divider) lower than 120 MHz. The higher this internal frequency, the better the frequency resolution of the DTO.

When a crystal is used as the master clock source, it is not advised to use another frequency than the recommended 14.31818 MHz, since the internal oscillator circuitry is not production tested at other frequencies. If another master clock is used, it is recommended to drive XTL1–MCLK by a direct clock signal. VCODIV should be programmed such that the internal clock remains close to but less than 120 MHz.

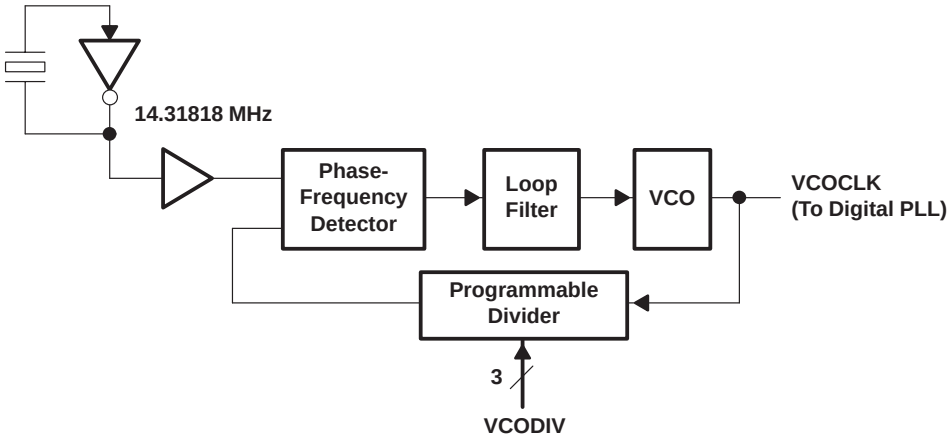


Figure 2–5. Analog PLL

2.6.2 Digital PLL

The digital PLL loop derives the ADC (pixel) clock frequency from the high-speed internal clock. A DTO will generate an output frequency from a user-programmable DTO increment. To operate over the 13.5–80 or 95 MHz range, an extra DTO clock output divider can be switched in. Appendix A shows the formula that relates the frequency of the internal high-speed clock, the DTO increment value, and the DTO clock output divider to the PLL output frequency.

The PLL output, after the clock divider, is sent to the programmable feedback divider (TERM_CNT register value). This value will typically be programmed to the number of total pixels per line for a given video/graphics format. The output of this divider is then one input to the phase-frequency detector. Its other input is typically the horizontal sync (HS) reference of a graphics/video signal. HS needs to be provided as a separate TTL/CMOS type signal to the dedicated input terminal; See section 2.3 *Composite Sync Slicer*, to use the PLL in the case of input signals with a composite sync. The polarity of HS is programmable (HS_POL register value).

Both HS and VS inputs on the THS8083 can accept a 3-V and a 5-V logic-compliant signal.

On the HS input, as on the VS input, a digital noise gate can be optionally switched in (HS_MS respectively VS_MS register values). The user can program the minimum number of clock cycles that HS and VS have to be present before they are interpreted as a valid HS and VS. This avoids having any spikes being interpreted as e.g. an active HS and falsely updating the PLL.

The PFD produces a digital error value, signaling the phase/frequency difference between the HS input and the divided PLL output clock. The integrated digital PLL loop filter subsequently filters this error value. This filter consists of a proportional and integrator (accumulator) part. Gains of both parts are programmable (GAIN_N and GAIN_P register values), each with eight settings. The higher the programmed value, the higher the gain in either the proportional or integrator portions of the filter, which translates into a wider capture range and faster acquisition but also higher steady-state jitter.

The PFD also provides a LOCK output on a dedicated output terminal. This output has a programmable hysteresis (LD_THRES register value). Details are explained in the section that describes the register map of this device. The LOCK output is made available on a dedicated pin so that the user could implement additional functionality before using this output (e.g., implement sticky nature of an unlock condition by routing it through an external set/reset flip-flop).

By integrating the loop filter and making it programmable, the user can trade off both at runtime depending on the quality of the incoming HS signal (inaccurate frequency, jitter content).

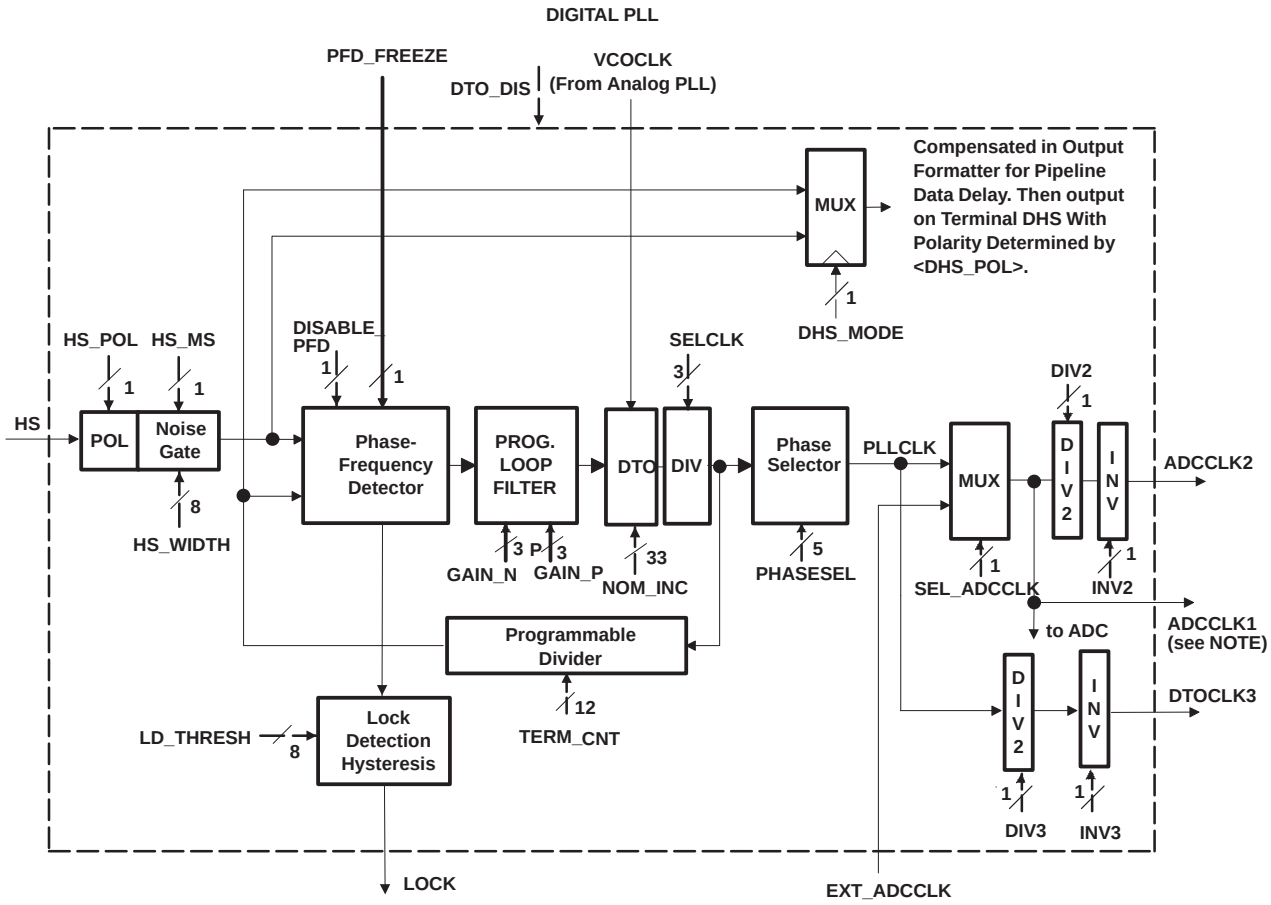
The filtered phase/frequency error value is now used to correct the programmed nominal DTO increment (NOM_INC register value) to the instantaneous DTO increment (DTO_INC reported value). This updated DTO increment determines the instantaneous DTO output frequency. By making DTO_INC available as a read-only register, the user can read out via I^2C and calculate the instantaneous frequency of the DTO generated clock.

Because of the digital nature of the PLL, the loop can be opened while still keeping an accurate frequency output. Therefore, the PLL can also be used as a frequency synthesizer, without any HS reference. This is done by disabling the PFD (PFD_DISABLE register value). This will keep DTO_INC always equal to NOM_INC, thereby producing a DTO output frequency always equal to the desired programmed frequency, irrespective of HS.

There is a second option to operate in open loop though. In some video/graphics modes no valid HS is present during a part of the frame/field period, typically during some lines of the VBI (vertical blanking interval). In order to have an accurate PLL output clock and avoid clock drift, the PFD output needs to be held constant during this time. The PFD FREEZE pin provides this option. Asserting this will freeze DTO_INC to its present value, thereby producing a constant PLL output clock frequency, not necessarily equal to the nominal desired frequency programmed by NOM_INC. Together with the composite sync slicer, this feature allows the use of the PLL for input signals with embedded composite sync with minimal external logic. See Composite Sync Slicer section.

The phase of the PLL generated clock can be programmed in 31 uniform steps over a single clock period (360/31 = 11.6 degrees phase resolution) so that the sampling phase of the ADC's can be controlled accurately.

Next to sourcing the ADC channel clock from the PLL, the option exists to use an external pixel clock (from terminal EXT_ADCCLK). If configured this way (via SEL_ADCCLK register value), a clock signal of the required sampling frequency should be applied to EXT_ADCCLK and this signal, instead of the PLL generated clock, is routed to the ADC channels. No phase control is available in this case on the external clock signal. Still, the internal PLL can be used and its output available externally as explained below. This means two clock domains can be implemented on THS8083: a first one from externally fed, a second one, possibly asynchronous to the first, generated by the internal PLL. This provides considerable flexibility in the design of video/graphics equipment that implements scaling and frame rate conversion.



NOTE: ADCCLK1 is used by the output formatter to generate the DATACLK1 output.

Figure 2–6. Digital PLL

The device provides three clock outputs. One of these output signals, DATACLK1, is derived from the ADC clock output. It is actually equal to the sampling clock but compensated in phase so that its rising edge always corresponds to the center valid region of the output data. Output data timing (setup/hold) is specified with respect to this rising edge. Therefore, DATACLK1 is typically used for clocking the THS8083's output data. The frequency of DATACLK1 will be either equal or 1/2 of the sampling clock, depending on the operation mode of the output formatter. When the THS8083 is clocked with an external sampling clock, this external clock is used as the source to generate DATACLK1 in the output formatter.

The second clock output, ADCCLK2, is equal to the ADC sampling clock but can optionally be divided by 2 and inverted.

Finally, the third clock output, DTOCLK3, is always derived from the PLL output clock, irrespective of the use of an external sampling clock on EXT_ADCCLK. So, when operating with an external sampling clock, the DTOCLK3 output can be used to generate a second, possibly asynchronous, clock signal in either open loop operation or in closed loop locked to a reference HS input. Also, DTOCLK3 can be optionally divided by 2 and inverted.

The divide and invert functions are implemented to enable a master/slave operation of two parts in case higher sampling speeds than 80/95MSPS are required. In this case the master will use its PLL to generate a line-locked clock, of which the inverse will be used as an external sampling clock by the second slave device.

2.7 Output Formatter

This block enables either a 4:4:4 24-bit output or 4:4:4 48-bit output at half the pixel clock or a 4:2:2 16-bit output, useful for YUV digitizing (ITU.BT-601 style). In the latter case, an 8-bit port is used for the Y output, while a second 8-bit port is used alternately for Cr and Cb. As per ITU BT-601, Cb is the first video data word for each line, as shown in Figure 2-7.

The first color sample after an incoming HS will be Cb. The output signal DHS is synchronized to the first pixel of a line and can therefore be used to uniquely identify Cb from Cr output data in downsampled modes.

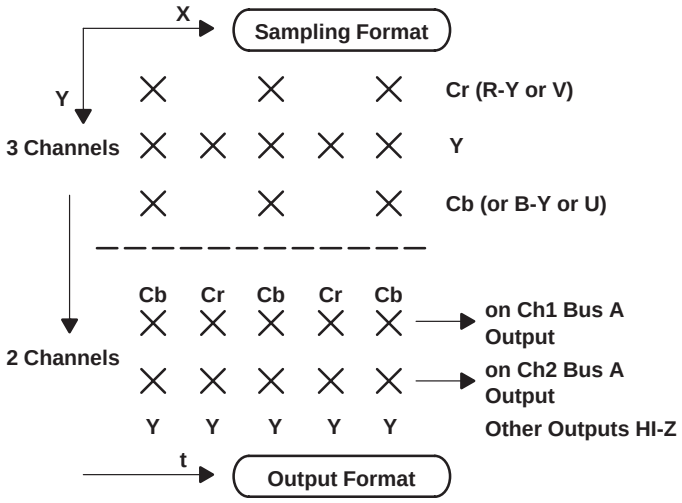


Figure 2–7. Output Formatter

2.8 Power Down

In the I^{2}C power-down register, four power down modes are defined:

- Chip power down: PWDN_ALL
  When PWDN_ALL=1, all analog circuits are powered down except the internal bandgap reference, the circuit that generates the clamping voltages and the sync reference voltage. All these are kept active for the composite sync slicer that remains active during power down. The clock frequency of the digital circuitry will be lowered to reduce power consumption when in power down.
- Internal reference power down: PWDN_REF
  When PWDN_REF=1, bottom and top references (VREFB, VREFT) on all channels become inputs and should be driven from external.
- Bandgap reference power down: PWDN_BGAP
  When PWDN_BGAP=1, the internal bandgap reference voltage is inactive and terminal VMID should be driven from external.
- DTO power down: DTO_DIS
  When DTO_DIS=1, the DTO frequency is lowered to reduce power dissipation. When an external sampling clock is used (EXT_ADCCLK), this power down can be activated.

2.9 Input Mode Detection

The THS8083 supports detection of the graphics input format in co-operation with an external microcontroller. Via the microcontroller interface the period of incoming HS and VS signals can be measured (HS_COUNT, VS _COUNT register values), as well as the frequency of the DTO clock (DTO_INC register value) and the PLL lock condition (terminal LOCK).

2.10 Test Mode

The ADC output data on each of the three channels can be sampled at a programmable position on each line (PIXTRAP register value) and latched into pixel readback registers (CH<n>_RDBK register values) that can be read by the microcontroller at lower speed via the I^2C interface. When programmed to read back during the horizontal blanking interval this can be a test for accurate positioning of the blanking level.

3 Register Definition

3.1 I2C Protocol

The THS8083 is a slave I2C device on which both write and read are supported. As shown in the register map, there are some status control registers that can only be read.

The device can support FAST I2C mode (SCL up to 400 kHz) when the DTO clock is running at over 25 MHz; at lower DTO frequencies only NORMAL I2C mode (SCL up to 100 kHz) is supported.

To discriminate between write and read operations, the device is addressed at separate device addresses. There is an automatic internal subaddress increment counter to efficiently write/read multiple bytes in the register map during one write/read operation. Furthermore, bit1 of the I2C device address is dependent upon the setting of the I2CA pin, as follows:

If address selecting pin I2CA = 0, then

WRITE address is 40 hex (01000000)

READ address is 41 hex (01000001)

If address selecting pin I2CA = 1, then

WRITE address is 42 hex (01000010)

READ address is 43 hex (01000011)

3.1.1 Write Format

S	Slave address(w)	A	Sub-address	A	Data0	A	……	Data(N–1)	A	P

S	Start condition
Slave address(w)	0100000 (0x40) if I2CA=0 / 01000010 (0x42) if I2CA=1
A	Acknowledge, it is generated by THS8083
Subaddress	Subaddress of the 1st register to write, length: 1 byte
Data0	First byte of the data
Data(N–1)	Nth byte of the data
P	Stop condition

3.1.2 Read Format

First write the subaddress, where data needs to be read out, to THS8083 in the format as follows:

S	Slave address(w)	A	Subaddress	A	P

Then:

S	Slave address(r)	A	DataN	AM	Data(N+1)	AM	……	NAM	P

S	Start condition
Slave address(r)	01000001 (0x41) if I2CA=0 / 01000011 (0x43) if I2CA=1
A	Acknowledge, it is generated by THS8083; if the transmission is successful, then A = 0, else A = 1
AM	Acknowledge, it is generated by a master
NAM	Not acknowledge, it is generated by a master
Subaddress	Subaddress of the first register to read, length = one byte
Data0	First byte of the data read
Data(N–1)	Nth byte of the data read
P	Stop condition

In both write and read operations, the subaddress will be incremented automatically when multiple bytes are written/read. So, only the first subaddress needs to be supplied to the THS8083.

R/W registers can be written and read.

R registers are read-only.

Table 3–1. I²C Register Map

REGISTER NAME	R/W	SUB ADDRESS	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TERM_CNT_0	R/W	00	TERM_CNT7	TERM_CNT6	TERM_CNT5	TERM_CNT4	TERM_CNT3	TERM_CNT2	TERM_CNT1	TERM_CNT0
TERM_CNT_1	R/W	01					TERM_CNT11	TERM_CNT10	TERM_CNT9	TERM_CNT8
NOM_INC_0	R/W	02	NOM_INC7	NOM_INC6	NOM_INC5	NOM_INC4	NOM_INC3	NOM_INC2	NOM_INC1	NOM_INC0
NOM_INC_1	R/W	03	NOM_INC15	NOM_INC14	NOM_INC13	NOM_INC12	NOM_INC11	NOM_INC10	NOM_INC9	NOM_INC8
NOM_INC_2	R/W	04	NOM_INC23	NOM_INC22	NOM_INC21	NOM_INC20	NOM_INC19	NOM_INC18	NOM_INC17	NOM_INC16
NOM_INC_3	R/W	05	NOM_INC31	NOM_INC30	NOM_INC29	NOM_INC28	NOM_INC27	NOM_INC26	NOM_INC25	NOM_INC24
NOM_INC_4	R/W	06								NOM_INC32
VCODIV	R/W	07						VCODIV2	VCODIV1	VCODIV0
SELCLK	R/W	08							SELCLK1	SELCLK0
PHASESEL	R/W	09				PHASE_SEL4	PHASE_SEL3	PHASE_SEL2	PHASE_SEL1	PHASE_SEL0
PLLFILT	R/W	0A			GAIN_N2	GAIN_N1	GAIN_N0	GAIN_P2	GAIN_P1	GAIN_P0
HS_WIDTH	R/W	0B	HS_WIDTH7	HS_WIDTH6	HS_WIDTH5	HS_WIDTH4	HS_WIDTH3	HS_WIDTH2	HS_WIDTH1	HS_WIDTH0
VS_WIDTH	R/W	0C	VS_WIDTH7	VS_WIDTH6	VS_WIDTH5	VS_WIDTH4	VS_WIDTH3	VS_WIDTH2	VS_WIDTH1	VS_WIDTH0
SYNC_CTRL	R/W	0D					HS_POL	HS_MS	VS_POL	VS_MS
LD_THRES	R/W	0E	LD_THRES7	LD_THRES6	LD_THRES5	LD_THRES4	LD_THRES3	LD_THRES2	LD_THRES1	LD_THRES0
PLL_CTRL	R/W	0F			DISABLE_PFD	SEL_ADCCLK	INV2	DIV2	INV3	DIV3
HS_COUNT_0	R	10	HS_COUNT7	HS_COUNT6	HS_COUNT5	HS_COUNT4	HS_COUNT3	HS_COUNT2	HS_COUNT1	HS_COUNT0
HS_COUNT_1	R	11					HS_COUNT11	HS_COUNT10	HS_COUNT9	HS_COUNT8
VS_COUNT_0	R	12	VS_COUNT7	VS_COUNT6	VS_COUNT5	VS_COUNT4	VS_COUNT3	VS_COUNT2	VS_COUNT1	VS_COUNT0
VS_COUNT_1	R	13					VS_COUNT11	VS_COUNT10	VS_COUNT9	VS_COUNT8
DTO_INC_0	R	14	DTO_INC7	DTO_INC6	DTO_INC5	DTO_INC4	DTO_INC3	DTO_INC2	DTO_INC1	DTO_INC0
DTO_INC_1	R	15	DTO_INC15	DTO_INC14	DTO_INC13	DTO_INC12	DTO_INC11	DTO_INC10	DTO_INC9	DTO_INC8
DTO_INC_2	R	16	DTO_INC23	DTO_INC22	DTO_INC21	DTO_INC20	DTO_INC19	DTO_INC18	DTO_INC17	DTO_INC16
DTO_INC_3	R	17	DTO_INC31	DTO_INC30	DTO_INC29	DTO_INC28	DTO_INC27	DTO_INC26	DTO_INC25	DTO_INC24
DTO_INC_4	R	18								DTO_INC32
SYNC_DETECT	R	19								NO_SYNC
Reserved		1A-1F								

NOTE: Blank register bits in this table are ignored upon write. When read they return 0.

Table 3–1. I²C Register Map (continued)

REGISTER NAME	R/W	SUB ADDRESS	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLP_CTRL	R/W	20		CLP_SEL	CLP1_EN	CLP1_RG	CLP2_EN	CLP2_RG	CLP3_EN	CLP3_RG
CLP_START_0	R/W	21	CLP_START7	CLP_START6	CLP_START5	CLP_START4	CLP_START3	CLP_START2	CLP_START1	CLP_START0
CLP_START_1	R/W	22					CLP_START11	CLP_START10	CLP_START9	CLP_START8
CLP_STOP_0	R/W	23	CLP_STOP7	CLP_STOP6	CLP_STOP5	CLP_STOP4	CLP_STOP3	CLP_STOP2	CLP_STOP1	CLP_STOP0
CLP_STOP_1	R/W	24					CLP_STOP11	CLP_STOP10	CLP_STOP9	CLP_STOP8
CH1_CLP	R/W	25	CH1_CLP7	CH1_CLP6	CH1_CLP5	CH1_CLP4	CH1_CLP3	CH1_CLP2	CH1_CLP1	CH1_CLP0
CH1_COARSE	R/W	26			CH1_COARSE5	CH1_COARSE4	CH1_COARSE3	CH1_COARSE2	CH1_COARSE1	CH1_COARSE0
CH1_FINE	R/W	27				CH1_FINE4	CH1_FINE3	CH1_FINE2	CH1_FINE1	CH1_FINE0
CH2_CLP	R/W	28	CH2_CLP7	CH2_CLP6	CH2_CLP5	CH2_CLP4	CH2_CLP3	CH2_CLP2	CH2_CLP1	CH2_CLP0
CH2_COARSE	R/W	29			CH2_COARSE5	CH2_COARSE4	CH2_COARSE3	CH2_COARSE2	CH2_COARSE1	CH2_COARSE0
CH2_FINE	R/W	2A				CH2_FINE4	CH2_FINE3	CH2_FINE2	CH2_FINE1	CH2_FINE0
CH3_CLP	R/W	2B	CH3_CLP7	CH3_CLP6	CH3_CLP5	CH3_CLP4	CH3_CLP3	CH3_CLP2	CH3_CLP1	CH3_CLP0
CH3_COARSE	R/W	2C			CH3_COARSE5	CH3_COARSE4	CH3_COARSE3	CH3_COARSE2	CH3_COARSE1	CH3_COARSE0
CH3_FINE	R/W	2D				CH3_FINE4	CH3_FINE3	CH3_FINE2	CH3_FINE1	CH3_FINE0
PIX_TRAP_0	R/W	2E	PIX_TRAP7	PIX_TRAP6	PIX_TRAP5	PIX_TRAP4	PIX_TRAP3	PIX_TRAP2	PIX_TRAP1	PIX_TRAP0
PIX_TRAP_1	R/W	2F					PIX_TRAP11	PIX_TRAP10	PIX_TRAP9	PIX_TRAP8
PWDN_CTRL	R/W	30				PWDN_ALL		PWDN_REF	PWDN_BGAP	DTO_DIS
AUX_CTRL	R/W	31				CS_DIS	TEST2	TEST1	TEST0	TACT
CH1_RDBK	R	32	CH1_RDBK7	CH1_RDBK6	CH1_RDBK5	CH1_RDBK4	CH1_RDBK3	CH1_RDBK2	CH1_RDBK1	CH1_RDBK0
CH2_RDBK	R	33	CH2_RDBK7	CH2_RDBK6	CH2_RDBK5	CH2_RDBK4	CH2_RDBK3	CH2_RDBK2	CH2_RDBK1	CH2_RDBK0
CH3_RDBK	R	34	CH3_RDBK7	CH3_RDBK6	CH3_RDBK5	CH3_RDBK4	CH3_RDBK3	CH3_RDBK2	CH3_RDBK1	CH3_RDBK0
Reserved		35-3F								
OFM_CTRL	R/W	40					DHS_MODE	DHS_POL	OFM_MODE1	OFM_MODE0

NOTE: Blank register bits in this table are ignored upon write. When read they return 0.

3.2 Register Description

Register values after reset/at power up/after power down mode: The default value with each register shows the startup condition after general chip reset. The register state after power up is undefined i.e., the device requires a reset after power up ($\overline{\text{RESET}}$ low) to put all registers in their default states. The value of these registers is preserved in all power-down modes (i.e. after power down the register values are identical as when entering power down); they do not return to their default values under this condition. In order for the device to reset correctly, a master clock signal needs to be applied during reset from either a clock signal on XTL1–MCLK or a crystal connected between XTL1–MCLK and XTL2. The reset signal needs to be at least 5 clock cycles wide.

Default values: The default values for this device are set for XGA@78.75 MHz.

3.2.1 Register Name: TERM_CNT_0 Subaddress: 00 (R/W)

MSB							LSB
TERM_CNT7	TERM_CNT6	TERM_CNT5	TERM_CNT4	TERM_CNT3	TERM_CNT2	TERM_CNT1	TERM_CNT0

TERM_CNT[7..0]:

TERM_CNT[11..0] sets the number of pixels per line. Controls the digital PLL feedback divider.
Default: 0x20

3.2.2 Register Name: TERM_CNT_1 Subaddress: 01 (R/W)

MSB							LSB
X	X	X	X	TERM_CNT11	TERM_CNT10	TERM_CNT9	TERM_CNT8

TERM_CNT[11..8]:

See register TERM_CNT_0.
Default: 0x5

Default TERM_CNT: 0x520 = 1312 pixels/line (XGA@75 Hz)

3.2.3 Register Name: NOM_INC_0 Subaddress: 02 (R/W)

MSB							LSB
NOM_INC7	NOM_INC6	NOM_INC5	NOM_INC4	NOM_INC3	NOM_INC2	NOM_INC1	NOM_INC0

NOM_INC[7..0]:

NOM_INC[32..27]: integer part of DTO increment value
NOM_INC[26..0] : fractional part of DTO increment value
[See appendix A for how to calculate the increment]
Default: 0x45

3.2.4 Register Name: NOM_INC_1 Subaddress: 03 (R/W)

MSB							LSB
NOM_INC15	NOM_INC14	NOM_INC13	NOM_INC12	NOM_INC11	NOM_INC10	NOM_INC9	NOM_INC8

NOM_INC[15..8]:

See register NOM_INC_0.
Default: 0xF6

3.2.5 Register Name: NOM_INC_2 Subaddress: 04 (R/W)

MSB							LSB
NOM_INC23	NOM_INC22	NOM_INC21	NOM_INC20	NOM_INC19	NOM_INC18	NOM_INC17	NOM_INC16

NOM_INC[23..16]:

See register NOM_INC_0.
Default: 0xB9

3.2.6 Register Name: NOM_INC_3 Subaddress: 05 (R/W)

MSB							LSB
NOM_INC31	NOM_INC30	NOM_INC29	NOM_INC28	NOM_INC27	NOM_INC26	NOM_INC25	NOM_INC24

NOM_INC[31..24]:

See register NOM_INC_0.
Default: 0x70

3.2.7 Register Name: NOM_INC_4 Subaddress: 06 (R/W)

MSB							LSB
X	X	X	X	X	X	X	NOM_INC32

NOM_INC32:

See register NOM_INC_0
Default: 0x01

NOTE: The default value for NOM_INC is 0x 0170B9F645. Split into the 6-bit integer/ 27 bit fractional part, this can be written as 0x2e.0b9f645 or 46.090802 in decimal format. From Appendix A, it can be calculated that this will correspond to a DTO output frequency of 78.75 MHz (XGA@75Hz).

IMPORTANT: To properly update the increment it is required to program successively NOM_INC_0 to NOM_INC_4 and then repeat the programming of the two last bytes NOM_INC3 and NOM_INC4 in this order. By doing so, the DTO will be properly set to the new frequency.

3.2.8 Register Name: VCODIV Subaddress: 07 (R/W)

MSB							LSB
X	X	X	X	X	VCODIV2	VCODIV1	VCODIV0

VCODIV[2..0]:

Divider in analog PLL loop. Determines the internal master clock frequency as VCODIV x master clock frequency (from XTL1–MCLK/XTL2).

Default: 0x03 i.e., analog multiplier of 8 producing an internal nominal frequency of 8x14.31818 MHz

VCO_DIV[2..0]	ANALOG PLL MULTIPLIER
000	5
001	6
010	7
011 (default)	8
100	9
101	10
110	11
111	12

3.2.9 Register Name: SELCLK — Subaddress: 08 (R/W)

MSB							LSB
X	X	X	X	X	X	SELCLK1	SELCLK0

SELCLK[1..0]:

Selects a clock divider on the DTO output., as shown below:
Default: 0x00 i.e., DTO divider = 1 (no additional division).

SEL_CLK[1..0]	DIVIDER CLKDIV
00 (default)	1
01	2
10	4
11	8

To cover the complete range 10 – 80/95 MHz, SELCLK needs to be changed as well, as shown in the PLL section.

3.2.10 Register Name: PHASESEL — Subaddress: 09 (R/W)

MSB							LSB
X	X	X	PHASESEL4	PHASESEL3	PHASESEL2	PHASESEL1	PHASESEL0

PHASESEL[4..0]:

Sets the phase for the DTO clock output.
Default: 0x10 i.e., phase shift = 180 degrees

3.2.11 Register Name: PLLFILT — Subaddress: 0A (R/W)

MSB							LSB
X	X	GAIN_N2	GAIN_N1	GAIN_N0	GAIN_P2	GAIN_P1	GAIN_P0

GAIN_N[2..0]: PLL gain control: Sets the loop filter proportional time constant
Default: 0x7 (highest gain – lowest time constant)

GAIN_P[2..0]: PLL gain control: Sets the loop filter integrator time constant
Default: 0x7 (highest gain – lowest time constant)

NOTE: The higher the PLL gain setting, the less critical the initial DTO programming becomes since the device will have a wider lock-in range. However, once lock is acquired, this means any jitter on HS will be amplified. Therefore, for high jitter sources, it is recommended to apply more filtering once lock is acquired to filter out this HS jitter.

3.2.12 Register Name: HS_WIDTH — Subaddress: 0B (R/W)

MSB							LSB
HS_WIDTH7	HS_WIDTH6	HS_WIDTH5	HS_WIDTH4	HS_WIDTH3	HS_WIDTH2	HS_WIDTH1	HS_WIDTH0

HS_WIDTH[7..0]:

Sets the width in pixels for HS detection. If the width of the incoming HS is less than this number, it is ignored. The width in pixels of an incoming HS is incremented at each pixel following the active edge (of which the polarity can be programmed, see HS_POL)

Default: 0x00

3.2.13 Register Name: VS_WIDTH — Subaddress: 0C (R/W)

MSB							LSB
VS_WIDTH7	VS_WIDTH6	VS_WIDTH5	VS_WIDTH4	VS_WIDTH3	VS_WIDTH2	VS_WIDTH1	VS_WIDTH0

VS_WIDTH[7..0]:

Sets the width in pixels for VS detection. If the width of the incoming VS is less than this number, it is ignored.

Default: 0x00

3.2.14 Register Name: SYNC_CTRL — Subaddress: 0D (R/W)

MSB							LSB
X	X	X	X	HS_POL	HS_MS	VS_POL	VS_MS

HS_POL:

Controls the polarity of the incoming HS.
0 = positive polarity (default)
1 = negative polarity

HS_MS:

Controls the mux selection for activating the noise filter on incoming HS.
0 = noise filter disabled (default)
1 = noise filter enabled

VS_POL:

Controls the polarity of the incoming VS
0 = positive polarity (default)
1 = negative polarity

VS_MS:

Controls the mux selection for activating the noise filter on incoming VS
0 = noise filter disabled (default)
1 = noise filter enabled

3.2.15 Register Name: LD_THRES — Subaddress: 0E (R/W)

MSB							LSB
LD_THRES7	LD_THRES6	LD_THRES5	LD_THRES4	LD_THRES3	LD_THRES2	LD_THRES1	LD_THRES0

LD_THRES[7..0]:

Sets hysteresis for PLL lock-detection output.

An internal counter counts the number of subsequent lines onto which lock is found, as follows. For each line (HS) on which the PFD finds that the PLL is locked, the counter is incremented by 1. The counter clips at 255 maximum. For each line (HS) that the PLL is not locked to, the counter is decremented by 8. This counter starts from 0.

Lock is signaled externally (via the LOCK_DETECT output) when this internal counter holds a value higher than <LD_THRESHOLD>. Unlock is signaled externally when this internal counter holds a value less than or equal to <LD_THRESHOLD>. So, a value of 255 will never assert the lock signal although the PLL might be locked internally.

NOTE: the higher this value is set, the more critical the PFD will be to signal lock. Therefore, for high jitter HS inputs, this value will have to be lower than for high quality sources.

Default: 0x10 = 16

3.2.16 Register Name: PLL_CTRL Subaddress: 0F (R/W)

MSB							LSB
X	X	DISABLE_PFD	SEL_ADCCLK	INV2	DIV2	INV3	DIV3

DISABLE_PFD:

Disables updating of the DTO increment (i.e., keeps DTO output frequency constant and independent of the incoming HS frequency). This effect is similar as opening the PLL loop.

0 = PFD enabled

1 = PFD disabled (default): the DTO runs at a constant frequency, as determined by NOM_INC. This means the output frequency returns to the nominal value and further updating of the DTO output frequency is avoided (the PLL loop is open). This is chosen as the default mode to avoid false random frequency changes by the DTO caused by noise on the HS input. In normal operation the microprocessor will periodically check the SYNC_DETECT register. If sync is present/absent, then the PFD is enabled/disabled so, frequency drift is avoided when no input signal is present. Still the panel can be driven then by data with a nominal pixel frequency.

SEL_ADCCLK:

Selects the PLL clock or the clock signal on the EXT_ADCCLK pin, as the clock source for the ADC channels
0: internal clock selected (default)
1: external clock selected

INV2 :

Selects inverting or noninverting clock output on ADCCLK2 output pin.
0: the output is not inverted (default) with respect to the internal ADCCLK1 clock
1: the output is inverted with respect to the internal ADCCLK1 clock

DIV2:

Enables divide-by-2 function on the clock output of ADCCLK2
0: divide by 2 mechanism is disabled (default)
1: divide by 2 mechanism is enabled

INV3:

Selects inverting or noninverting output on DTOCLK3, with respect to the internal DTOCLK3 clock.
0: the output is not inverted (default)
1: the output is inverted

DIV3:

Enables divide-by-2 function on the clock output of DTOCLK3
0: divided by 2 mechanism is disabled (default)
1: divided by 2 mechanism is enabled

3.2.17 Register Name: HS_COUNT_0 Subaddress: 10 (R)

MSB							LSB
HS_COUNT7	HS_COUNT6	HS_COUNT5	HS_COUNT4	HS_COUNT3	HS_COUNT2	HS_COUNT1	HS_COUNT0

HS_COUNT[7..0]

HS_COUNT[11..0] holds the last horizontal sync period number (i.e., the number of pixel clock cycles between the last two HS occurrences). The device updates the value at each active edge of HS. Internal arbitration logic avoids potential read errors between the register contents and the asynchronous I^2C bus. This value can be read by the microcontroller to derive the line frequency of the incoming video/graphics format.

Default: (changed during operation)

3.2.18 Register Name: HS_COUNT_1 Subaddress: 11 (R)

MSB							LSB
X	X	X	X	HS_COUNT11	HS_COUNT10	HS_COUNT9	HS_COUNT8

HS_COUNT[11..8]:

See register HS_COUNT_0

Default: (changed during operation)

3.2.19 Register Name: VS_COUNT_0 Subaddress: 12 (R)

MSB							LSB
VS_COUNT7	VS_COUNT6	VS_COUNT5	VS_COUNT4	VS_COUNT3	VS_COUNT2	VS_COUNT1	VS_COUNT0

VS_COUNT[7..0]:

VS_COUNT[11..0] holds the last vertical sync period number (i.e., the number of line periods between the last two VS occurrences). The device updates the value at each active edge of VS. Internal arbitration logic avoids potential read errors between the register contents and the asynchronous I^2C bus. This value can be read by the microcontroller to derive the frame rate of the incoming video/graphics format.

Default: (changed during operation)

3.2.20 Register Name: VS_COUNT_1 Subaddress: 13 (R)

MSB							LSB
X	X	X	X	VS_COUNT11	VS_COUNT10	VS_COUNT9	VS_COUNT8

VS_COUNT[11..8]

See register VS_COUNT0
Default: (changed during operation)

3.2.21 Register Name: DTO_INC_0 Subaddress: 14 (R)

MSB							LSB
DTO_INC7	DTO_INC6	DTO_INC5	DTO_INC4	DTO_INC3	DTO_INC2	DTO_INC1	DTO_INC0

DTO_INC[7..0]

DTO_INC[32..0] stores the current value of the DTO increment. This can be read by the microcontroller to derive the actual pixel clock frequency.
Default: (changed during operation)

3.2.22 Register Name: DTO_INC_1 Subaddress: 15 (R)

MSB							LSB
DTO_INC15	DTO_INC14	DTO_INC13	DTO_INC12	DTO_INC11	DTO_INC10	DTO_INC9	DTO_INC8

DTO_INC[15..8]:

See register DTO_INC_0
Default: (changed during operation)

3.2.23 Register Name: DTO_INC_2 Subaddress: 16 (R)

MSB							LSB
DTO_INC23	DTO_INC22	DTO_INC21	DTO_INC20	DTO_INC19	DTO_INC18	DTO_INC17	DTO_INC16

DTOINC[23..16]:

See register DTO_INC_0
Default: (changed during operation)

3.2.24 Register Name: DTO_INC_3 Subaddress: 17 (R)

MSB							LSB
DTO_INC31	DTO_INC30	DTO_INC29	DTO_INC28	DTO_INC27	DTO_INC26	DTO_INC25	DTO_INC24

DTO_INC[31..24]:

See register DTO_INC_0.
Default: (changed during operation)

3.2.25 Register Name: DTO_INC_4 Subaddress: 18 (R)

MSB							LSB
X	X	X	X	X	X	X	DTO_INC32

DTO_INC32:

See register DTO_INC_0.
Default: (changed during operation)

3.2.26 Register Name: SYNC_DETECT Subaddress: 19 (R)

MSB							LSB
X	X	X	X	X	X	X	NO_SYNC

NO_SYNC:

Sync detection on HS.
0 = HS present
1 = HS missing
Default: (changed during operation)

3.2.27 Register Name: CLP_CTRL Subaddress: 20 (R/W)

MSB							LSB
	CLPSEL	CLP1_EN	CLP1_RG	CLP2_EN	CLP2_RG	CLP3_EN	CLP3_RG

CLPSEL Selects the clamp timing signal

0: internal clamp timing pulse is selected (default)
1: external clamp timing pulse is selected

CLP1_EN: Enables/disables clamping on Channel 1.

1: enable (default)
0: disable

CLP1_RG: Sets the clamp range for Channel 1.

1: middle range

0: bottom range (default)

CLP2_EN: Enables/disables clamping on Channel 2.

1: enable (default)

0: disable

CLP2_RG: Sets the clamp range for Channel 2.

1: middle range

0: bottom range (default)

CLP3_EN: Enables/disables clamping on Channel 3.

1: enable (default)

0: disable

CLP3_RG: Sets the clamp range for Channel 3.

1: middle range

0: bottom range (default)

3.2.28 Register Name: CLP_START_0 Subaddress: 21 (R/W)

MSB							LSB
CLP_START7	CLP_START6	CLP_START5	CLP_START4	CLP_START3	CLP_START2	CLP_START1	CLP_START0

CLP_START[7..0]:

CLP_START[11..0] sets the pixel count value that defines the start of the internal clamping pulse. If external clamping is selected (via CLPSEL) this value has no meaning.
Default: 0x2

3.2.29 Register Name: CLP_START_1 Subaddress: 22 (R/W)

MSB							LSB
X	X	X	X	CLP_START11	CLP_START10	CLP_START9	CLP_START8

CLP_START[11..8]:

See register CLP_START_0
Default: 0x00

3.2.30 Register Name: CLP_STOP_0 Subaddress: 23 (R/W)

MSB							LSB
CLP_STOP7	CLP_STOP6	CLP_STOP5	CLP_STOP4	CLP_STOP3	CLP_STOP2	CLP_STOP1	CLP_STOP0

CLP_STOP[7..0]:

CLP_STOP[11..0] sets the pixel count value that defines the end of the internal clamping pulse. If external clamping is selected (via CLPSEL) this value has no meaning.
Default: 0x40 = 64

3.2.31 Register Name: CLP_STOP_1 Subaddress: 24 (R/W)

MSB							LSB
X	X	X	X	CLP_STOP11	CLP_STOP10	CLP_STOP9	CLP_STOP8

CLP_STOP[11..8]:

See register CLP_STOP_0
Default: 0x00

NOTE: A setting of about 62 clamp clk cycles is sufficient to guarantee enough clamp timing (>500 ns) at worst case (=highest clock frequency).

3.2.32 Register Name: CH1_CLP Subaddress: 25 (R/W)

MSB							LSB
CH1_CLP7	CH1_CLP6	CH1_CLP5	CH1_CLP4	CH1_CLP3	CH1_CLP2	CH1_CLP1	CH1_CLP0

CH1_CLP[7..0]

Programmable clamp value for Channel 1.
Default: 0x80 = 128 (mid-range)

3.2.33 Register Name: CH1_COARSE Subaddress: 26 (R/W)

MSB							LSB
X	X	CH1_COARSE5	CH1_COARSE4	CH1_COARSE3	CH1_COARSE2	CH1_COARSE1	CH1_COARSE0

CH1_COARSE[5..0]

Coarse PGA value for Channel 1
Default: 0x20 = 32 (mid-range)

3.2.34 Register Name: CH1_FINE Subaddress: 27 (R/W)

MSB							LSB
X	X	X	CH1_FINE4	CH1_FINE3	CH1_FINE2	CH1_FINE1	CH1_FINE0

CH1_FINE[4..0]

Fine PGA value for Channel 1.
Default: 0x10 = 16 (mid-range)

3.2.35 Register Name: CH2_CLP Subaddress: 28 (R/W)

MSB							LSB
CH2_CLP7	CH2_CLP6	CH2_CLP5	CH2_CLP4	CH2_CLP3	CH2_CLP2	CH2_CLP1	CH2_CLP0

CH2_CLP[7..0]

Programmable clamp value for Channel 2.
Default: 0x80 = 128 (mid-range)

3.2.36 Register Name: CH2_COARSE Subaddress: 29 (R/W)

MSB							LSB
X	X	CH2_COARSE5	CH2_COARSE4	CH2_COARSE3	CH2_COARSE2	CH2_COARSE1	CH2_COARSE0

CH2_COARSE[5..0]

Coarse PGA value for Channel 2.
Default: 0x20 = 32 (mid-range)

3.2.37 Register Name: CH2_FINE Subaddress: 2A (R/W)

MSB							LSB
X	X	X	CH2_FINE4	CH2_FINE3	CH2_FINE2	CH2_FINE1	CH2_FINE0

CH2_FINE[4..0]

Fine PGA value for Channel 2.
Default: 0x10 = 16 (mid-range)

3.2.38 Register Name: CH3_CLP — Subaddress: 2B (R/W)

MSB							LSB
CH3_CLP7	CH3_CLP6	CH3_CLP5	CH3_CLP4	CH3_CLP3	CH3_CLP2	CH3_CLP1	CH3_CLP0

CH3_CLP[7..0]

Programmable clamp value for Channel 3.
Default: 0x80 = 128 (mid-range)

3.2.39 Register Name: CH3_COARSE — Subaddress: 2C (R/W)

MSB							LSB
X	X	CH3_COARSE5	CH3_COARSE4	CH3_COARSE3	CH3_COARSE2	CH3_COARSE1	CH3_COARSE0

CH3_COARSE[5..0]

Coarse PGA value for Channel 3.
Default: 0x20 = 32 (mid-range)

3.2.40 Register Name: CH3_FINE — Subaddress: 2D (R/W)

MSB							LSB
X	X	X	CH3_FINE4	CH3_FINE3	CH3_FINE2	CH3_FINE1	CH3_FINE0

CH3_FINE[4..0]

Fine PGA value for Channel 3.
Default: 0x10 = 16 (mid-range)

3.2.41 Register Name: PIX_TRAP_0 — Subaddress: 2E (R/W)

MSB							LSB
PIX_TRAP7	PIX_TRAP6	PIX_TRAP5	PIX_TRAP4	PIX_TRAP3	PIX_TRAP2	PIX_TRAP1	PIX_TRAP0

PIX_TRAP[7..0]

PIX_TRAP[10..0] sets the pixel count value in a line to be sampled. Each <PIX_TRAP>th value on each line will be stored into the CH<n>_RDBK registers

Default: 0x04

3.2.42 Register Name: PIX_TRAP_1 — Subaddress: 2F (R/W)

MSB							LSB
X	X	X	X	PIX_TRAP11	PIX_TRAP10	PIX_TRAP9	PIX_TRAP8

PIX_TRAP[11..8]:

See register PIX_TRAP_0
Default: 0x00

3.2.43 Register Name: PWDN_CTRL — Subaddress: 30 (R/W)

MSB							LSB
X	X	X	PWDN_ALL	X	PWDN_REF	PWDN_BGAP	DTO_DIS

PWDN_ALL

Powers down complete chip excluding I^2C, clamping and composite sync slicer. Enables green mode for monitor standby.

0 = active (default)
1 = powered down

PWDN_REF

Powers down internal top and bottom references for all channels (VREFT / VREFB). If powered down, enables user to supply external VREFT / VREFB references on corresponding pins.

0 = active (default)
1 = powered down

PWDN_BGAP

Powers down bandgap reference. If powered down, enables user to supply external VMID (input common mode voltage) on corresponding pin.

0 = active (default)
1 = powered down

DTO_DIS

Disables the DTO. Can be disabled when an external clock (EXT_ADCCLK) is used and the user does not intend to use the PLL output on DTOCLK3. When the PLL is active, it can be used as the clock source for the ADC channels or the ADC's can still run from EXT_ADCCLK depending on the SEL_ADCCLK register setting. Note that when the DTO is enabled and the device is configured to use an external clock, the DTO clock is still available on the DTOCLK3 pin so it can be used as a general-purpose clock synthesizer for other parts in the system, possibly the display clock if this is different from the input pixel clock.

Since the DTO is also used for internal clock generation, power should always be supplied to the PLL supply pins, even when the ADC sampling clock is fed from EXT_ADCCLK and DTO_DIS is active.

0 = active (default)
1 = powered down

3.2.44 Register Name: AUX_CTRL Subaddress: 31 (R/W)

MSB							LSB
X	X	X	CS_DIS	TEST2	TEST1	TEST0	TACT

CS_DIS

Enables/disables the composite sync output on terminal CS/TEST1. The state of the CS output is also dependent on the clamp range (see section Composite Sync Slicer in functional description).

0 = enabled (default)
1 = disabled

TEST[2..0]
TACT

This is for TI factory testing only and should not be changed from its default all 0 value.

3.2.45 Register Name: CH1_RDBK Subaddress: 32 (R)

MSB							LSB
CH1_RDBK7	CH1_RDBK6	CH1_RDBK5	CH1_RDBK4	CH1_RDBK3	CH1_RDBK2	CH1_RDBK1	CH1_RDBK0

CH1_RDBK[7..0]:

Readback register of ADC Channel 1.
Default: (changed during operation)

3.2.46 Register Name: CH2_RDBK — Subaddress: 33 (R)

MSB							LSB
CH2_RDBK7	CH2_RDBK6	CH2_RDBK5	CH2_RDBK4	CH2_RDBK3	CH2_RDBK2	CH2_RDBK1	CH2_RDBK0

CH2_RDBK[7..0]:

Readback register of ADC Channel 2.
Default: (changed during operation)

3.2.47 Register Name: CH3_RDBK — Subaddress: 34 (R)

MSB							LSB
CH3_RDBK7	CH3_RDBK6	CH3_RDBK5	CH3_RDBK4	CH3_RDBK3	CH3_RDBK2	CH3_RDBK1	CH3_RDBK0

CH3_RDBK[7..0]:

Readback register of ADC Channel 3.
Default: (changed during operation)

3.2.48 Register Name: OFM_CTRL — Subaddress: 40 (R/W)

MSB							LSB
X	X	X	X	DHS_MODE	DHS_POL	OFM_MODE1	OFM_MODE0

DHS_MODE

Controls how DHS (display horizontal sync output) is generated. DHS can be a version of the signal on the HS input terminal, synchronized to the sampling clock and compensated for the data pipeline delay through the part (see timing diagrams). This preserves the HS width but has the disadvantage that for some phase settings there will be a one-pixel uncertainty on the exact timing of DHS (if HS falls within setup/hold time of the input register that is clocked by the ADC sampling clock).

Therefore, a second option exist to generate DHS as the output pulse of the PLL feedback divider. Since this pulse is generated once for every <TERM_CNT> cycles of the DTO clock, the uncertainty is resolved. This can avoid possible horizontal line jitter on the display system. The width of the DHS pulse is in this case always 1 ADC clock cycle, independent of the width of the incoming HS. This method also assures the generation of a DHS pulse on every line, even when no incoming HS is present or when it is filtered out by sync processing (e.g., from composite sync extraction).

0 = DHS is generated from the output of the PLL feedback divider (default)
1 = DHS is generated as a latched and delayed version of HS input

DHS_POL

Controls polarity of the DHS output
0 = positive polarity (default)
1 = negative polarity

OFM_MODE[1..0]:

Defines mode of output formatter and frequency on DATACLK1 as in Table 3–2.

Table 3–2. Output Formatter

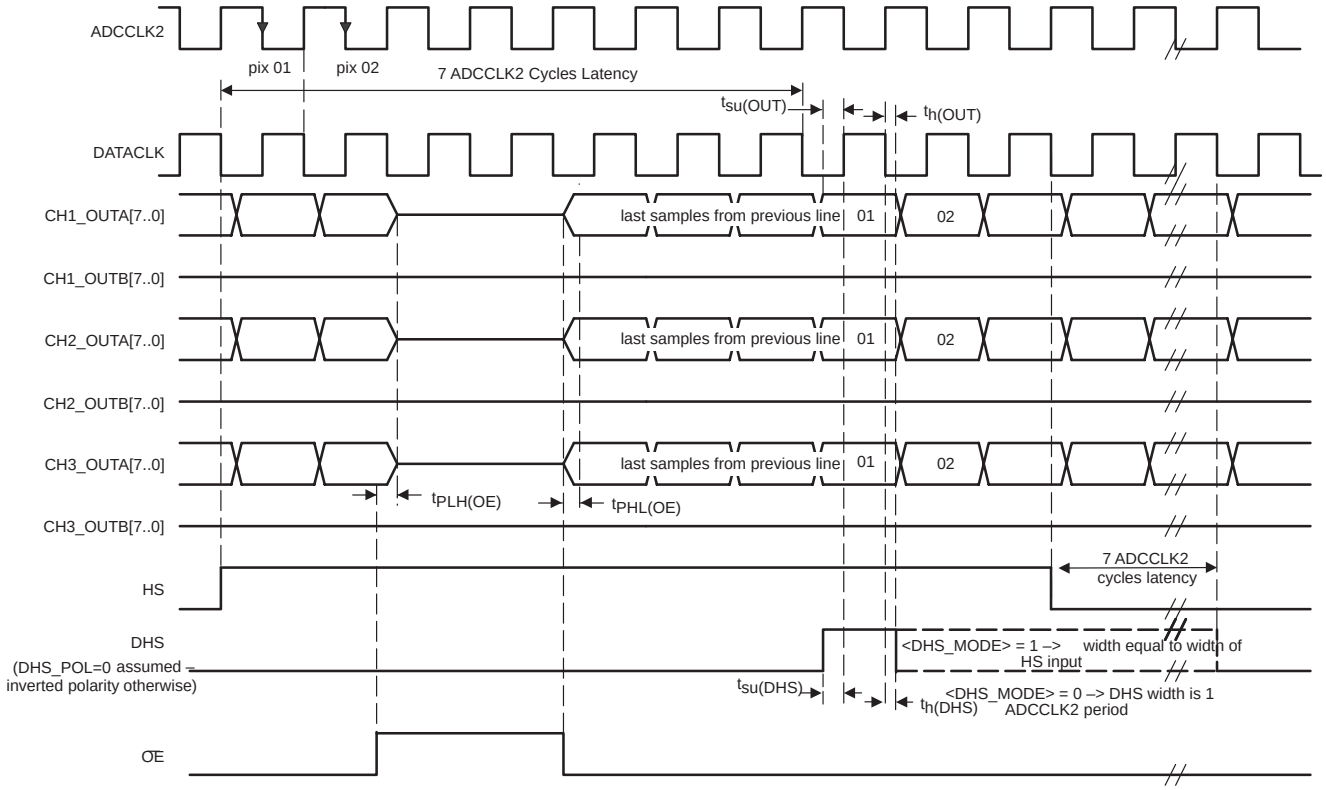
OFM_MODE [1..0]	DESCRIPTION	DATACLK1 OUTPUT FREQUENCY
00 (default)	24-bit parallel mode: 24-bit output on bus A, Bus B is Hi-Z	Fs
01	16-bit mode 16-bit output on ch1 and ch2 of bus A, with data from ch2 and ch3 downsampled by 2 (parallel 4:2:2 CCIR–601 mode), Bus B is Hi-Z	Fs
10	48-bit interleaved mode 48-bit output on buses A and B at half sampling rate. Data on bus B shifted by 1-Fs clock.	Fs/2
11	48-bit parallel mode 48-bit output on buses A and B at half sampling rate.	Fs/2

4 Parameter Measurement Information

All timing diagrams are shown for operation with internal PLL clock at phase 0, and ADCCLK2 non-inverted and non-divided-by-2.

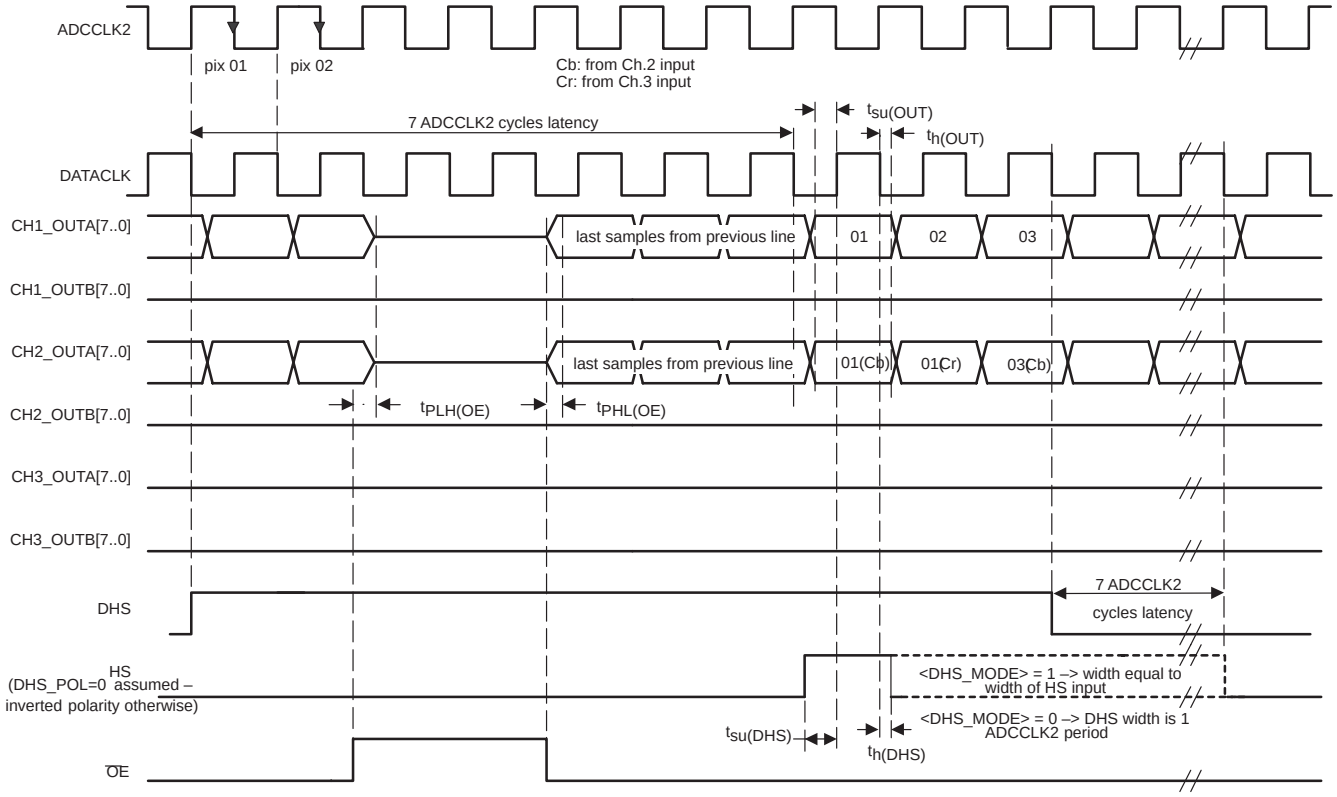
4.1 Timing Diagram – 24-Bit Parallel Mode

This mode outputs data on the three channels simultaneously in single-pixel mode. DATACLK1 is at the sampling clock frequency; output bus B remains high-impedance.



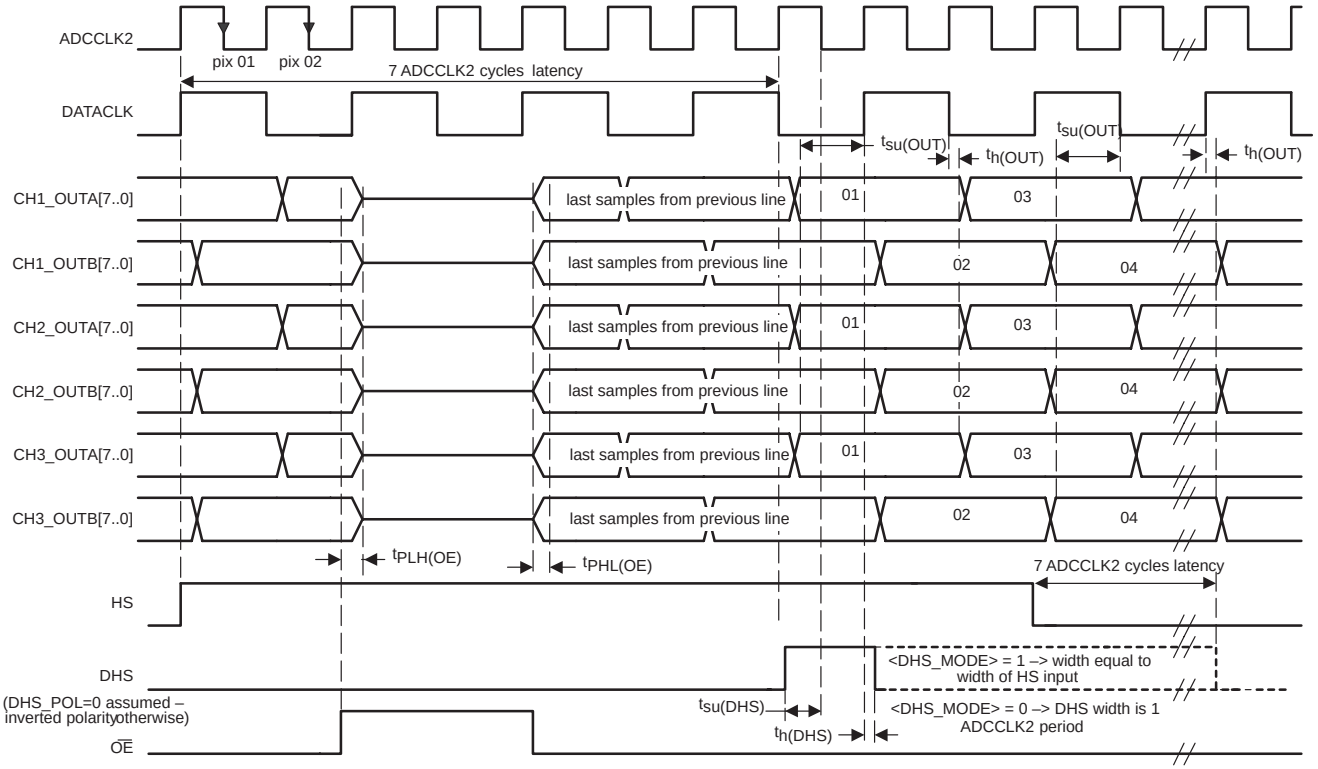
4.2 Timing Diagram – 16-Bit Parallel Mode

This is the ITU.BT–601 style mode that will typically be used in YUV operation of the part with a Y analog input connected to the Ch1 input of THS8083, Cb from Ch.2 input, and Cr from Ch.3 input. The DATACLK1 output is at the sampling clock frequency and Ch3 remains unused. Output bus B of all channels is high impedance. The DHS signal can be used to uniquely identify Cb from Cr output data.



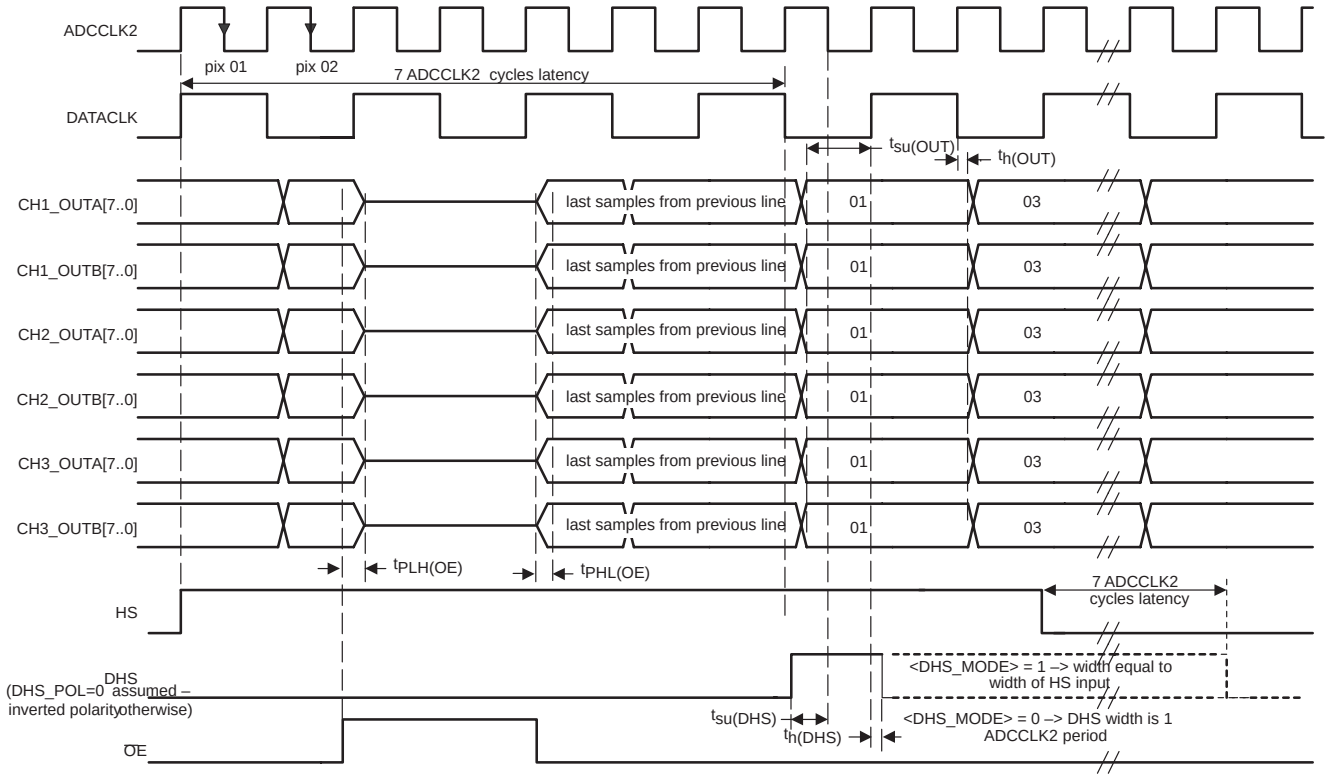
4.3 Timing Diagram – 48-Bit Interleaved Mode

This mode allows a double-pixel width output interface with a 1 sampling clock period time offset between buses A and B. The DATACLK1 output is at half of the sampling clock frequency.



4.4 Timing Diagram – 48-Bit Parallel Mode

This mode allows a double-pixel width output interface with no time offset between buses A and B. The DATACLK1 output is at half of the sampling clock frequency.



5 Electrical Specification

Electrical specifications over recommended operating conditions with Fs = 80 MSPS, (unless otherwise noted)

5.1 Definition of Test Conditions

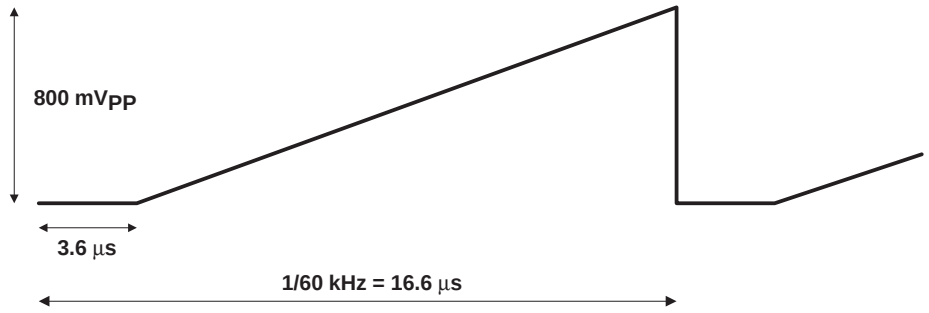


Figure 5–1. Input Test Waveform

Test condition **SYSTEM_INTREF** refers to:

- All supplies at 3.3 V
- XTL1_MCLK & XTL2 connected at 14.31818 MHz
- No power downs enabled
- XGA at 75-Hz operation mode, internal clock, clamping enabled, internal clamp timing, coarse and fine PGAs at midscale, bottom-level clamping, clamp code at midscale, 24-bit output mode
- Identical ac-coupled 0.8 Vpp ramp-shape input on all 3 channels at 60.0-kHz line rate, as shown in Figure 5-1
- Use of internal bandgap and voltage references

Test condition **PLL** refers to:

- SYSTEM_INTREF, with an input signal other than the ramp-shape input test waveform of Figure 5–1**.**

Test condition **ADC_INTREF** refers to:

- All supplies at 3.3 V
- Use of internal bandgap and voltage references
- Use of external ADCCLK (SEL_ADCCLK = 1) clock, driven at 81.92 MHz
- No power downs enabled
- Identical ac–coupled 0.8 Vpp ramp-shape input on all three channels at 60.0-kHz line rate, as shown in Figure 5-1

Test condition **ADC_EXTREF** refers to:

- ADC_INTREF, except: PWDN_BGAP = PWDN_REF = 1, VMID and VREFTO/BO driven from external at nominal levels

Test condition **ADC_PWDN** refers to:

- ADC_INTREF, except: PWDN_ALL = 1

5.2 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)

Supply voltage range: Analog supplies (see Note 1) to AGND,
Digital supplies (see Note 2) to DGND . . . . . –0.5 to 4.5 V
Analog supplies to digital supplies, AGND to DGND . . . . . –0.5 to 0.5 V
Digital input voltage range to DGND, V_I . . . . . –0.5 to DV_{DD} + 0.5 V
Analog input voltage range to AGND, V_I . . . . . –0.5 to AV_{DD} + 0.5 V
Bandgap reference to AGND (see Note 3) . . . . . –0.5 to AV_{DD} + 0.5 V
Reference voltage (VREFTO_CHx,VREFBO_CHx) input range to AGND, V_{ref}
(see Note 4) . . . . . –0.5 to AV_{DD} + 0.5 V
Operating free-air temperature range, T_A: THS8083CPZP and THS8083-95CPZP . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. AVDD_PLL, AVDD_REF, AVDD_CH1, AVDD_CH2_3
2. DVDD_PLL, DVDD
3. Only input in case PWDN_BGAP=1
4. Only input in case PWDN_REF=1

5.3 Recommended Operating Conditions Over Operating Free-Air Temperature Range, T_A = 0°C to 70°C (unless otherwise noted)

5.3.1 Power Supply

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, all supplies	3.15	3.3	3.6	V

5.3.2 Analog and Reference Inputs (see Note 5)

PARAMETER	MIN	NOM	MAX	UNIT
Reference input voltage (top), $V_{I(REFT)}$	1.88	1.9	1.92	V
Reference input voltage (bottom), $V_{I(REFB)}$	1.08	1.10	1.12	V
Analog input voltage (dc-coupled), $V_{I(AIN)}$	$V_{I(REFB)}$		$V_{I(REFT)}$	V
Analog input voltage range, V_I			1.2	V

NOTE 5: VREFTO_CHx and VREFBO_CHx can be inputs only when PWDN_REF=1.

5.3.3 Digital Inputs

PARAMETER		MIN	NOM	MAX	UNIT
High-level input voltage, V_{IH}		2.0		DVDD	V
Low-level input voltage, V_{IL}		DGND		0.2 x DVDD	V
Clock period, t_c	THS8083	12.5			ns
	THS8083-95	10.5			ns
Pulse duration, clock high, $t_{w(CLKH)}$	THS8083	5.25			ns
	THS8083-95	TBD			ns
Pulse duration, clock low, $t_{w(CLKL)}$	THS8083	5.25			ns
	THS8083-95	TBD			ns

5.4 Electrical Characteristics Over Recommended Operating Free-Air Temperature Range, T_A = 0°C to 70°C (unless otherwise noted)

NOTE: In order to reach stated performance levels, the device's PowerPad feature should be thermally and electrically connected to the pcb ground plane, as described in section 6.1 *Designing With PowerPad™*.

5.4.1 Power Supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analog supply (=AVDD_CH1+AVDD_CH2_3+AVDD_PLL+AVDD_REF)	ADC_INTREF	T_A = 25°C		275	320	mA
					340	
Digital supply (=DVDD+DVDD_PLL)	ADC_INTREF	T_A = 25°C		110	120	mA
					125	
Total power dissipation normal operation	ADC_INTREF	T_A = 25°C		1.28	1.35	W
					1.48	
Total power dissipation, power down all modes	ADC_PWDN	T_A = 25°C		255	270	mW
					290	

5.4.2 Digital Logic Inputs (HS, VS, SCL, SDA, I2CA, XTL1_MCLK, EXT_ADCCLK, $\overline{OE}$, $\overline{RESET}$, EXT_CLP)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	DVDD = 3.6 V, Digital inputs and CLK at 0 V for I_{IL}; Digital inputs and CLK at 3.6 V for I_{IH}	–10		10	µA
I_{IL}	Low-level input current		–10		10	µA
$I_{IL(CLK)}$	Low-level input current, CLK (see Note 6)		–14		17	µA
$I_{IH(CLK)}$	High-level input current , CLK (see Note 6)		–14		17	µA
C_I	Input capacitance			5		pF

NOTE 6: Applies to when XTL1_MCLK is driven by the clock signal directly.

5.4.3 Logic Outputs (SDA, CHn_OUTA[7..0], CHn_OUTB[7..0], DTOCLK3, ADCCLK2, DATACLK1, DHS, LOCK)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	DVDD = 3 V at I_{OH} = 50 µA, Digital output forced high	2.9			V
V_{OL}	Low-level output voltage	DVDD = 3.6 V at I_{OL} = 50 µA, Digital output forced low			0.15	V
C_O	Output capacitance			5		pF
$I_{OZ(H)}/I_{OZ(L)}$†	High-impedance state output current	DVDD = 3.6 V Worst-case for V_O = 3.6 V and V_O = 0 V	–10		10	µA

† Tested for CHn-OUTA[7..0] and CHn_OUTB[7..0] only

5.4.4 I²C Interface

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage				0.99	V
V_{IH}	High-level input voltage		2.31			V
$f_{(SCL)}$	SCL clock frequency		0		400†/100‡	kHz
$t_{(LOW)}$	Low period of SCL	Valid for I²C fast mode support only. See footnotes to SCL clock frequency.	1.3			µs
$t_{(HIGH)}$	High period of SCL		0.6			µs
$t_{h(DATA)}$	Data hold time		0§			µs
$t_{su(DATA)}$	Data setup time		100¶			µs
$C_{(b)}$	Capacitive load for each bus line#				400	pF

† For DTO clock frequencies of minimum 25 MHz (I²C fast mode)
‡ For DTO clock frequencies of below 25 MHz (I²C normal mode)
§ The device must internally provide a hold time of 300 ns for the SDA signal (referred to $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
¶ If the device is used in a standard mode I²C system the requirement of $t_{su(DATA)}$>=250 ns must be met.
# C_b= total capacitance of one bus line in pF

5.4.5 ADC Channel

5.4.5.1 DC Accuracy†

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Integral nonlinearity (INL)	PLL (see Note 7)	T_A = 25°C	–2	±1.25	2	LSB
			–2.5		–2.5	
Differential nonlinearity (DNL)	PLL (see Note 8)	T_A = 25°C	–1	–0.6/1	1.5	LSB
			–1		1.75	
No missing codes					Assured	
Gain error	ADC_INTREF (see Note 9)			20		mV
Offset error	ADC_INTREF (see Note 10)			–20		mV

† Guaranteed at nominal voltage supply levels only.

NOTES: 7. Integral nonlinearity (INL) – Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.

8. Differential nonlinearity (DNL) – An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test (i.e., last transition level – first transition level)/(2^n – 2). Using this definition for DNL separates the effects of gain and offset error. A DNL of less than ±1 LSB ensures no missing codes.
A DNL of less than ±1/2 LSB assures monotonic behavior.

9. Gain error – The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale (the voltage applied to the REFBI terminal). The last transition should occur for an analog value 1/2 LSB below nominal positive full scale (the voltage applied to the REFTI terminal). Gain error is defined here as the deviation from the ideal location of the highest transition level on the ADC transfer function.

10. Offset error – The first code transition should occur at a level 1/2 LSB above zero. Offset is defined as the deviation of the actual first code transition from that point.

5.4.5.2 Dynamic Performance†

PARAMETER	TEST CONDITIONS ADC_INTREF	MIN	TYP	MAX	UNIT
Effective number of bits, ENOB	f_I = 20 MHz		6.4		Bits
Signal-to-total ratio without distortion, SNR	f_I = 20 MHz		40.5		dB
Total harmonic distortion, THD	f_I = 1 MHz		–43.5		dB
Spurious free dynamic range, SFDR	f_I = 1 MHz		49		dB
Analog input full-power bandwidth, BW	(see Note 11)		500		MHz

† Based on analog input voltage of 1 dB FS referenced to the full-scale input range and a clock signal with 50% duty cycle.

NOTE 11: Analog input bandwidth – The analog input bandwidth is defined as the maximum frequency of the input sine that can be applied to the device for which a 3 dB attenuation is observed in the reconstructed signal.

5.4.5.3 Clamp

PARAMETER	TEST CONDITIONS ADC_INTREF		MIN	TYP	MAX	UNIT
Clamp code adjustment range	See Note 12	T_A = 25°C	110		133	LSB
			105		133	
Clamp acquisition time at input dc level change	Input level changed by 100 mV	Within 10% of final value		1	1.8	ms
		Within 1 LSB of final value		2.1	3.6	ms
Clamp acquisition time, clamp code change	Clamp changed from min to max	Within 1 LSB		400	700	ns
Clamp droop error	Droop between 2 clamps at 15 kHz line rate	T_A = 25°C		0.35	1.1	LSB
				0.35	1.2	

NOTE 12: Clamp code adjustment range – A dc-input signal is applied to the device. The clamp code is changed from the minimum to maximum setting. The corresponding change in the ADC output code is defined as the clamp code adjustment range.

5.4.6 Coarse PGA

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full-scale adjustment range		0.4		1.2	V
Accuracy		± 6			LSB
Full-scale gain change settling time				285	ns

5.4.7 Fine PGA

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full-scale adjustment range		–4		8	LSB

5.4.8 Output Formatter/Timing Requirements

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Maximum conversion rate	THS8083		80			MHz
		THS8083-95		95			
f_{clk}	Minimum conversion rate					10	MHz
$t_{su(OUT)}$	Setup time		With respect to 50% level of rising edge on DATACLK	3			ns
$t_{h(OUT)}$, $t_{h(DHS)}$	Hold time			1			ns
$t_{su(DHS)}$	Setup time			4			ns
$t_{PLH(OE)}$	Propagation (delay) time, low-to-high		See Note 13			8.5	ns
$t_{PHL(OE)}$	Propagation (delay) time, high-to-low-level output					8	
	DATACLK1 output duty cycle			40%		58%	
	HS and data pipeline delay		See Note 14	See timing diagrams			

NOTES: 13. Output timing – OE timing $t_{PLH(OE)}$ is measured from the $V_{IH(MIN)}$ level of OE to the high-impedance state of the output data. The digital output load is not higher than 10 pF.
OE timing $t_{PHL(OE)}$ is measured from the $V_{IL(MAX)}$ level of OE to the instant when the output data reaches $V_{OH(min)}$ or $V_{OL(max)}$ output levels. The digital output load is not higher than 10 pF.

14. Pipeline delay (latency) – The number of clock cycles between conversion initiation on an input sample and the corresponding output data being made available. Once the data pipeline is full, new valid output data are provided every clock cycle.

5.4.9 PLL

5.4.9.1 Open Loop

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DTO frequency range, $f_{(DTO)}$	THS8083CPHP	See Note 15		10		80	MHz
	THS8083-95CPHP			10		95	
Instantaneous jitter, $t_{(INS)}$					260 (p-p)		ps
Short-term jitter, $t_{(JOS)}$					525 (p-p) 150 (rms)		ps
			T_A = 25°C			900 (p-p) 360 (rms)	ps
Phase Increment					11.25 Monotonic		deg

NOTE 15: PLL characterization:

- Instantaneous jitter is the pk-pk variation of position of clock rising edge between succeeding periods.
- Short term jitter in open loop or closed loop is defined as the variation within one PLL update period (= within the same video line) of the clock rising edge. This can be measured visually by capturing the clock and displaying it on a digital scope with a persistency of one video line. Numerically the time instants of the rising edges, at a defined voltage level, of a number N of clock cycles (N = 800) are captured at high sampling rate. From these time instants, the average clock time period is calculated. The deviation between each actual time instant and the ideal, based on the average clock time period, is defined as a statistically distributed jitter value along one line. This jitter is measured on both DATACLK1 and DTOCLK3 outputs.

5.4.9.2 Closed Loop

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(HS)}$	HS locking range	See Note 16		15		100	kHz
$t_{(acq)}$	Lock-in time				5	12	ms
$t_{(JCS)}$	Short-term jitter				700 (p-p) 185 (rms)		ps
			T_A = 25°C			1250 (p-p) 440 (rms)	ps
$t_{(JCL)}$	Long-term jitter	See Note 16			700 (pk-pk) 185 (rms)		ps
			T_A = 25°C			1250 (p-p) 440 (rms)	ps

NOTE 16: PLL characterization:

- Short term jitter in open loop or closed loop is defined as the variation within one PLL update period (= within the same video line) of the clock rising edge. This is measured visually by capturing the clock and displaying it on a digital scope with a persistency of one video line. Numerically the time instants of the rising edges, at a defined voltage level, of a number of clock cycles (N = 800) are captured at high sampling rate. From these time instants, the average clock time period is calculated. The deviation between each actual time instant and the ideal, based on the average clock time period, is defined as a statistically distributed jitter value along one line. This jitter is measured on both DATACLK1 and DTOCLK3 outputs.
- Long term jitter in closed loop is defined as the variation over one video frame of the Nth clock rising edge on each line. This is measured by capturing the time instant that a defined level on the rising edge of the Nth clock after HS is reached on each line. The same principle for calculation is used as for short term jitter but now for one sample taken on every line and N = 800 lines.

5.4.10 Typical Plots (25°C and Measured for Standard VESA Graphics Formats)

Note: The THS8083 is configured for each video mode with I^2C register settings as specified in application note *Using THS8083 for PC Graphics and Component Video Digitizing*.

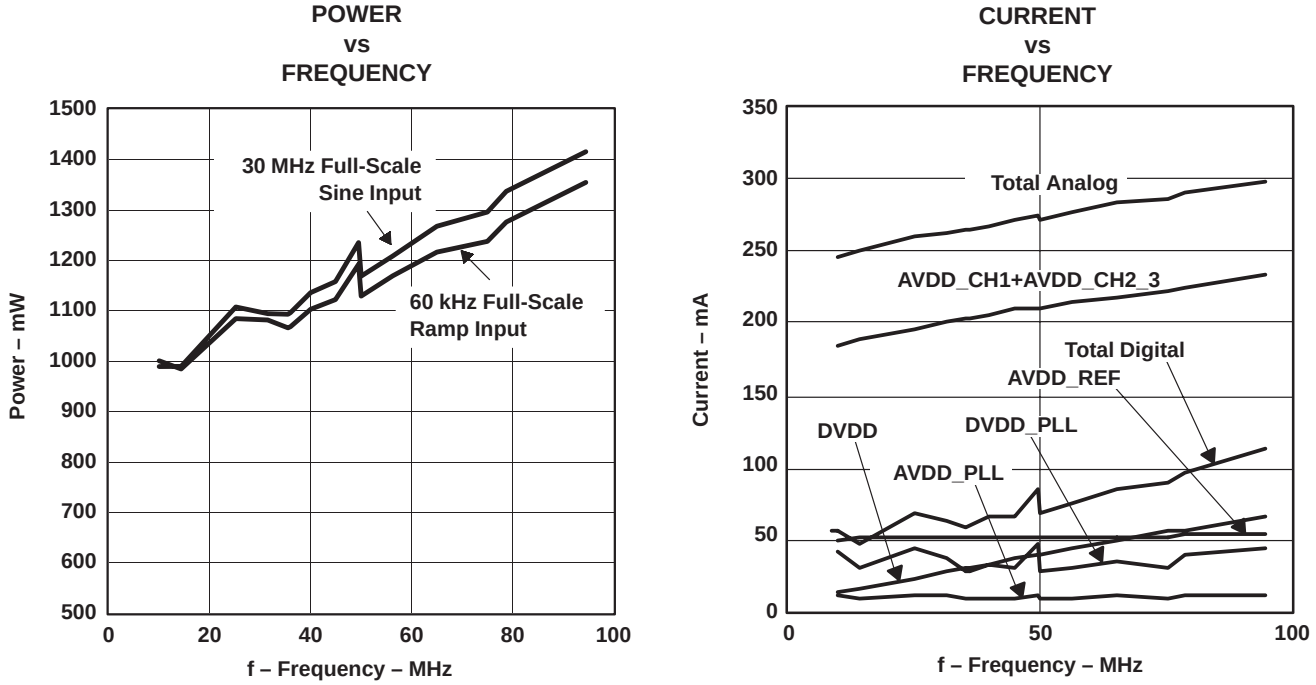


Figure 5–2. Power Consumption

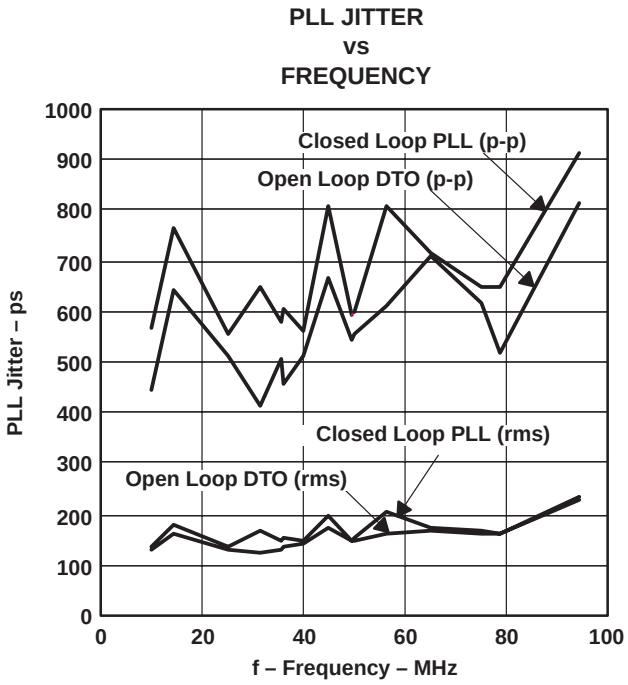


Figure 5–3. PLL Jitter

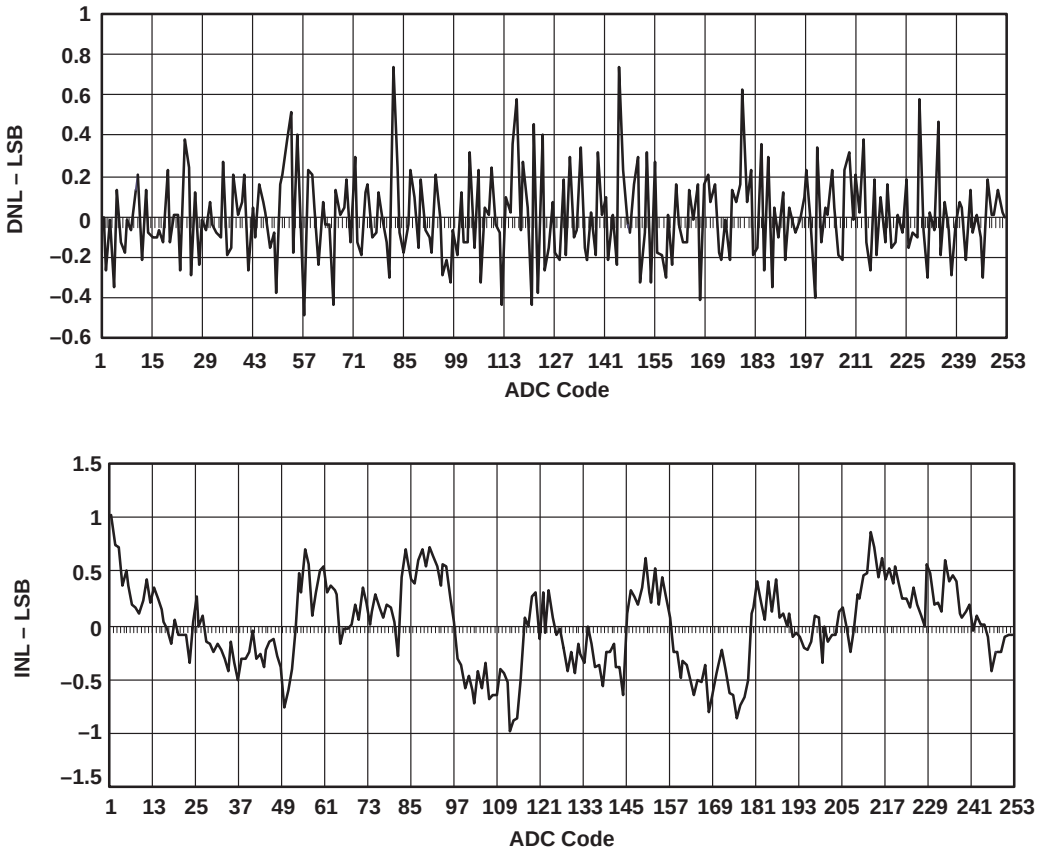


Figure 5–4. Linearity of AGY Channel at 80 MSPS (external clock)

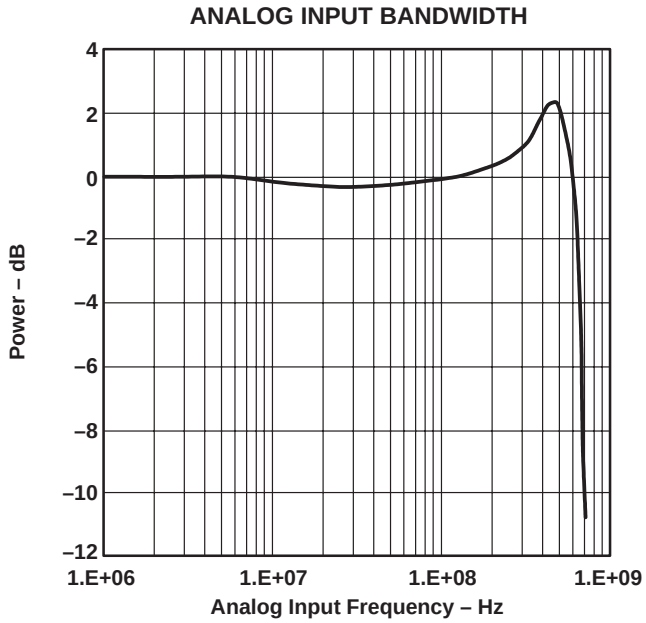


Figure 5–5. Analog Input Bandwidth

6 Application Information

6.1 Designing With PowerPAD™

The THS8083 is housed in a high-performance, thermally enhanced, 100-pin PowerPAD™ package (TI package designator: 100PZP). Use of the PowerPAD™ package does not require any special considerations except to note that the PowerPAD™, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing the PowerPAD™ PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD™ of connection etches or vias under the package. The recommended option, however, is not to run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keepout area for the 100-pin PZP PowerPAD™ package is 5 mm $\times$ 5 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD™ package. The thermal land will vary in size, depending on the PowerPAD™ package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

More information on this package and other requirements for using thermal lands and thermal vias are detailed in the TI application note *PowerPAD™ Thermally Enhanced Package Application Report*, TI literature number SLMA002, available via the TI Web pages beginning at URL: http://www.ti.com

For the THS8083, this thermal land should be grounded to the low impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal terminals. The thermal land may be soldered to the exposed PowerPAD™ using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device.

Table 6-1 lists a comparison for thermal resistances between the PowerPAD™ package (100PZP) used for this device and a regular 100-pin TQFP package.

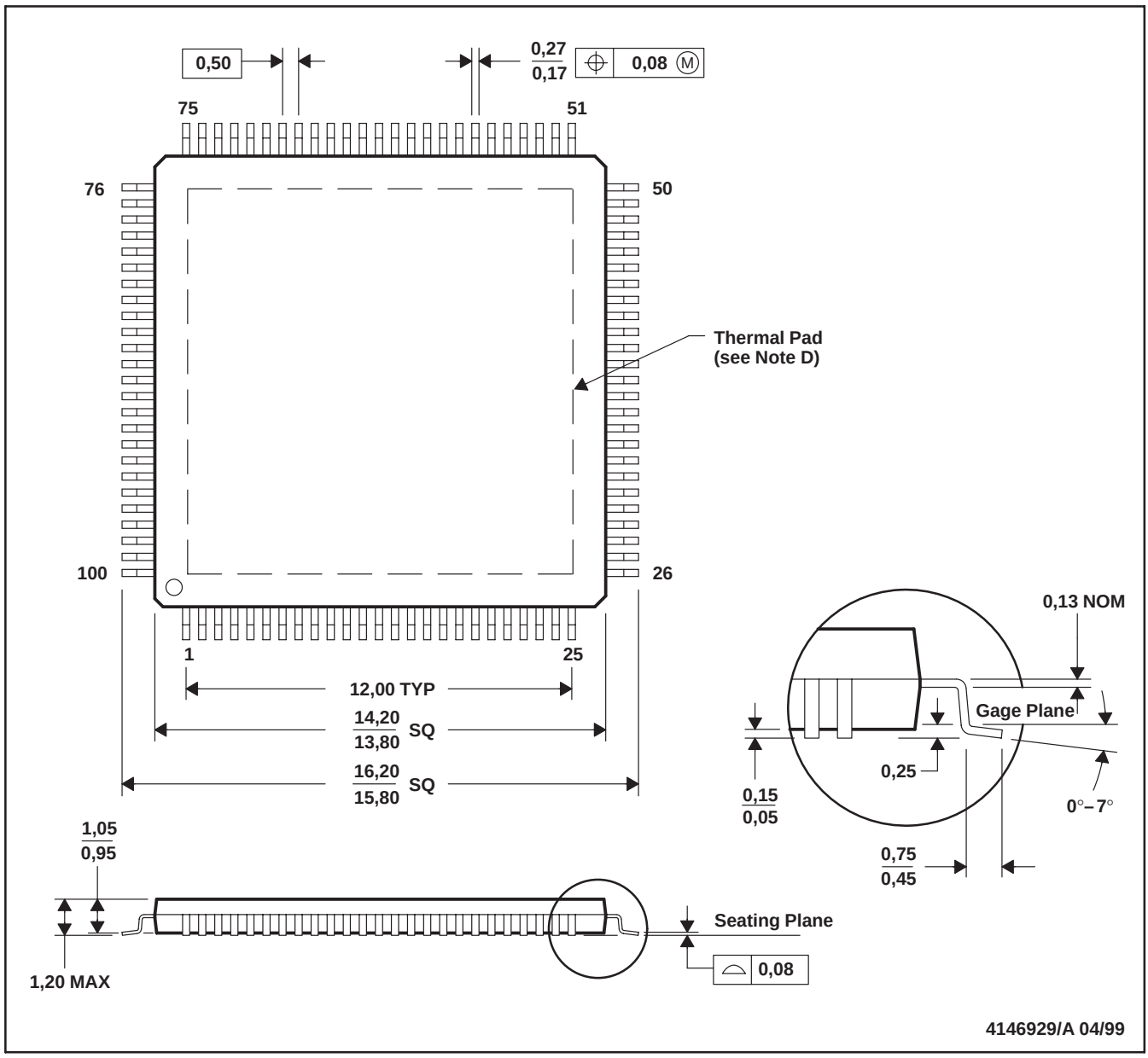
Table 6–1. Junction-Ambient and Junction-Case Thermal Resistances

100 PZP PowerPAD™ vs 100 PIN REGULAR TQFP	AIRFLOW IN lfm			
	0	150	250	500
θ_{JA} (°C/W) 100 PZP	17.3	11.8	10.4	9.0
θ_{JC} (°C/W) 100 PZP	0.12			
θ_{JA} (°C/W) 100 pin regular	49			
θ_{JC} (°C/W) 100 pin regular	3			

PowerPAD is a trademark of Texas Instruments.

7 Mechanical Data

PZP (S-PQFP-G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

Appendix A
PLL Formula and Register Settings

If:

F(XTL) = frequency of external crystal or master clock connected to XTL1 input of THS8083
F(VCO) = frequency of THS8083–internal VCO
F(DTO) = frequency of THS8083–internal DTO
F(DTOCLK) = frequency of externally available DTO clock output
F(HS) = frequency of HS input
CLKDIV = clock output divider setting
VCODIV = feedback divider in THS8083–internal analog PLL loop
TERMCNT = feedback divider in THS8083–internal digital PLL loop
DTO_INC = DTO increment (when NOM_INC is programmed, DTO_INC is initialized to NOM_INC)

Then:

F(VCO) = F(XTL) x VCODIV
F(DTO) = 31 x F(VCO) / DTO_INC
F(DTOCLK) = F(DTO) / CLKDIV
AND, if PLL is locked:
F(DTOCLK) = TERMCNT * F(HS)

Summarizing:

DTO_INC = [31xF(XTL)xVCODIV] / [F(DTOCLK)xCLKDIV]

The formats of DTO_INC and NOM_INC:

Both are 33 bit values, consisting of a 6-bit integer and a 27-bit fractional part. So, in hexadecimal notation, the value is between 00.0000000hex and 3F.7FFFFFFhex. The decimal value of the increment is: <integer part>.<fractional part interpreted as integer value>x2^(–27).

Due to the architecture of the DTO, to all increment values with an integer part higher than 31, 1 needs to be added when programming the register.

For example:

Actual increment	–>	Programmed increment
30.0	–>	30.0
31.0	–>	31.0
32.0	–>	33.0

Additional restrictions:

– CLKDIV should be chosen such that the programmed increment NOM_INC falls within the range [28.62]

Examples:

1. For generating the XGA@75Hz pixel clock of 78.75 MHz, with F(XTL) = 14.31818 MHz & VCODIV=8:
   NOM_INC = [31x14.31818x8]/[78.75x1] = 45.090802

Since this is higher than 31, the programmed value needs to be 46.090802. Converting this to the 6bit.27bit notation, gives us 2E.0B9F645.

To achieve lock with an incoming HS, TERMCNT is programmed with 1312 (i.e., the total number of pixels per line in this mode).

2. For generating a 13.5-MHz pixel clock for TV signals, with F(XTL) = 14.31818 MHz and VCODIV = 8; NOM_INC = [31x14.31818x8]/[13.5x1] = 263.0303

NOM_INC falls outside the range of the [28..62] allowable increment range. If CLKDIV is chosen 8 instead of 1, then NOM_INC = 32.87878...which is within the allowable range. Since the integer value is >31, the programmed increment NOM_INC becomes 33.87878...

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.