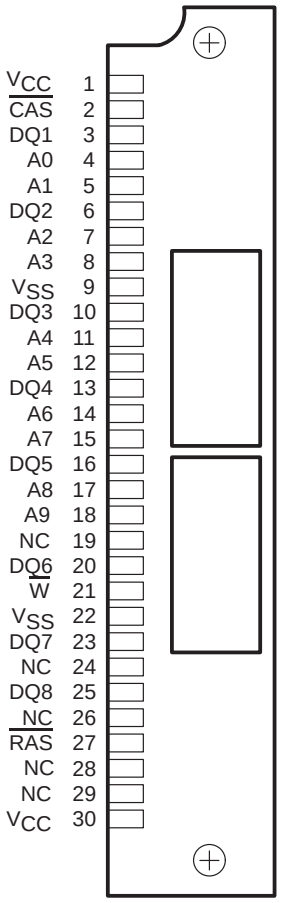
SMMS181A–JANUARY 1991–REVISED JANUARY 1993

- **Organization . . . 1 048 576 × 8**
- **Single 5-V Power Supply (±10% Tolerance)**
- **30-Pin Single In-Line Memory Module (SIMM)**
- **TM124GU8A Utilizes Two 4-Megabit Dynamic RAMs in Plastic Small-Outline J-Lead Packages (SOJs)**
- **Long Refresh Period . . . 16 ms (1024 Cycles)**
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Outputs**
- **Performance Ranges:**

	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
TM124GU8A-60	60 ns	30 ns	110 ns
TM124GU8A-70	70 ns	35 ns	130 ns
TM124GU8A-80	80 ns	40 ns	150 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range 0°C to 70°C**

SINGLE IN-LINE MODULE (TOP VIEW)



PIN NOMENCLATURE

A0–A9	Address Inputs
CAS	Column-Address Strobe
DQ1–DQ8	Data In/Data Out
NC	No Internal Connect
RAS	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TM124GU8A is a dynamic random-access memory module organized as 1 048 576 × 8 in a 30-pin leadless single in-line memory module (SIMM).

The TM124GU8A is composed of two TMS44400, 1 048 576 × 4 bit dynamic RAMs in 20/26-lead plastic small-outline J-lead packages (SOJs).

The TM124GU8A is mounted on a substrate with decoupling capacitors. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

The TM124GU8A features $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM124GU8A is characterized for operation from 0°C to 70°C.

operation

The TM124GU8A operates as two TMS44400s connected as shown in the functional block diagram. The common I/O features of the TM124GU8A dictates the use of early write cycles to prevent contention on the DQ lines.

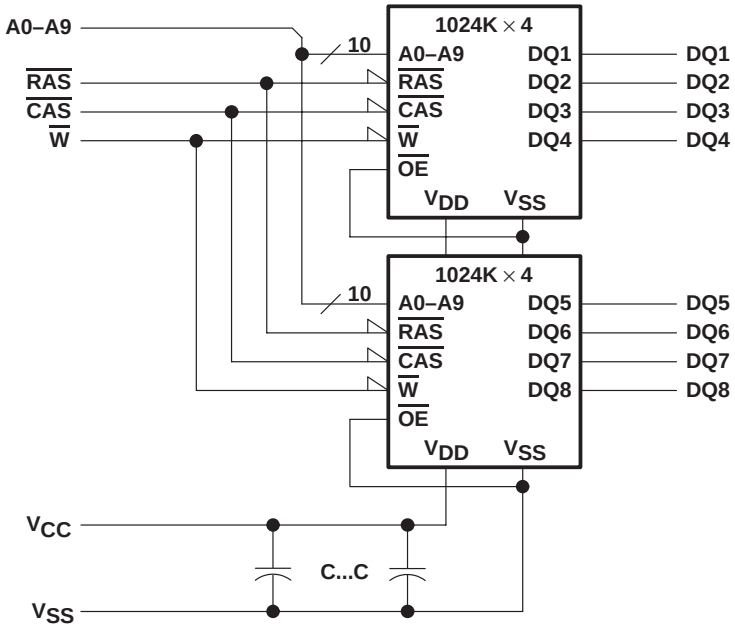
specifications

Refresh period is extended to 16 milliseconds and, during this period, each of the 1024 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

single in-line memory module and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness on contact area
Bypass capacitors: Multilayer ceramic
Contact area for socketable devices: Nickel plate and solder plate over copper

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Voltage range on V_{CC} . . . . . – 1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 2 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM124GU8A-60		TM124GU8A-70		TM124GU8A-80		UINT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read or write cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		210		180		160	mA
I_{CC2}	Standby Current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		4		4		4	mA
		After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		2		2		2	mA
I_{CC3}	Average refresh current (see Note 3)	Minimum cycle, V_{CC}= 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		210		180		160	mA
I_{CC4}	Average page current (see Note 4)	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		180		160		140	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		10	pF
$C_{i(DQ)}$	Input capacitance, data inputs/outputs		7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		14	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		14	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TM124GU8A-60		TM124GU8A-70		TM124GU8A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 5)	0	15	0	18	0	20	ns

NOTE 5: t_{OFF} is specified when the otuput is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		TM124GU8A-60		TM124GU8A-70		TM124GU8A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 6)	110		130		150		ns
t_{PC}	Page-mode read or write cycle time (see Note 7)	40		45		50		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$ low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$ low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$ low setup time before $\overline{CAS}$ low	0		0		0		ns
t_{WSR}	$\overline{W}$ high setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTS}	$\overline{W}$ low setup time (test mode only)	10		10		10		ns
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low (see Note 8)	50		55		60		ns
t_{DH}	Data hold time	10		15		15		ns
t_{AR}	Column-address hold time after $\overline{RAS}$ low (see Note 8)	50		55		60		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 8)	50		55		60		ns
t_{WHR}	$\overline{W}$ high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{WTH}	$\overline{W}$ low hold time (test mode only)	10		10		10		ns

Continued next page.

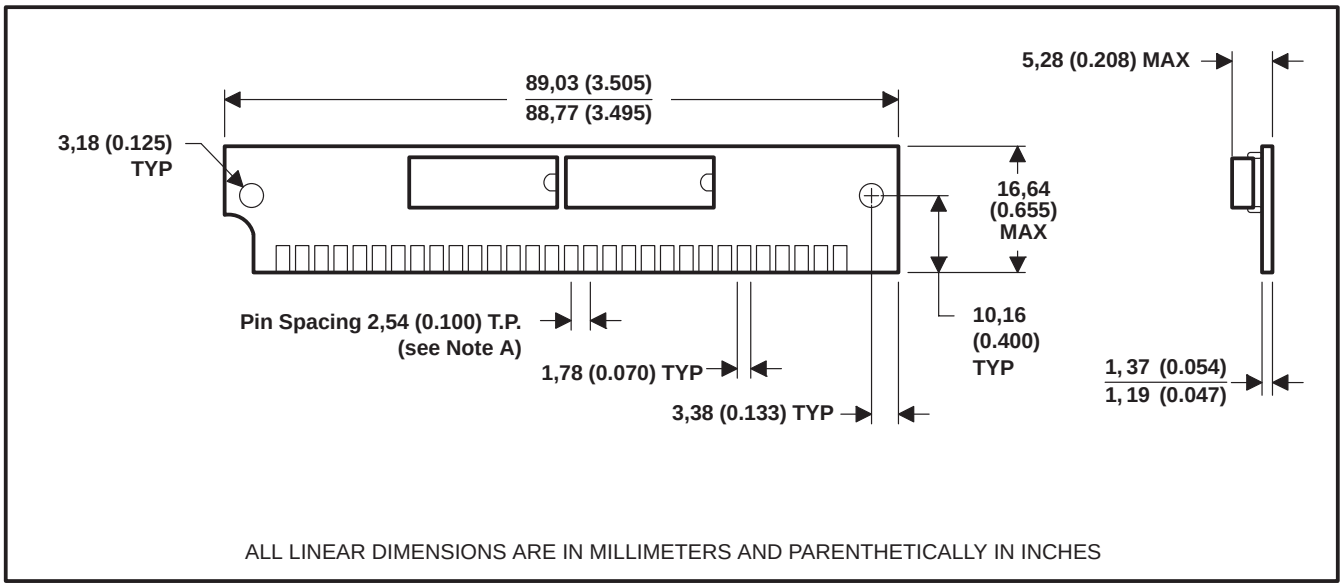
NOTES: 6. All cycle times assume t_T = 5 ns.
7. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns.
8. The minimum value is measured when t_{RCD} is set to t_{RCD} min as a reference.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

		TM124GU8A-60		TM124GU8A-70		TM124GU8A-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	15		15		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	0		0		0		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column-address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{TAA}	Access time from address (test mode)	35		40		45		ns
t_{TCPA}	Access time from column precharge (test mode)	40		45		50		ns
t_{TRAC}	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	50	2	50	2	50	ns

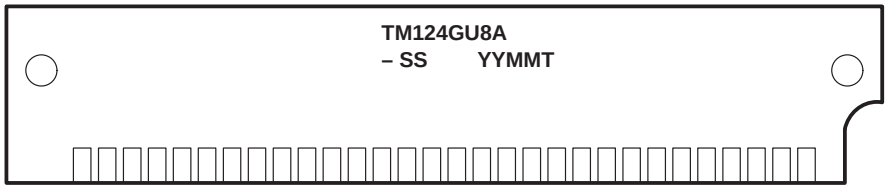
NOTE 10: The maximum value is specified only to assure access time.

30-pin U-A single in-line memory module



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

device symbolization



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed

NOTE: The location of the part number may vary.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.