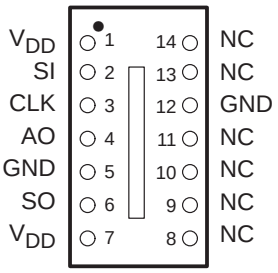
- **On-Board 64-Bit Static Shift Register**
- **Extendable Data I/O for Expanding the Number of Sensors**
- **Analog Buffer With Sample and Hold for Analog Output Over Full Clock Period**
- **Single-Supply Operation**
- **500-kHz Shift Clock**
- **14-Pin Clear Plastic Package**
- **Advanced LinCMOS™ Technology**

(TOP VIEW)



NC – No internal connection

description

The TSL214 integrated opto sensor consists of 64 charge-mode pixels arranged in a 64 × 1 linear array. Each pixel measures 120 µm × 70 µm, with 125-µm center-to-center spacing. Operation is simplified by internal logic requiring only clock and start-integration-pulse signals.

The TSL214 is intended for use in a wide variety of applications including linear and rotary encoding, bar-code reading, edge detection and positioning, and contact imaging.

The TSL214 is supplied in a 14-pin dual-in-line clear plastic package.

Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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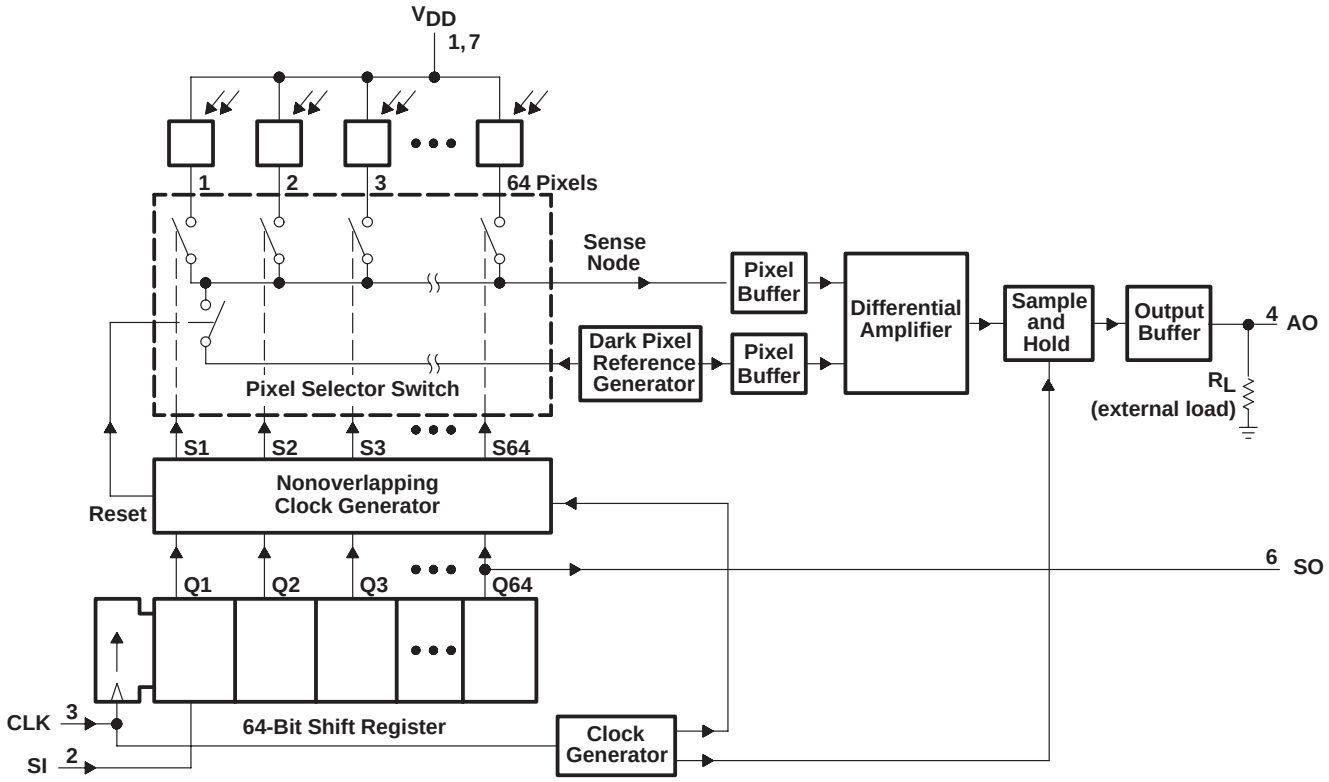
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO	4	Analog output
CLK	3	Clock input. CLK controls charge transfer, pixel output, and reset.
GND	5, 12	Ground (substrate). All voltages are referenced to the substrate.
NC	8–11, 13, 14	No internal connection
SI	2	Serial input. SI defines the end of the integration period and initiates the pixel output sequence.
SO	6	Serial output. SO provides a signal to drive the SI input of another TSL214 sensor for cascading.
V_{DD}	1, 7	Supply voltage. V_{DD} supplies power to the analog and digital circuits.

detailed description

sensor elements

The line of sensor elements, called pixels, consists of 64 discrete photosensing areas. Light energy striking a pixel generates electron-hole pairs in the region under the pixel. The field generated by the bias on the pixel causes the electrons to collect in the element while the holes are swept into the substrate. The amount of charge accumulated in each element is directly proportional to the amount of incident light and the integration time.

device operation

Operation of the 64 × 1 array sensor consists of two time periods: an integration period during which charge is accumulated in the pixels and an output period during which signals are transferred to the output. The integration period is defined by the interval between serial-input (SI) pulses and includes the output period (see Figure 1). The required length of the integration period depends upon the amount of incident light and the desired output signal level.

sense node

On completion of the integration period, the charge contained in each pixel is transferred in turn to the sense node under the control of the clock (CLK) and SI signals. The signal voltage generated at this node is directly proportional to the amount of charge and inversely proportional to the capacitance of the sense node.

reset

An internal reset signal is generated by the nonoverlapping clock generator (NOCG) and occurs every clock cycle. Reset establishes a known voltage on the sense node in preparation for the next charge transfer. This voltage is used as a reference level for the differential signal amplifier.

shift register

The 64-bit shift register controls the transfer of charge from the pixels to the output stages and provides timing signals for the NOCG. The SI signal provides the input to the shift register and is shifted under direct control of the clock. The input is shifted out to the serial output (SO) on the 64th clock cycle. This SO pulse can then be used as the SI pulse for another device for multiple-unit operation.

The output period is initiated by the presence of the SI pulse coincident with a rising edge of the clock (Figures 1 and 2). The output voltage corresponds to the level of the first pixel after settling time (t_S) and remains constant for a valid time (t_V). A voltage corresponding to each succeeding pixel is available at each rising edge of the clock. The output period ends on the rising edge of the 65th clock cycle, at which time the output assumes a high-impedance state. The 65th clock cycle terminates the output of the last pixel and clears the shift register in preparation for the next SI pulse. To achieve minimum integration time, the SI pulse may be present on the 66th rising edge of the clock to immediately reinitiate the output phase. Once the output period is initiated by an SI pulse, the clock must be allowed to complete 65 positive-going transitions in order to reset the internal logic to a known state.

sample-and-hold

The sample-and-hold signal generated by the NOCG is used to hold analog output voltage of each pixel constant until the next pixel is clocked out. The signal is sampled while the clock is high and held constant while the clock is low.

nonoverlapping clock generators

The NOCG circuitry provides internal control signals for the sensor, including reset and pixel-charge sensing. The signals are synchronous and are controlled by the outputs of the shift register.

initialization

Initialization of the sensor elements may be necessary on power up or during operation after any period of clock or SI inactivity exceeding the integration time. The initialization phase consists of 12 to 15 consecutively performed output cycles and clears the pixels of any charge that may have accumulated during the inactive period.

multiple unit operation

Multiple sensor devices may be connected together in a serial or parallel configuration. The serial connection is accomplished by connecting analog outputs (AO) together and connecting the SO terminal of each sensor device to the SI terminal of the next device. The SI signal is applied to the first device only, with each succeeding device receiving its SI from the SO of the preceding device. For n cascaded devices, the SI pulse is applied to the first device after every n•64 positive-going clock transitions. A common clock signal is applied to all the devices simultaneously. Parallel operation of multiple devices is accomplished by supplying clock and SI signals to all the devices simultaneously. The output of each device is then separately used for processing.

output enable

The internally generated output-enable signal enables the output stage of the sensor during the output period (64 clock cycles). During the remainder of the integration period, the output stage is in the high-impedance state, which allows output interconnections of multiple devices without interference.

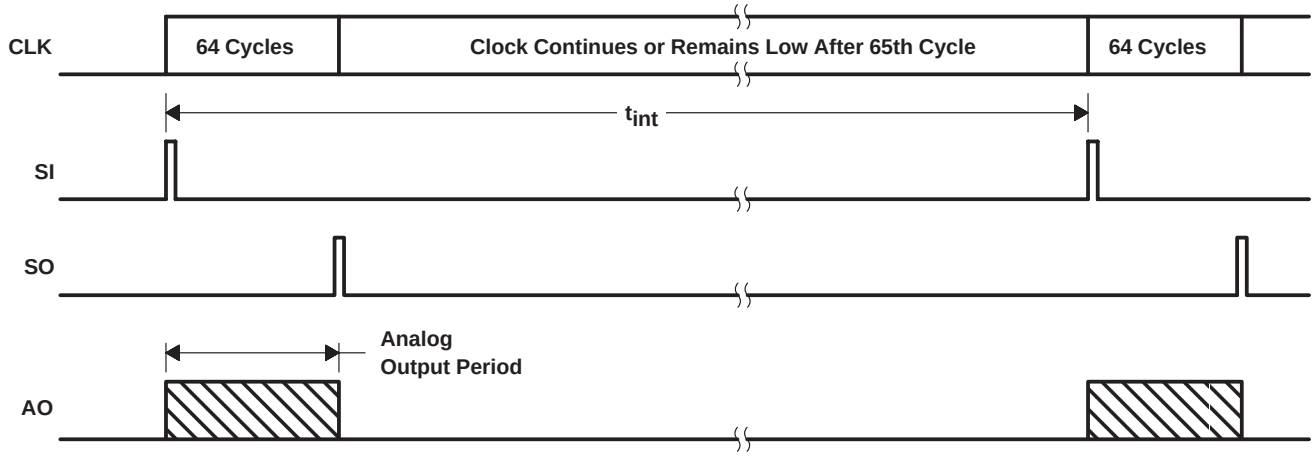


Figure 1. Timing Waveforms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) (see Note 1)†

Supply voltage range, V_{DD} (see Note 1) . . . . . –0.5 V to 7 V
Digital output voltage range, V_O . . . . . –0.5 V to V_{DD} +0.5 V
Digital output current, I_O . . . . . 3 mA
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating case temperature range, T_C (see Note 2) . . . . . –10°C to 85°C
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to GND.
2. Case temperature is the surface temperature of the plastic measured directly over the integrated circuit.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5		5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}	0		$V_{DD} \times 0.3$	V
Wavelength of light source, λ		750		nm
Clock input frequency, f_{clock}	10		500	kHz
Pulse duration, CLK low, $t_{w(CLKL)}$	1			µs
Sensor integration time, t_{int} (see Figures 1 and 2)		5		ms
Setup time, SI before CLK↑, $t_{su(SI)}$	50			ns
Hold time, SI after CLK↑, $t_{h(SI)}$	50			ns
External resistive load, AO, R_L		330		Ω
Total number of TSL214 outputs connected together			10	
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{DD} = 5 V, T_A = 25°C, f_{clock} = 180 kHz, λ_p = 565 nm, R_L = 330 Ω, C_L = 330 pF, t_{int} = 5 ms, E_e = 20 μW/cm² (unless otherwise noted) (see Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low-level output voltage	I_O = 0			0.1	V
High-level output voltage		4.4			V
Analog output voltage saturation level	E_e = 60 μW/cm²	3	3.4		V
Analog output voltage (white, average over 64 pixels)		1.75	2.2		V
Analog output voltage (dark, each pixel)	E_e = 0		0.25	0.4	V
Output voltage (white) change with change in V_{DD}	V_{DD} = 5 V ±5%		±2%		
Dispersion of analog output voltage	See Note 4			±7.5%	
Linearity of analog output voltage	See Note 5	0.85		1.15	
Pixel recovery time	See Note 6		25	40	ms
Supply current	I_{DD} (average)		4	9	mA
High-level input current	$V_I = V_{DD}$			0.5	μA
Low-level input current	V_I = 0			0.5	μA
Input capacitance			5		pF

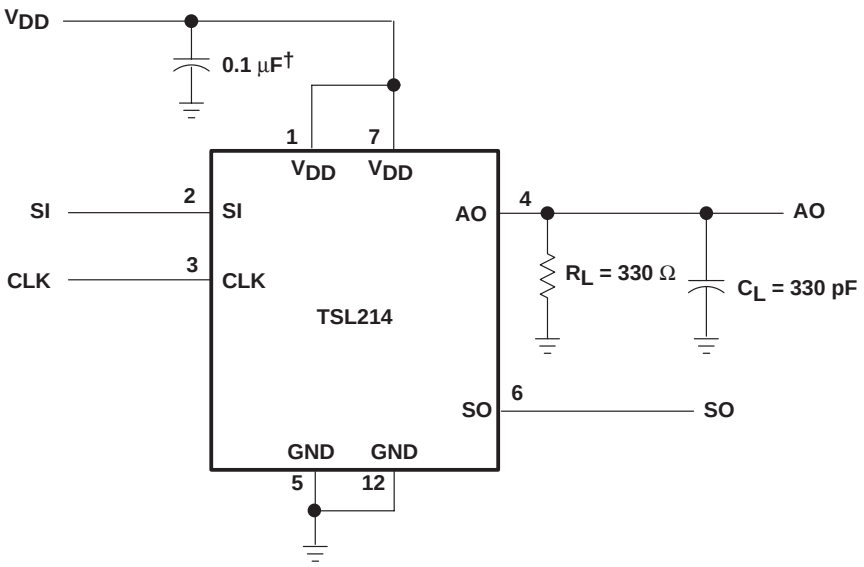
NOTES: 3. The input irradiance (E_e) is supplied by an LED array with λ_p = 565 nm.
4. Dispersion of analog-output voltage is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test.
5. Linearity of analog-output voltage is calculated by averaging over 64 pixels and measuring the maximum deviation of the voltage at 2 ms and 3.5 ms from a line drawn between the voltage at 2.5 ms and the voltage at 5 ms.
6. Pixel recovery time is the time required for a pixel to go from the analog-output voltage (white, average over 64 pixels) level to analog-output voltage (dark, each pixel) level or vice versa after a step change in light input.

operating characteristics, V_{DD} = 5 V, T_A = 25°C, f_{clock} = 500 kHz, R_L = 330 Ω, C_L = 330 pF, t_{int} = 5 ms, E_e = 20 μW/cm² (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(SO)}$	Rise time, SO	See Figure 2 and Note 7		25		ns
$t_{f(SO)}$	Fall time, SO			25		ns
$t_{pd(SO)}$	Propagation delay time, SO			70		ns
t_s	Settling time				1	μs
t_v	Valid time				1/2 f_{clock}	μs

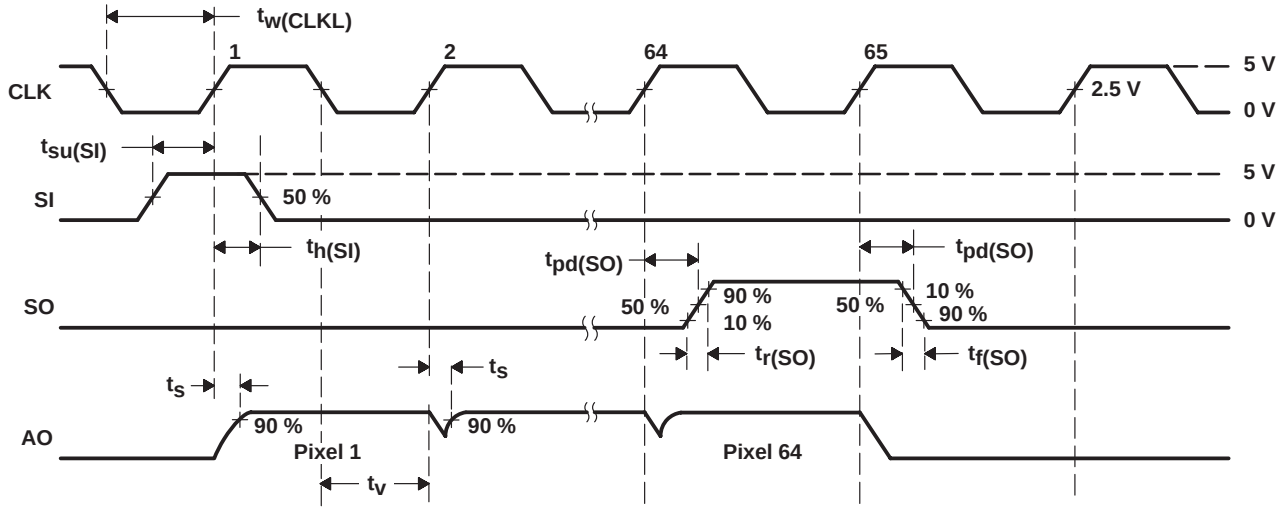
NOTE 7: Clock duty cycle is assumed to be 50%.

PARAMETER MEASUREMENT INFORMATION



† Supply bypass capacitor with short leads should be placed as close to the device as possible.

TEST CIRCUIT



OPERATIONAL WAVEFORMS

Figure 2. Test Circuit and Operational Waveforms

TYPICAL CHARACTERISTICS

NORMALIZED RESPONSIVITY vs WAVELENGTH OF INCIDENT LIGHT

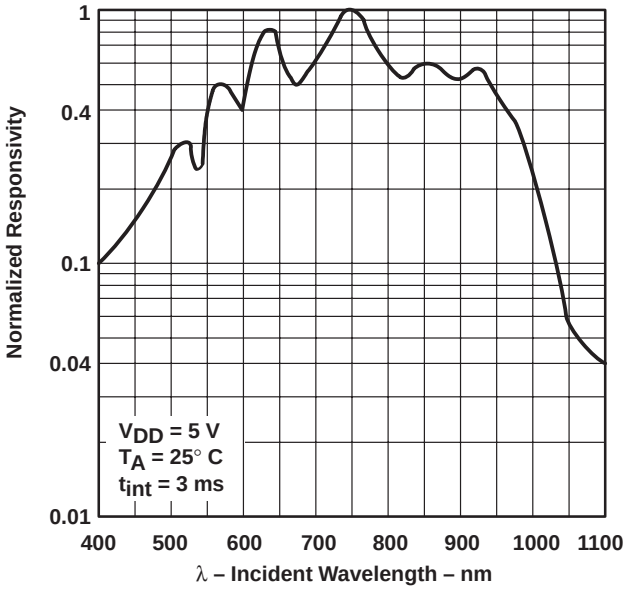


Figure 3

INTEGRATION TIME vs IRRADIANCE, FOR CONSTANT AVERAGE ANALOG OUTPUT VOLTAGE

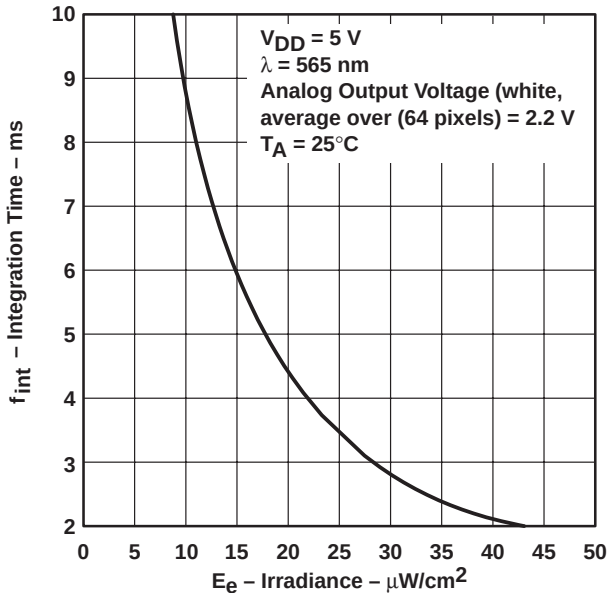


Figure 4

ANALOG OUTPUT VOLTAGE (DARK) vs INTEGRATION TIME

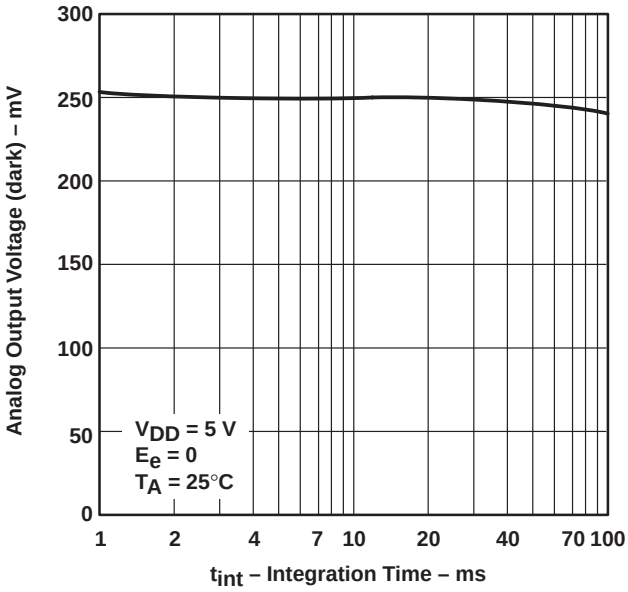


Figure 5

OUTPUT VOLTAGE vs INTEGRATION TIME

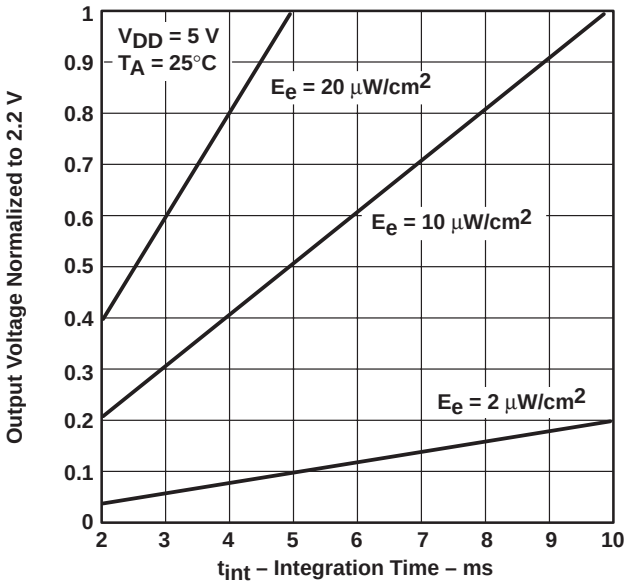
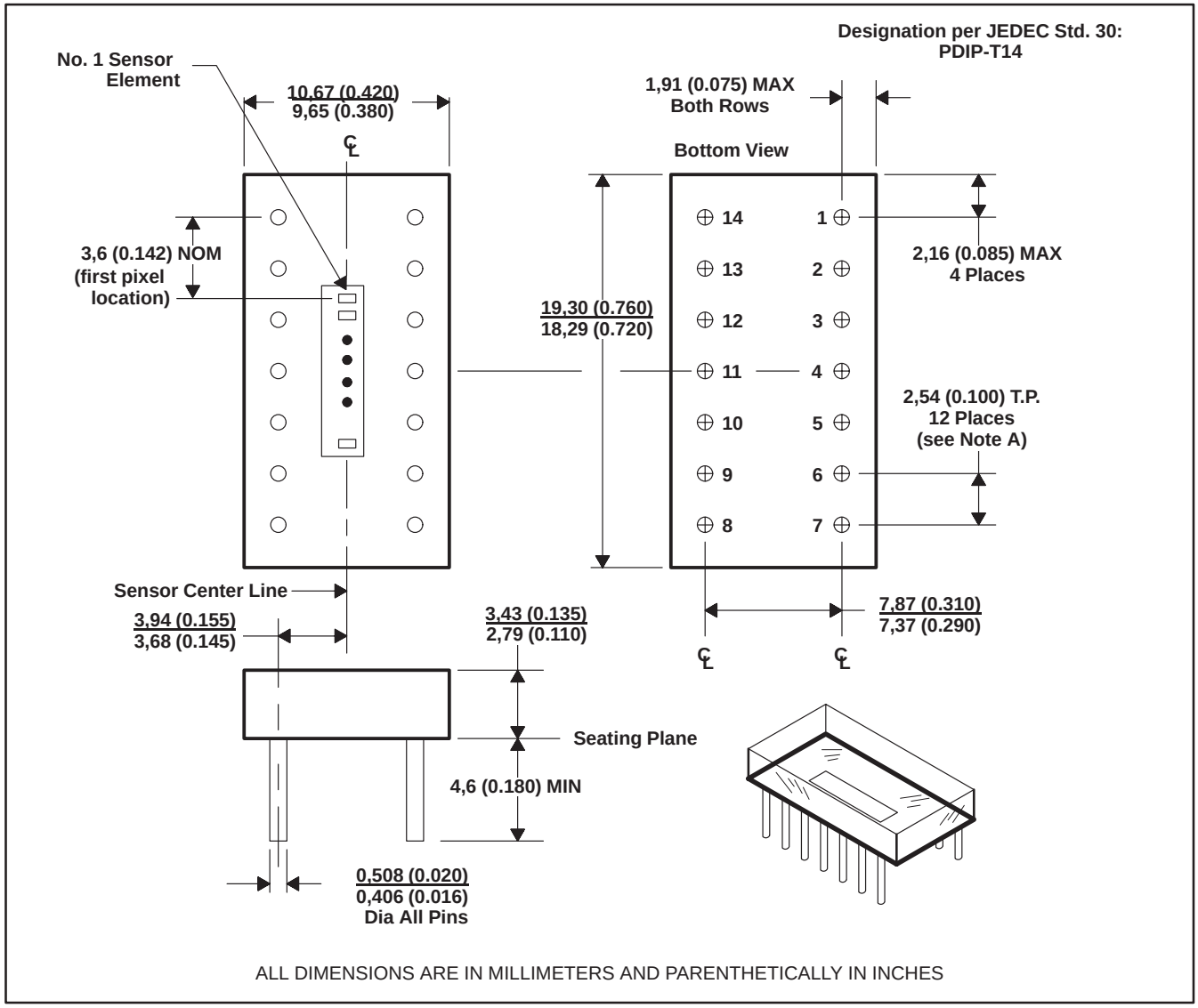


Figure 6

MECHANICAL DATA

This assembly consists of a sensor chip mounted on a printed circuit board in a clear molded plastic package. The distance between the top surface of the package and the surface of the sensor is nominally 1,0 mm (0.040 inch).



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: The true-position spacing is 2,54 mm (0.100 inch) between lead centerlines. Each pin centerline is located within 0,25 mm (0.010 inch) of its true longitudinal positions.

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