FAIRCHILD
SEMICONDUCTOR®

SPT5240

10-BIT, 400 MHz CURRENT OUTPUT D/A CONVERTER

PRELIMINARY INFORMATION

DECEMBER 15, 2001

FEATURES

- 400 MWPS update rate
- Differential current output
- +3.3 V power supply
- Ultralow power dissipation:
  140 mW (typ) @ f_{CLK} = 400 MHz
- Power-down mode draws less than 5 nA from AV_{DD} and 200 µA from DV_{DD} with no clock or data
- Excellent AC performance:
  SFDR = –57 dBc for f_{CLK} = 400 MHz and f_{OUT} = 1.27 MHz
- Internal reference

APPLICATIONS

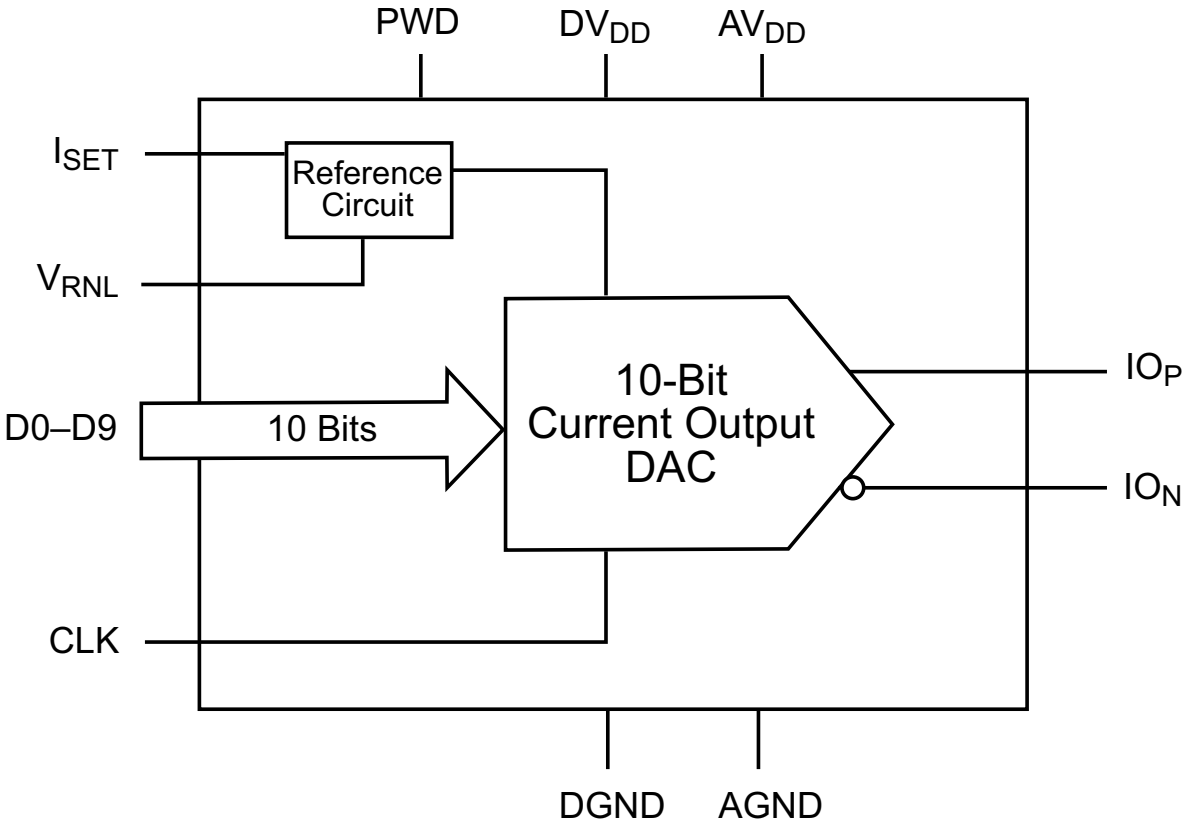
- Battery-operated devices
- Portable RF devices
- Set top boxes
- Video displays
- Broadband RF
- High-speed test equipment

GENERAL DESCRIPTION

The SPT5240 is a 10-bit digital-to-analog converter that performs at an update rate of 400 M words per second. The part is implemented in a 0.25 µm CMOS process. The architecture achieves excellent high-frequency performance with very low power dissipation. This makes it ideal for all types of battery-operated equipment requiring high-speed digital-to-analog conversion.

The SPT5240 operates over an extended industrial temperature range from –40 °C to +85 °C and is available in a 32-lead TQFP package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur) 25 °C

Supply Voltages

AV_{DD} ..... 3.7 V
DV_{DD} ..... 3.7 V
A/D ground voltage differential ..... 0.5 V

Input Voltages

D_{IN} ..... –0.5 V to DV_{DD} +0.5 V
Clock ..... –0.5 V to DV_{DD} +0.5 V

Output Currents

Bandgap reference output current (V_{RNL}) ..... 1 µA

Note: This is a No Load reference. Any load applied will cause a degradation at the output.

Temperature

Operating temperature ..... –40 to +85° C
Junction temperature ..... 150° C
Lead, soldering (10 seconds) ..... 250° C
Storage ..... –65 to +150° C

Note: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = 25° C, AV_{DD} = DV_{DD} = 3.3 V, f_{OUT} = 1.27 MHz, f_{CLK} = 400 MHz, Clock Duty Cycle = 50%, I_{OUT} = 20 mA, R_L = 50 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT5240 MIN	SPT5240 TYP	SPT5240 MAX	UNITS
DC Performance						
Resolution				10		Bits
Differential Linearity Error (DLE)	f_{CLK}=1 MHz	V		±0.9		LSB
Integral Linearity Error (ILE)	f_{CLK}=1 MHz	V		±1.34		LSB
Max Offset Error		V		20		nA
Full-Scale Error		V		±5		% FS
Gain Error		V		± 5		% FS
Maximum Full-Scale Output Current		V		40		mA
Output Compliance Voltage		V		+1.25		V
Minimum Output Impedance		V		250		kΩ
Gain Error Tempco		V		±100		ppm FS/°C
AC Performance						
Maximum Output Update Rate		V		400		MWPS
Glitch Energy		V		2.23		pV-s
Settling Time ($t_{settling}$)	See figure 1	V		104		ns
Output Rise Time		V		1.22		ns
Output Fall Time		V		1.36		ns
Output Slew Rate Rising Edge		V		802		V/µs
Output Slew Rate Falling Edge		V		656		V/µs
Spurious Free Dynamic Range (SFDR)		V		57		dBc
Total Harmonic Distortion (THD)		V		–54		dBc
Digital Data Input						
V_{IH} Minimum		V		+2.1		V
V_{IL} Maximum		V		+1.3		V
Logic “1” Current		V		±10		µA
Logic “0” Current		V		±10		µA
Input Setup Time (t_S)	See figure 1	V		590		ps
Input Hold Time (t_H)	See figure 1	V		410		ps
Output Delay Time (t_D)	See figure 1	V		1 clk+4ns		ns
Clock Feedthrough		V		–29		dBFS
Reference						
Reference Voltage		V		+1.17		V

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PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT5240 MIN	SPT5240 TYP	SPT5240 MAX	UNITS
Power Supply Requirements						
Digital Supply Voltage		V		+3.3		V
Analog Supply Voltage		V		+3.3		V
Supply Current Sleep Mode						
AV_{DD}	50 MHz Clock	V		410		nA
DV_{DD}	50 MHz Clock	V		1		mA
AV_{DD}	Clock/Data Off	V		4		nA
DV_{DD}	Clock/Data Off	V		193		µA
PWD Pin Current	Clock/Data Off	V		83		µA
Power Supply Rejection Ratio		V		50		dB
Power Dissipation	20 mA I_{OUT}	V		196		mW
	12 mA I_{OUT}	V		140		mW
Clock Input						
V_{IH} Minimum		V		+1.5		V
V_{IL} Maximum		V		+1.2		V
Input Current		V		±10		µA

TEST LEVEL CODES

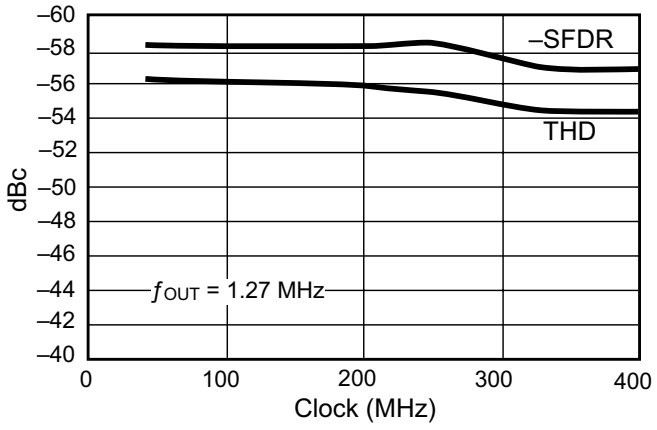
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

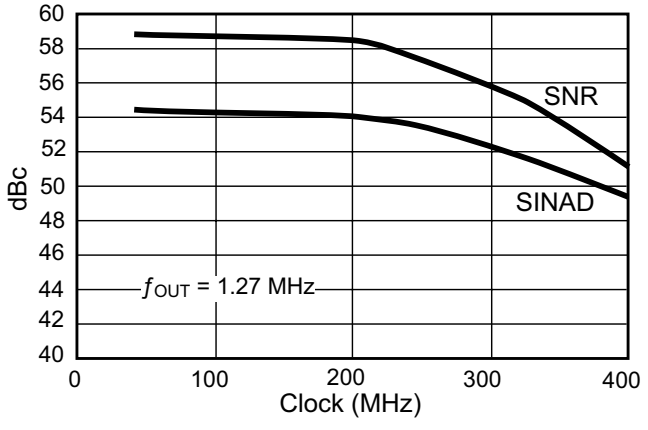
LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

THD and SFDR vs Input Frequency



SNR and SINAD vs Input Frequency



SPECIFICATION DEFINITIONS

DIFFERENTIAL LINEARITY ERROR (DLE) OR DIFFERENTIAL NONLINEARITY (DNL)

In an ideal DAC, output transitions are 1 LSB apart. Differential Linearity Error is the maximum deviation, expressed in LSBs, from this ideal value.

INTEGRAL LINEARITY ERROR (ILE) OR INTEGRAL NONLINEARITY (INL)

The ideal transfer for a DAC is a straight line drawn between "zero-scale" output and "full-scale" output. ILE is the worst-case deviation of the output from the straight line. The deviation of the output at each code is measured and compared to the ideal output at that code. ILE may also be expressed as a sum of DLE starting from code 0…0 to the code that ILE measurement is desired.

MONOTONIC

A digital-to-analog converter is considered monotonic if the analog output never decreases as the code value at the input increases. A DLE of –1 would indicate a non-monotonic DAC.

OFFSET ERROR

The deviation, from ideal, at the DAC output when set to zero-scale. In the current output DAC there should be no current flow at zero-scale. Therefore, Offset Error is the amount of current measured with the DAC set to zero-scale.

FULL-SCALE ERROR

The ideal maximum full-scale current output of the DAC is determined by the value of R_{SET}. Full-scale error is the deviation of the output from ideal with the offset error included.

GAIN ERROR

The ideal maximum full-scale current output of the DAC is determined by the value of R_{SET}. Gain error is the deviation of the output from ideal with the offset error removed.

FULL-SCALE OUTPUT

The maximum current output available for a given value of R_{SET}. In the SPT5240 IO_P is full-scale at code 1111111111 and IO_N is full-scale at code 0000000000.

ZERO-SCALE OUTPUT

The minimum current output, ideally zero amps. In the SPT5240 IO_P is zero-scale at code 0000000000 and IO_N is zero-scale at code 1111111111.

COMPLIANCE VOLTAGE

The maximum terminal output voltage for which the device will provide the specified current output characteristics.

HARMONIC

1. Of a sinusoidal wave, an integral multiple of the frequency of the wave. *Note:* The frequency of the sine wave is called the fundamental frequency or the first harmonic, the second harmonic is twice the fundamental frequency, the third harmonic is thrice the fundamental frequency, etc.

2. Of a periodic signal or other periodic phenomenon, such as an electromagnetic wave or a sound wave, a component frequency of the signal that is an integral multiple of the fundamental frequency. *Note:* The fundamental frequency is the reciprocal of the period of the periodic phenomenon.

TOTAL HARMONIC DISTORTION (THD)

The ratio of the sum of the power of first 9 harmonics above the fundamental frequency to the power of the fundamental frequency. Usually expressed in dBc.

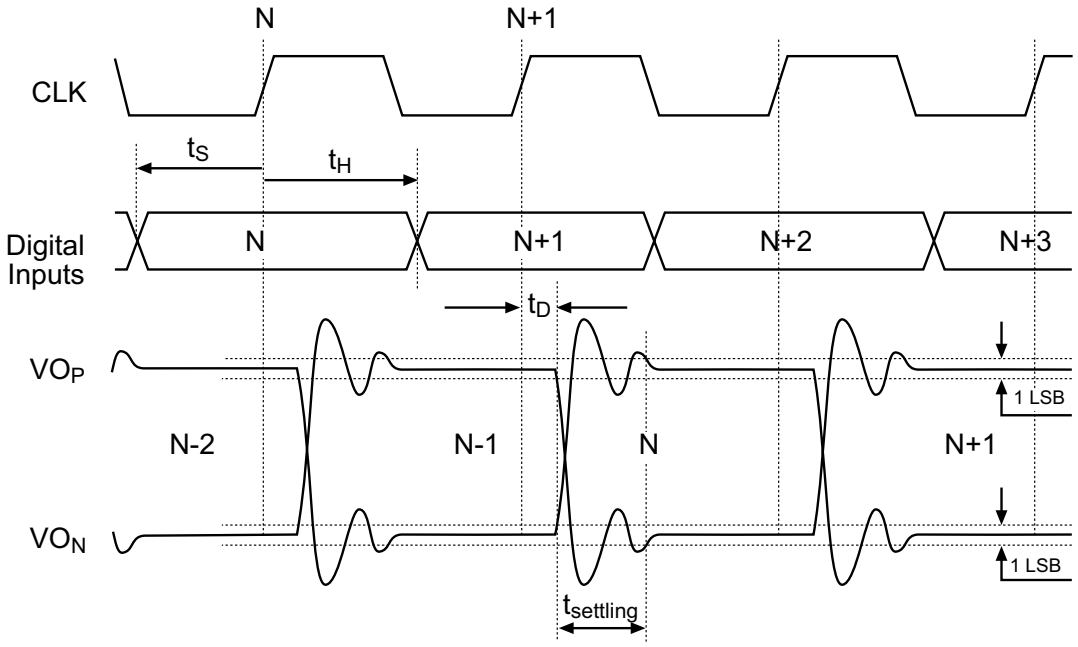
SPURIOUS FREE DYNAMIC RANGE (SFDR)

The ratio of the fundamental sinusoidal power to the power of the single largest harmonic or spurious signal within the range of the 9th harmonic.

CLOCK FEEDTHROUGH

The ratio of the full-scale output to the peak-to-peak noise generated at the DAC output by input clock transitions. Expressed in dBFS.

Figure 1 – Timing Diagram



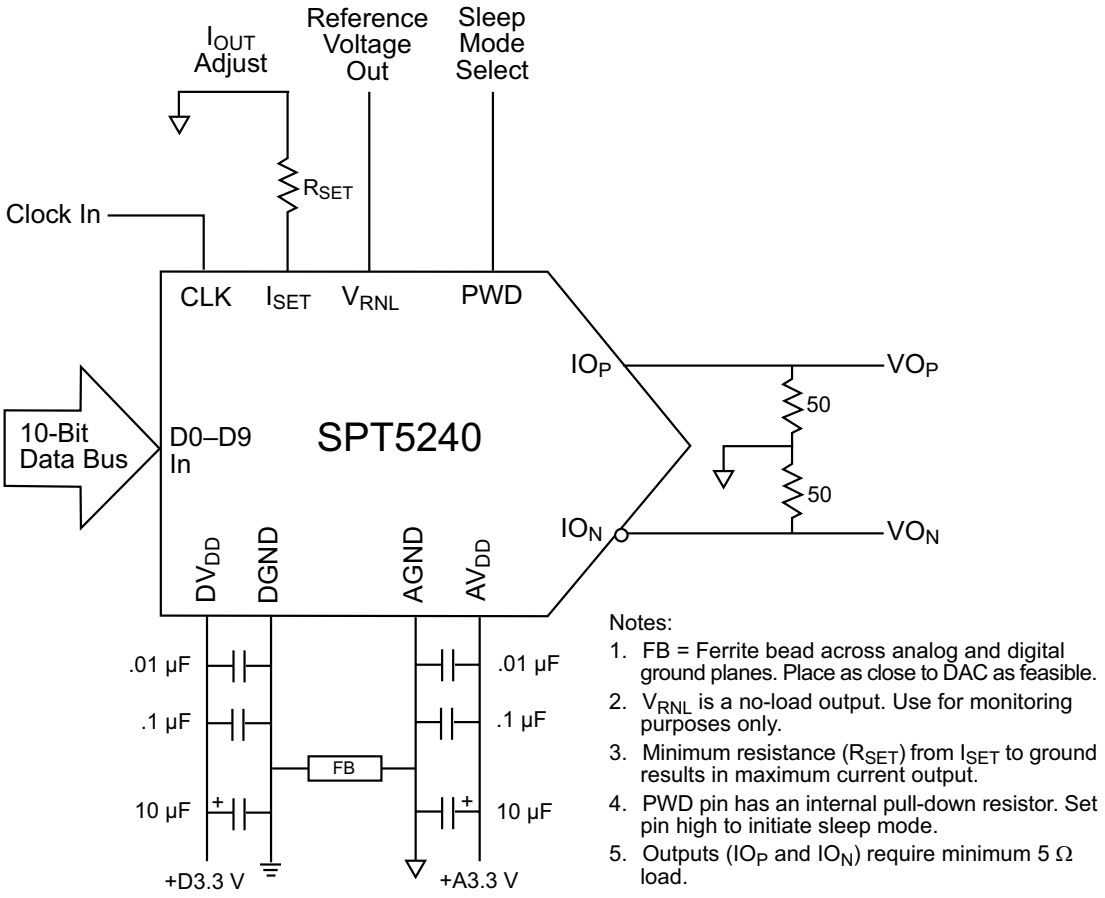
THEORY OF OPERATION

The SPT5240 is a 10-bit 400 MWPS digital-to-analog converter implemented in 0.25 µm CMOS technology. It integrates a DAC core with a bandgap reference and operates from a +3.3-volt power supply.

The DAC architecture is a compound differential current output DAC consisting of a 6-bit fully segmented DAC for the MSBs and a 4-bit fully segmented DAC for the LSBs. The input cell, followed by a master-slave latch, buffers the digital inputs. A 6:64 decoder decodes the digital data for the MSBs, and a 4:16 decoder does so for the LSBs. The outputs of the decoders are latched using a second bank of master-slave latches whose outputs then drive differential current switches, which steer the appropriate current to the IO_P or IO_N outputs.

The analog (AV_{DD}) and digital (DV_{DD}) power supplies are separated on chip to allow flexibility in the interface board. The analog (AGND) and digital (DGND) are separated on chip. Circuit board ground planes should be separated and tied together with a ferrite bead.

Figure 2 – Typical Interface Circuit



Notes:
1. FB = Ferrite bead across analog and digital ground planes. Place as close to DAC as feasible.
2. V_{RNL} is a no-load output. Use for monitoring purposes only.
3. Minimum resistance (R_{SET}) from I_{SET} to ground results in maximum current output.
4. PWD pin has an internal pull-down resistor. Set pin high to initiate sleep mode.
5. Outputs (IO_P and IO_N) require minimum 5 Ω load.

TYPICAL INTERFACE CIRCUIT

The SPT5240 requires few external components to achieve the stated performance. Figure 2 shows the typical interface requirements when used in normal circuit operation. The following sections provide descriptions of the major functions and outline performance criteria to consider for achieving optimal performance.

DIGITAL INPUTS

The SPT5240 has a 10-bit-wide parallel data input designed to work at +3.3 V CMOS levels. Fast edges and low transients provide for improved performance.

CLOCK INPUT

The SPT5240 is driven by a single-ended clock circuit. In order to achieve best performance at the highest throughput, a clock generation circuit should provide fast edges and low jitter.

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit. This circuit provides robust ESD protection in excess of 3,000 volts, in human body model, without sacrificing speed.

POWER SUPPLIES AND GROUNDING

The SPT5240 may be operated in the range of 2.8 to 3.6 volts. Normal operation is recommended to be separate analog and digital supplies operating at +3.3 volts. All power supply pins should be bypassed as close to the package as possible with the smallest capacitor closest to the device. Analog and digital ground planes should be connected together with a ferrite bead as shown in figure 2 and as close to the DAC as possible.

SLEEP MODE

To conserve power, the SPT5240 incorporates a power-down function. This function is controlled by the signal on pin PWD. When PWD is set high, the SPT5240 enters the sleep mode. The analog outputs are both set to zero current output, resulting in less than 500 nA current draw from the analog supply. For minimum power dissipation, data and clock inputs should be removed.

REFERENCES

The SPT5240 utilizes an on-chip bandgap reference to set full-scale output current level. The current reference to the DAC circuitry is set by the external resistance value between the I_{SET} pin and analog ground. An output of the bandgap reference voltage is available for monitoring purposes only at the V_{RNL} pin.

ANALOG OUTPUTS

The SPT5240 provides differential current outputs which provide an output level based on the value of R_{SET} at maximum output code (see Figure 3). The required value of R_{SET} may be calculated using the formulas:

$$LSB = I_{FS} / 1023$$

Then:

$$R_{SET} = \frac{1.1302 - (1000 \bullet LSB)}{4 \bullet LSB}$$

Where I_{FS} is the desired full-scale current output.

Each output requires a minimum 5-ohm load to analog ground. The typical circuit utilizes 50-ohm loads to develop voltage for the output transformer.

Figure 3 – R_{SET} vs I_{OUT}

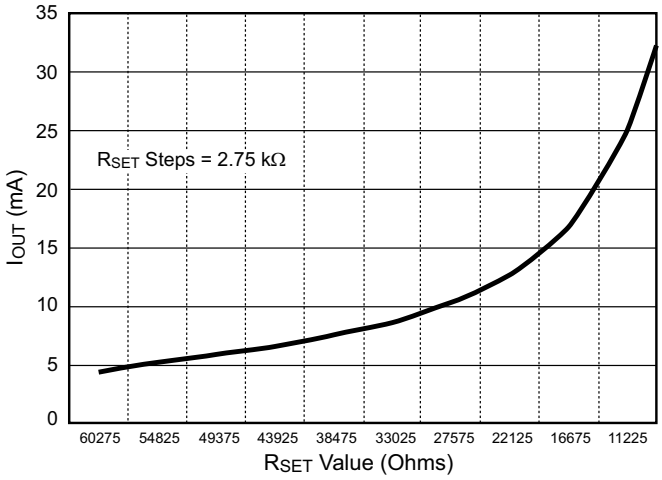


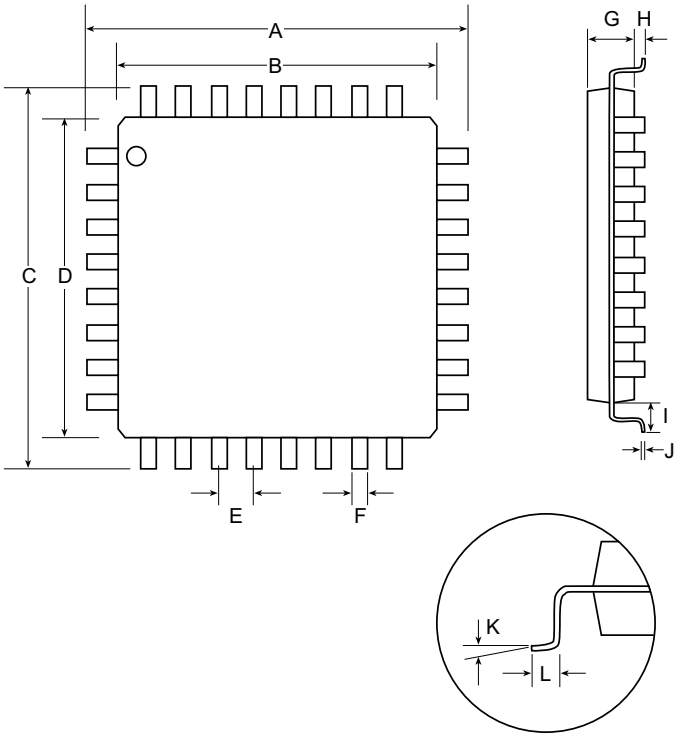
Table I – Input Data Format

Input Code D9–D0	Analog Output	
	IO_N	IO_P
0000000000	FS	0
1111111111	0	FS
Sleep XXXXXXXXXX	0	0

X indicates either data state.

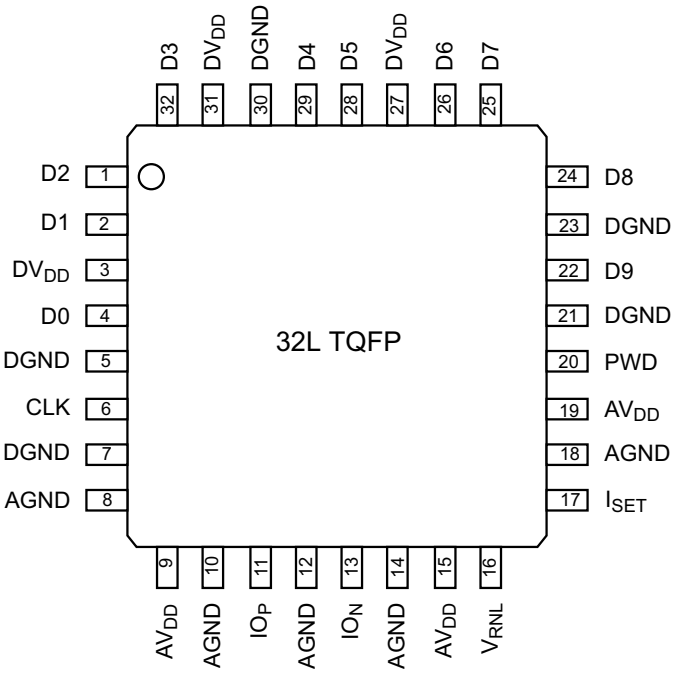
PACKAGE OUTLINE

32-Lead TQFP



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.346	0.362	8.80	9.20
B	0.272	0.280	6.90	7.10
C	0.346	0.362	8.80	9.20
D	0.272	0.280	6.90	7.10
E	0.031 typ		0.80 BSC	
F	0.012	0.016	0.30	0.40
G	0.053	0.057	1.35	1.45
H	0.002	0.006	0.05	0.15
I	0.037	0.041	0.95	1.05
J		0.007		0.17
K	0°	7°	0°	7°
L	0.020	0.030	0.50	0.75

PIN ASSIGNMENTS



PIN FUNCTIONS

ANALOG OUTPUTS	
IO_P	DAC current output. Full-scale output at 11...11 input code.
IO_N	Differential current output. Full-scale output at 00...00 input code.
DIGITAL INPUTS	
D0–D9	Digital Inputs (D0 is the LSB)
PWD	Power down mode pin. Active high. Internally pulled down.
CLK	Clock input pin. Data is latched on the rising edge.
REFERENCE	
V_{RNL}	Voltage Reference – No Load Output. This pin is provided for monitoring purposes only.
I_{SET}	Full-scale Adjust Control. Connection for reference-current setting resistor.
POWER	
AGND	Analog Supply Ground.
DGND	Digital Supply Ground.
AV_{DD}	Analog +3.3 V supply.
DV_{DD}	Digital +3.3 V supply.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT5240SIT	–40 to +85 °C	32L TQFP

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.