FAIRCHILD
SEMICONDUCTOR®

SPT7883

10-BIT, 70 MSPS A/D CONVERTER

PRELIMINARY INFORMATION

NOVEMBER 21, 2001

FEATURES

- 2.5 V power supply
- SNR: 60 dB @f_{IN} = 10 MHz, f_S = 70 MHz;
  58 dB @f_{IN} = 30 MHz
- Low power dissipation: 145 mW @2.5 V;
  Sleep mode: 2.6 mW
- Sample rate: 10–115 MSPS
- Frequency-dependent biasing
- Internal sample-and-hold
- Differential input
- Low input capacitance
- 9.67 ENOBs @ f_{IN} = 10 MHz, f_S = 70 MHz
- SFDR: 73 dB
- IP core available

APPLICATIONS

- Imaging
- Computer scanners
- Communications
- Set top boxes
- Video products
- Battery-operated equipment
- Portable test equipment

GENERAL DESCRIPTION

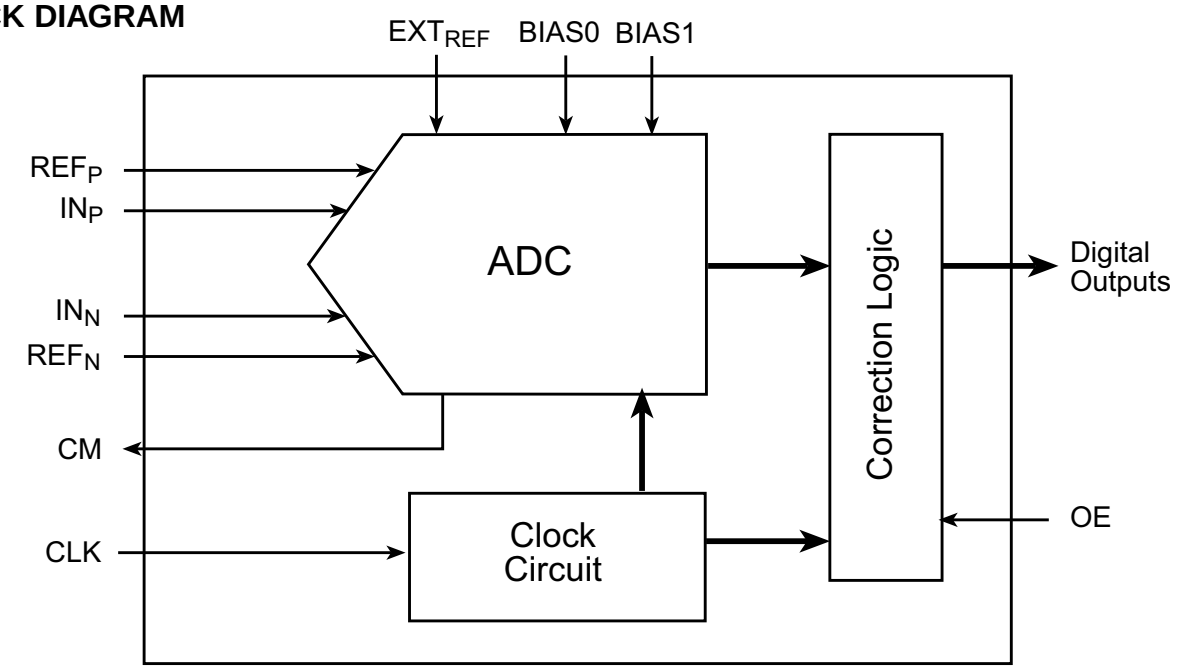
The SPT7883 is a compact, high-speed, low-power 10-bit monolithic analog-to-digital converter, implemented in a 0.25 µm CMOS process. It has 10-bit resolution with 9.67 effective bits and spurious-free dynamic range (SFDR) of 73 dB for video frequency signals. The converter includes a high bandwidth sample-and-hold. The full-scale range can be set between ±0.5 V and ±1.5 V. It operates from a single 2.5 V supply. Its low distortion and high dynamic range provide the performance needed for demanding imaging, video, and communications applications.

The bias current level for the ADC is automatically adjusted based on the clock input frequency. Hence, the power dissipation of the device is continuously optimized for the operating frequency.

The SPT7883 has a pipelined architecture, resulting in low input capacitance. Digital error correction of the 9 most significant bits ensures good linearity for input frequencies approaching Nyquist.

The SPT7883 is available in a 28-lead SSOP package over the industrial temperature range (–40 to +85 °C).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur) 25 °C

Supply Voltages

V_{DD} ..... –0.3 V to +3 V
OV_{DD} ..... –0.3 V to V_{DD} + 0.3 V

Input Voltages

Digital Input..... –0.3 V to V_{DD} + 0.3 V
REF_P ..... –0.3 V to V_{DD} + 0.3 V
REF_N ..... –0.3 V to V_{DD} + 0.3 V
CLOCK ..... –0.3 V to V_{DD} + 0.3 V

Temperatures

Operating Temperature ..... ….–40 to +85 °C
Storage Temperature.. ..... –65 to +125 °C

Note: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = 25 °C, V_{DD} = OV_{DD} = 2.5 V, f_S = 70 MSPS, f_{IN} = 10 MHz, differential input signal, internal references, 50% clock duty cycle, typical bias, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT7883 MIN	SPT7883 TYP	SPT7883 MAX	UNITS
DC Performance						
Differential Linearity Error (DLE)		V		±0.35		LSB
Integral Linearity Error (ILE)		V		±0.25		LSB
No Missing Codes				Guaranteed		
Offset Error		V		±4.88		mV
Gain Error		V		0.98		%FS
Analog Input						
Input Voltage Range (differential)		V	±0.5	±1.0	±1.5	V
Input Common Mode Voltage		V		1.2		V
Timing Characteristics						
Conversion Rate[1]		V	10	70	115	MSPS
Pipeline Delay		V		6		Clocks
CLK to Output Delay		V		6		ns
Dynamic Performance						
Signal to Noise and Distortion Ratio (SINAD)	f_{IN} = 10 MHz	V		60		dBc
	f_{IN} = 30 MHz	V		58		dBc
Signal to Noise Ratio (SNR)	f_{IN} = 10 MHz	V		60		dBc
	f_{IN} = 30 MHz	V		59		dBc
Total Harmonic Distortion (THD)	f_{IN} = 10 MHz	V		–71		dBc
	f_{IN} = 30 MHz	V		–68		dBc
Spurious Free Dynamic Range (SFDR)	f_{IN} = 10 MHz	V		73		dBc
	f_{IN} = 30 MHz	V		70		dBc
Power Supply Requirements						
Supply Voltage (V_{DD})		V	2.3	2.5	2.75	V
Supply Current (V_{DD})		V		50		mA
Supply Current (OV_{DD})		V		8		mA
Output Driver Supply Voltage (OV_{DD})			2.3	2.5	2.75	V
Power Dissipation	f_S=70 MHz; f_{IN}=10 MHz	V		145		mW
Sleep Mode Power Dissipation	Clock off	V		2.6		mW

[1]See graph on page 4

ELECTRICAL SPECIFICATIONS

T_A = 25 °C, V_{DD} = OV_{DD} = 2.5 V, f_S = 70 MSPS, f_{IN} = 10 MHz, differential input signal, internal references, 50% clock duty cycle, typical bias, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT7883 MIN	SPT7883 TYP	SPT7883 MAX	UNITS
External Reference Voltages	EXT_{REF} = 1					
Negative Input Voltage		V	0.5	0.85		V
Positive Input Voltage		V		1.60	1.9	V
ΔReference Input Voltage Range (REF_P–REF_N)		V	0.5	0.75	1.4	V
Internal Reference Voltages	EXT_{REF} = 0					
Negative Input Voltage		V		0.75		V
Positive Input Voltage		V		1.75		V
Common Mode Voltage		V		1.20		V
Digital Inputs						
Logic “0” Voltage					0.4	V
Logic “1” Voltage			2.1			V
Logic “0” Current (V_I=GND)					±10	µA
Logic “1” Current (V_I=V_{DD})					±10	µA
Digital Outputs						
Logic “0” Voltage	I = 2 mA	V		0.2	0.4	V
Logic “1” Voltage	I = –2 mA	V	85% OV_{DD}	90% OV_{DD}		V

TEST LEVEL CODES

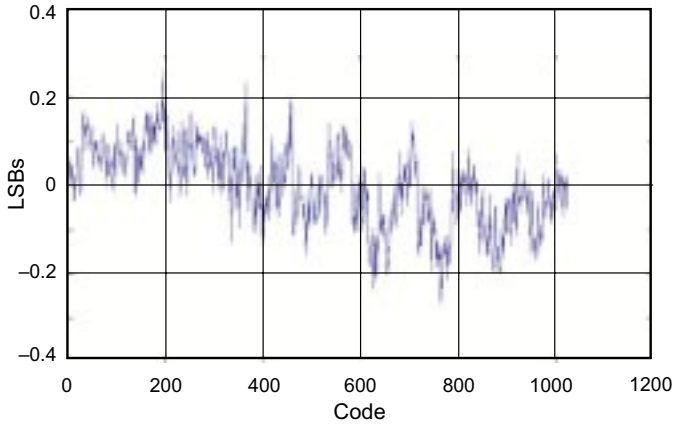
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

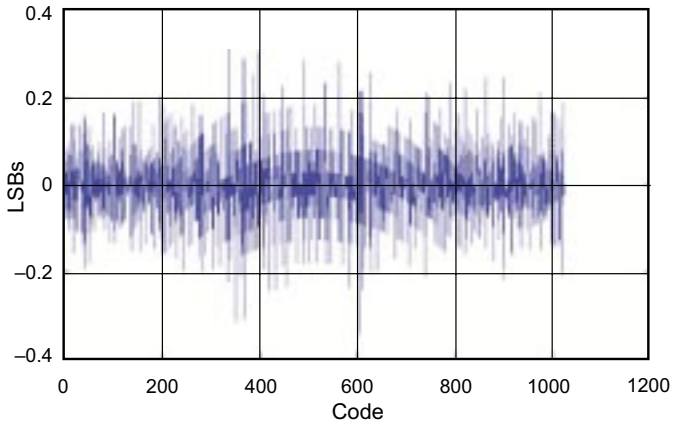
LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

Integral Linearity Error Versus Code

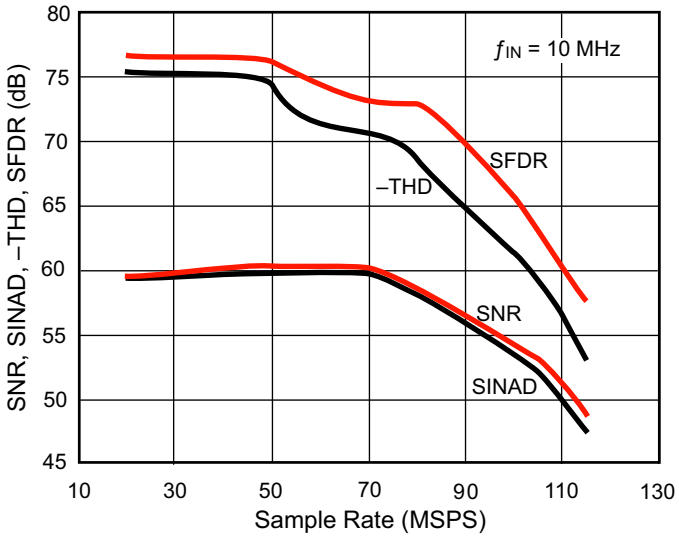


Differential Linearity Error Versus Code

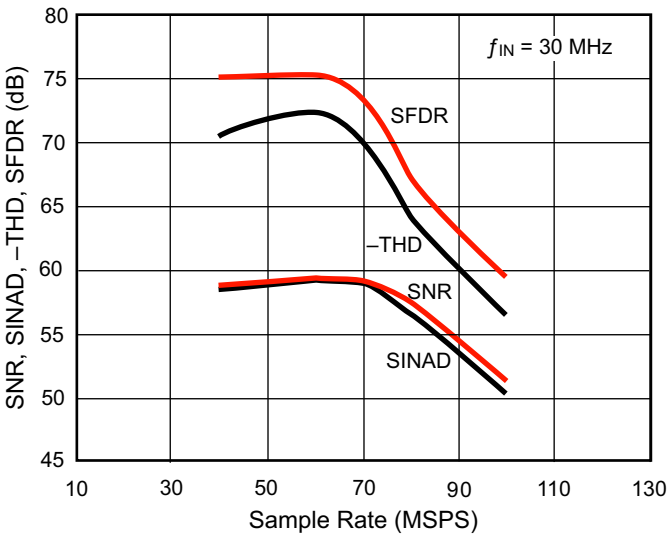


TYPICAL PERFORMANCE CHARACTERISTICS

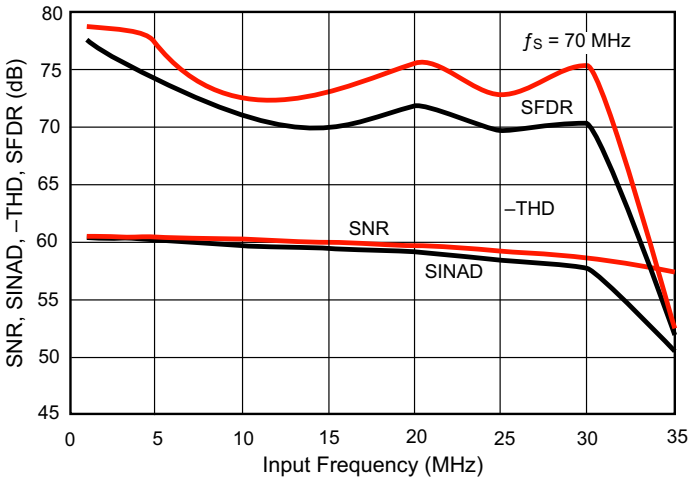
Performance Versus Sample Rate @ f_{IN} = 10 MHz



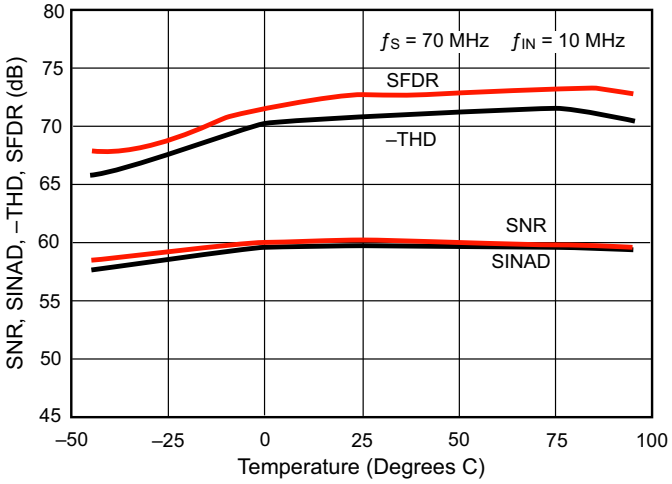
Performance Versus Sample Rate @ f_{IN} = 30 MHz



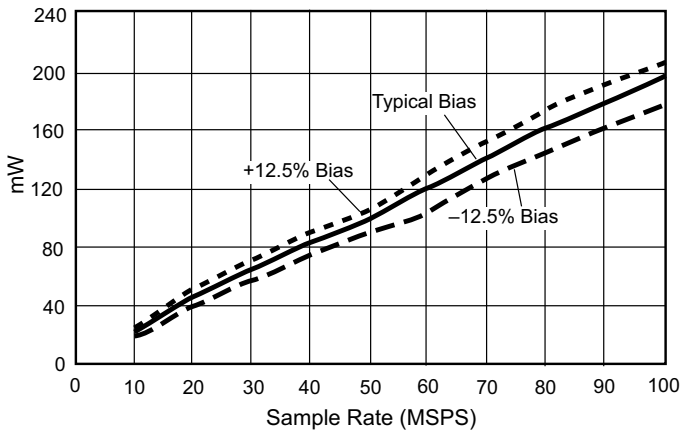
Performance Versus Input Frequency



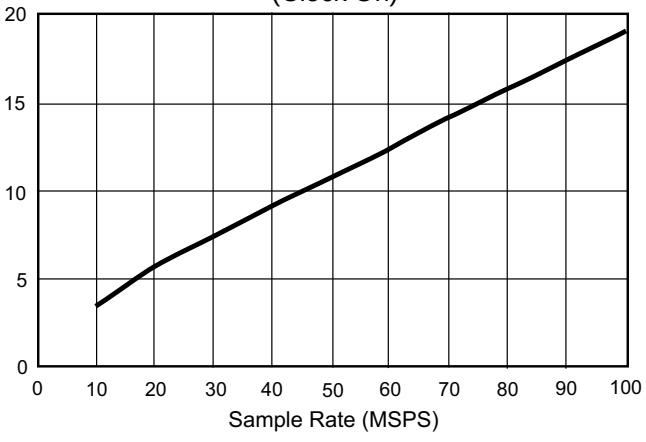
Performance Versus Temperature



Power Dissipation Versus Sample Rate



Sleep Mode Power Dissipation Versus Sample Rate (Clock On)



REFERENCES

The SPT7883 can use either an internal or external voltage reference. When the digital input EXT_{REF} is high, the external reference is used. When EXT_{REF} is low, the internal reference is used.

INTERNAL REFERENCE

The internal references are set at +0.75 V and +1.75 V. When the internal reference is used, the full-scale range of the analog input is set at ±1.0 V differential. Do not connect external references when the internal reference is used.

EXTERNAL REFERENCE

When external references are used, the voltages applied to the $V_{REF}+$ and $V_{REF}–$ pins determine the input voltage range, which is equal to $\pm(V_{REF}+ – V_{REF}–)$. Externally generated reference voltages must be connected to these pins and should be symmetric about the common mode voltage (1.2 V).

ANALOG INPUT

The SPT7883 has a differential input that should have a common mode voltage of 1.2 V. The input voltage range is determined by the reference voltages, which may be generated internally or applied externally.

The input of the SPT7883 can be configured in various ways depending on whether a single-ended or differential, AC- or DC-coupled input is desired.

AC-coupled input is most conveniently implemented using a transformer with a center-tapped secondary winding. The center tap is connected to the CM node, as shown in figure 1. In order to obtain low distortion, it is important that the selected transformer does not exhibit core saturation at full scale. Excellent results are obtained with the Mini-Circuits T1-6T or T4-6T. Proper termination of the input is important for input signal purity. A 50 Ω resistor in series with each input and a small capacitor (typ 27 pF) across the inputs will attenuate kickback noise from the sample-and-hold.

If a DC-coupled single-ended input is wanted, a solution based on operational amplifiers is usually preferred. The AD8138 is an easy-to-use, single-ended-to-differential converter. Its data sheet claims –87 dBc @ 20 MHz. Lower-cost operational amplifiers may be used if the demands are less strict.

CLOCK

In order to preserve accuracy at high input frequency, it is important that the clock have low jitter and fast rise and fall times. Rise/fall times should be kept shorter than 2 ns whenever possible. Overshoot should be minimized. Low jitter is especially important when converting high-frequency input signals. Jitter causes the noise floor to rise proportionally to input signal frequency. The analog input is sampled at the falling edge of the clock.

Figure 1 – Typical Interface Circuit

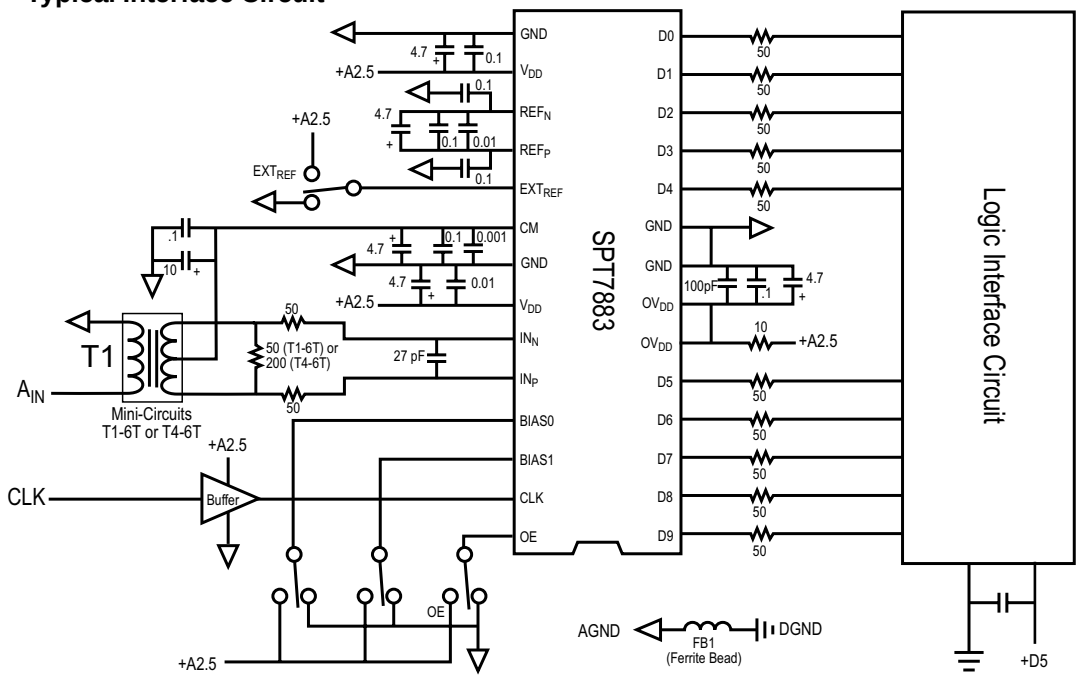
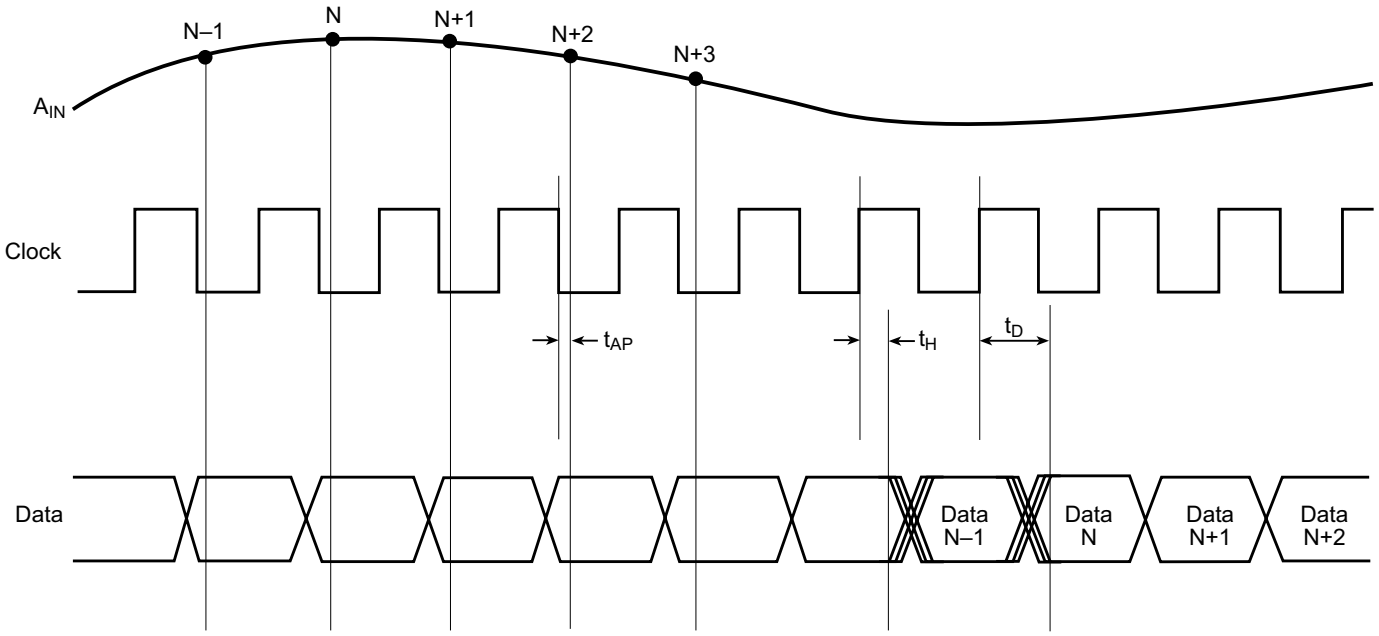


Figure 2 – Timing Diagram



DIGITAL OUTPUTS

When the output enable is set high, then the digital output data appears in offset binary code at CMOS 2.5 V logic levels. Full-scale negative input results in output code 000…0. Full-scale positive input results in output code 111…1. Output data is available 6 clock cycles after the data is sampled. The analog input is sampled one aperture delay (t_{AP}) after the high-to-low clock transition. Output data should be sampled as shown in the timing diagram above.

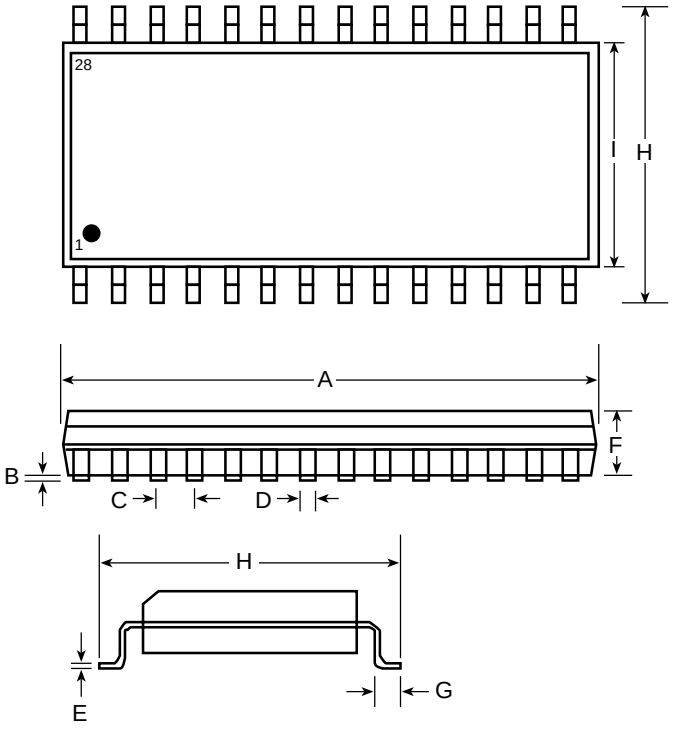
When the output enable is set low, then the digital output data goes into a high Z-mode.

PCB LAYOUT AND DECOUPLING

A well designed PCB is necessary to get good spectral purity from any high-performance ADC. A multilayer PCB with a solid ground plane is recommended for optimum performance. If the system has a split analog and digital ground plane, it is recommended that all ground pins on the ADC be connected to the analog ground plane (AGND). All digital interface circuits are connected to the digital ground (DGND). AGND and DGND planes must be connected through a ferrite bead placed as close to the ADC as possible. Refer to the typical interface circuit diagram (figure 1) or AN7883 application note for recommended decoupling and PCB layout.

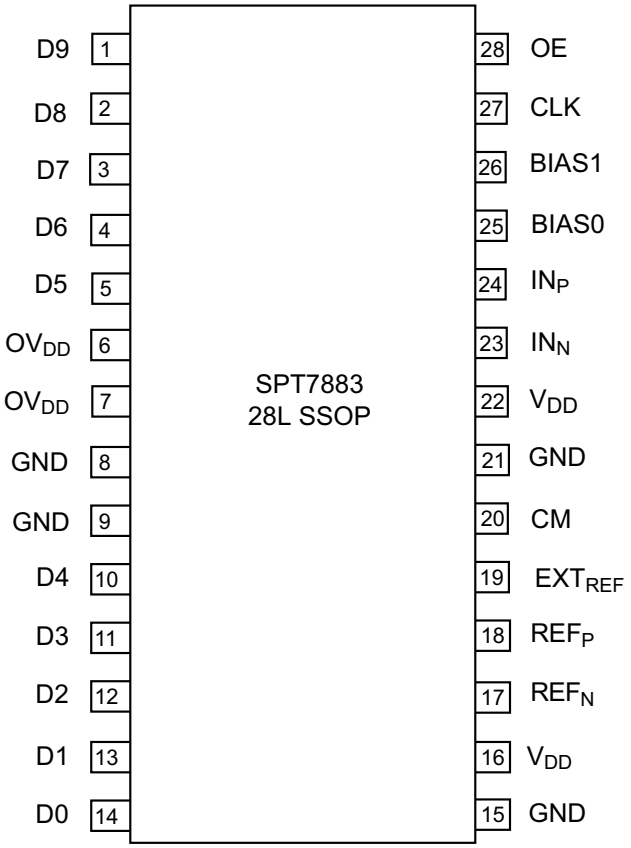
PACKAGE OUTLINE

28-Lead SSOP



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.397	0.407	10.07	10.33
B	0.002	0.008	0.05	0.21
C	0.0256 typ		0.65 typ	
D	0.010	0.015	0.25	0.38
E	0.004	0.008	0.09	0.20
F	0.066	0.070	1.68	1.78
G	0.025	0.037	0.63	0.95
H	0.301	0.311	7.65	7.90
I	0.205	0.212	5.20	5.38

PIN ASSIGNMENTS



PIN FUNCTIONS

Pin Name	Description
IN_P IN_N	Differential input signal pins. Common-mode voltage: 1.2 V
REF_P REF_N	Reference I/O pins.
BIAS0, BIAS1	BIAS1=0, BIAS0=0: Sleep mode (power save) BIAS1=0, BIAS0=1: –12.5% bias BIAS1=1, BIAS0=0: +12.5% bias BIAS1=1, BIAS0=1: Typ. Bias
CLK	Clock input
CM	Common mode voltage output
D9–D0	Digital outputs (MSB to LSB)
OE	Enable digital outputs Logic 1: Digital output enable Logic 0: Tri-state
EXT_{REF}	Digital input: Reference select. EXT_{REF}=1: Use external reference. Internal reference powered down. EXT_{REF}=0: Internal reference is used.
V_{DD}	Power supply pins
GND	Ground pins
OV_{DD}	Power supply pins for output drivers

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT7883SIR	–40 to +85 °C	28L SSOP

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