GSM-GPRS Receiver

Description

The T0701 is a bipolar integrated RF transceiver for GSM-based cellular systems (900/ 1800/ 1900 MHz) and other wireless communication applications. This integrated circuit consists of a superheterodyne receiver with a high 1st intermediate frequency (IF) of 378 MHz and an offset PLL transmitter architecture.
Receiver functions include: low-noise pre–amplifier, mixer, digitally controlled gain amplifiers, quadrature demodulator, baseband filters, and baseband amplifiers. Transmitter functions include: I/Q modulator, phase comparator, auxiliary VCO including PLL functions and down-converter. The device is controlled by a 3-wire bus.

The T0701 enables to build a small-sized GSM transceiver by adding a single PLL frequency synthesizer (main oscillator), a power amplifier (e.g. TST0911) and few external components.
Triple band operation is possible with a 1st IF of 378 MHz and using only a single channel raster VCO with a tuning range of approximately 8.54%.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- One device for all GSM bands (900/ 1800/ 1900 MHz)
- Support of GPRS; EDGE compatible (receive path)
- Supply voltage range 2.7 V to 3.3 V
- Current consumption (continuous operation)
  RX mode: 43 mA, @ Vs = 3 V
  TX mode: 50 mA, @ Vs = 3 V
  Power-down mode: < 10 µA
- 100 dB of total voltage gain
- Noise figure 4.5 dB; on-chip auxiliary VCO
- Modulation loop transmitter architecture avoids TX spurious, and exhibits excellent noise performance
- No TX duplex filter needed, longer battery life
- 3-wire bus control for RX/ TX frequencies, gain, modes, and band selection
- 64-Pin Thin Quad Flat Package (TQFP64)

Block Diagram

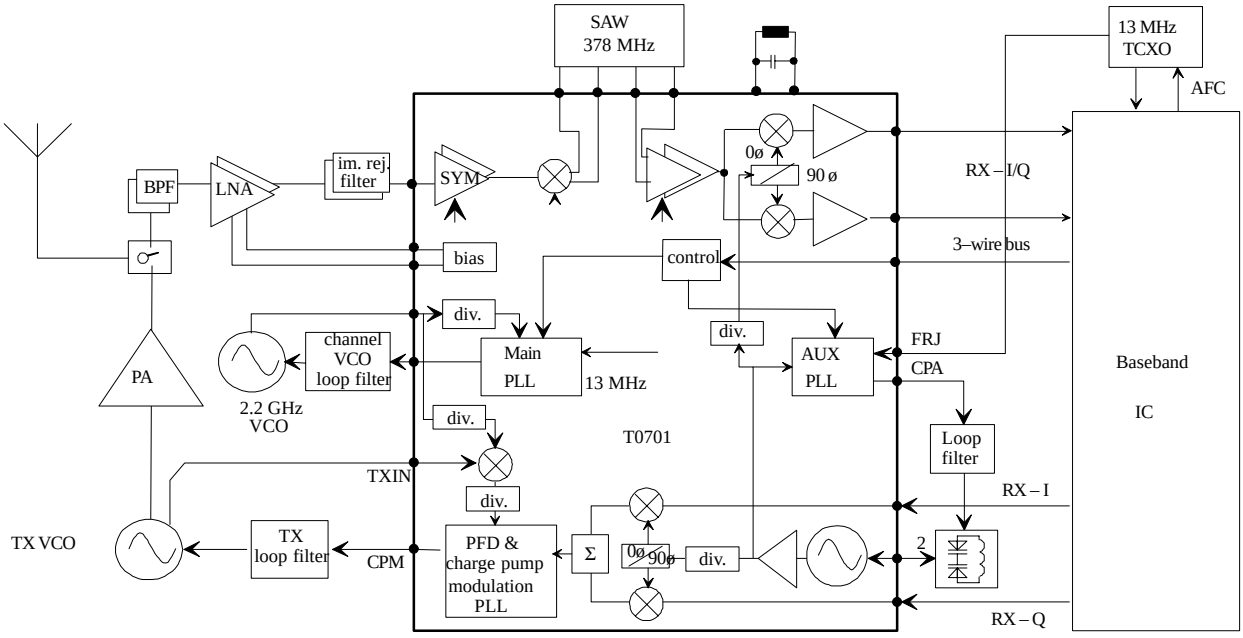


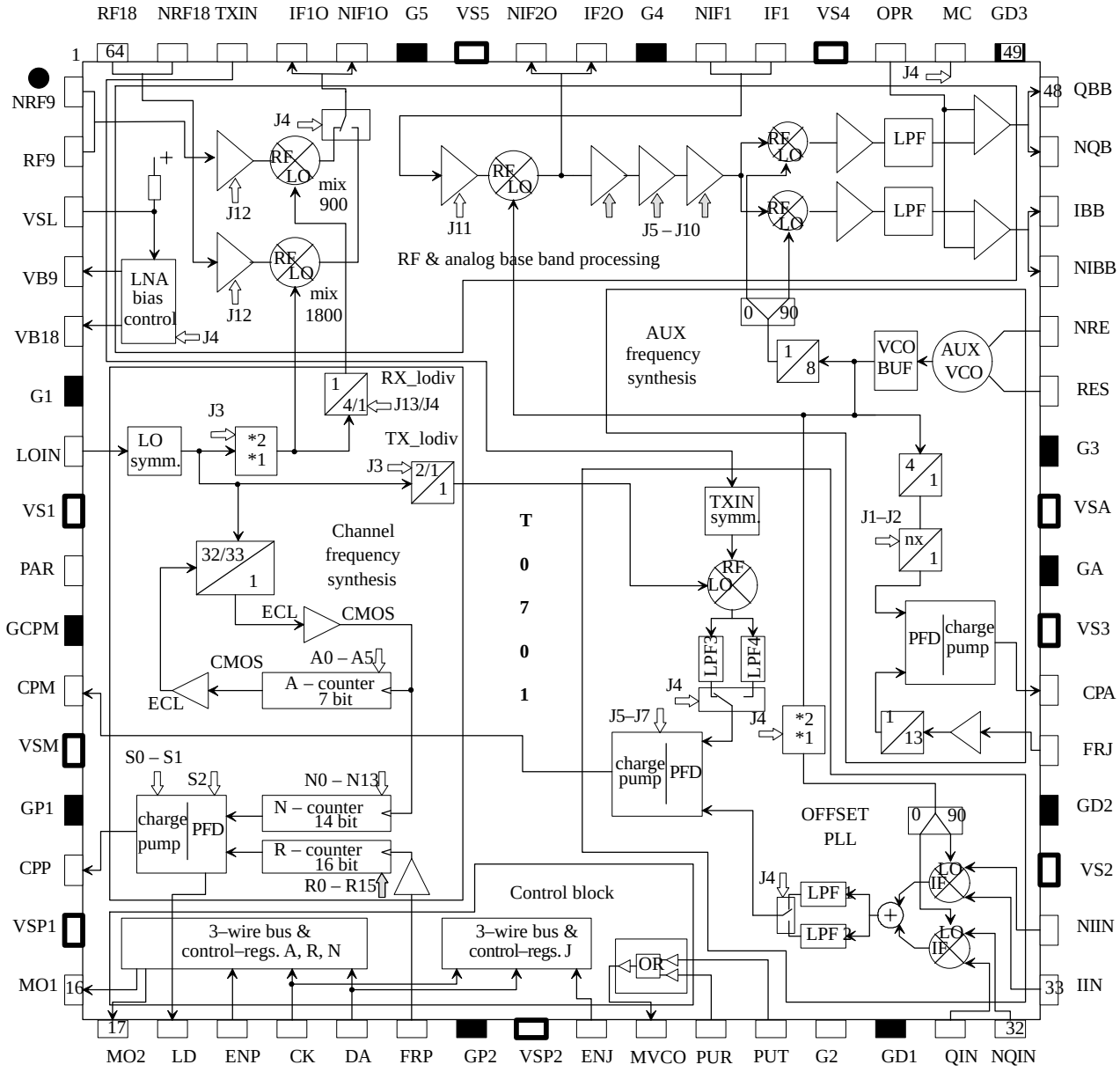
Figure 1. Block diagram

Target Specification

Ordering Information

Extended Type Number	Package	Remarks
T0701-RPQ	TQFP64	Taped and reeled
T0701-RPT	TQFP64	Tray

Detailed Block Diagram



TQFP64 input–/output positive supply negative supply (ground)

Arrows indicate programmability by a bus. e.g. J5 means: that function is controlled by J-bus bit position 5.

Figure 2. Detailed block diagram

Pin Description

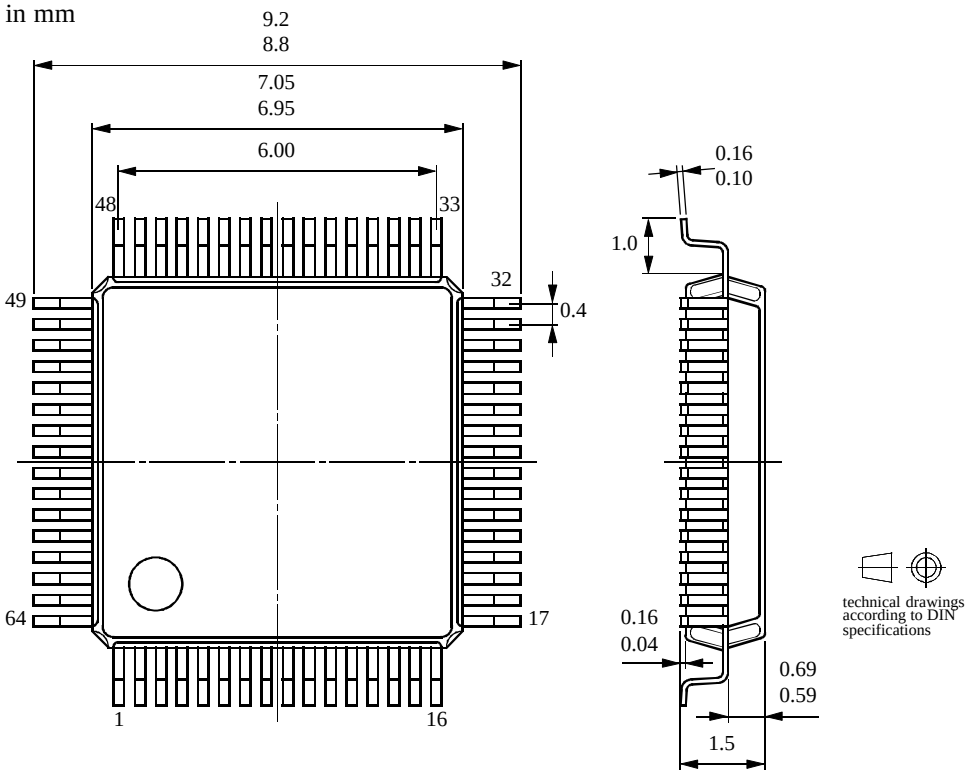
Pin	Symbol	Type	Function
1	NRF9	IB	Complementary to RF9
2	RF9	IB	RF input 900 MHz
3	VSL	O	Collector-supply LNA stages
4	VB9	O	Base-supply 900 MHz LNA
5	VB18	O	Base-supply 1800 MHz LNA
6	G1	P	GND #1, RX/TX
7	LOIN	I	LO input
8	VS1	P	Positive supply #1, RX/TX
9	PAR	I	Unbalancing I/Q modulator
10	GCPM	P	GND charge pump, offset PLL
11	CPM	O	Charge pump out, offset PLL
12	VSM	P	Positive supply offset PLL
13	GP1	P	GND #1, main PLL
14	CPP	O	Charge pump output, main PLL
15	VSP1	P	Positive supply #1, main PLL
16	MO1	O	Prog. output, main PLL
17	MO2	I/O	Input/ output, main PLL
18	LD	O	Lock detect main PLL
19	ENP	I	Enable P-bus, main PLL
20	CK	I	Clock input 3-wire bus
21	DA	I	Data input 3-wire bus
22	FRP	I	Reference frequency input, main PLL
23	GP2	P	GND #2, main PLL
24	VSP2	P	Positive supply #2, main PLL
25	ENJ	I	Enable J-bus
26	MVCO	O	Control for power VCO
27	PUR	I	Power-up RX part
28	PUT	I	Power-up TX part
29	G2	I	GND #2, RX/TX
30	GD1	P	GND #1, die pad
31	QIN	IB	Q-input, I/Q modulator
32	NQIN	IB	Complementary to QIN

Pin	Symbol	Type	Function
33	IIN	IB	I-input, I/Q modulator
34	NIIN	IB	Complementary to IIN
35	VS2	P	Positive supply #2, RX/TX
36	GD2	P	GND # 2, die pad
37	FRJ	I	Reference frequency, RX/TX
38	CPA	O	Charge pump output, AUX VCO
39	VS3	P	Positive supply #3, RX/TX
40	GA	P	GND, AUX VCO
41	VSA	P	Positive supply, AUX VCO
42	G3	P	GND #3, RX/TX
43	RES	I/O B	Resonator for AUX VCO
44	NRES	I/O B	Complementary to RES
45	NIBB	OB	Complementary to IBB
46	IBB	OB	Baseband output I channel
47	NQBB	OB	Complementary to QBB
48	QBB	OB	Baseband output Q channel
49	GD3	P	GND #3, die pad
50	MC	O	Mode control
51	OPR	I	Voltage reference for baseband amp.
52	VS4	P	Positive supply, #4, RX/TX
53	IF1	I	IF1 input
54	NIF1	P	Complementary to IF1
55	G4	P	GND #4, RX/TX
56	NIF2O	O	Complementary to IF2
57	IF2O	O	IF2 output
58	VS5	P	Positive supply #5, RX/TX
59	G5	P	GND #5, RX/TX
60	NIF1O	OB	Complementary to IF1O
61	IF1O	O	IF1 output
62	TXIN	I	Input TX down-converter
63	NRF18	IB	Complementary to RF18
64	RF18	IB	RF input 1800/ 1900 MHz

I: input
IB: input balanced
O: output
OB: output balanced
P: power

Package Information

Package TQFP 64
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.temic–semi.com

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