Features

- **Supply voltage up to 40 V**
- **R_{DSon} typ. 0.5 Ω @ 25°C, max. 1 Ω @ 150°C**
- **Up to 1.5 A output current**
- **Three half-bridge outputs formed by three high-side and three low-side drivers**
- **Capable to switch all kinds of loads such as DC motors, bulbs, resistors, capacitors and inductors**
- **No crossover current**
- **Very low quiescent current Is < 10 µA in stand-by mode vs. total temperature range**
- **Outputs short-circuit protected**
- **Overtemperature protection for each switch and overtemperature prewarning**
- **Undervoltage protection**
- **Various diagnosis functions such as shorted output, open load, overtemperature and power-supply fail**
- **Serial data interface, daisy chain capable, up to 2 MHz clock frequency**
- **SO14 power package**

Description

T6818 / T6828 are fully protected driver interfaces designed in 0.8-µm BCDMOS technology. It is used to control up to 3 different loads by a microcontroller in automotive and industrial applications.

Each of the 3 high-side and 3 low-side drivers is capable to drive currents up to 1.5 A. The drivers are internally connected to form 3 half-bridges and can be controlled separately from a standard serial data interface. Therefore all kinds of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC design especially supports the applications of H-bridges to drive DC motors.

Protection is guaranteed in terms of short-circuit conditions, overtemperature and undervoltage. Various diagnosis functions and a very low quiescent current in stand-by-mode opens a wide range of applications. Automotive qualification referring to conducted interferences, EMC protection and 2 kV ESD protection gives added value and enhanced quality for demanding up-market applications.

Ordering Information

Extended Type Number	Package	Remarks
T6818-TBS	SO14	Power package, tubed
T6818-TBQ	SO14	Power package with head slug, taped and reeled
T6828-TBS	SO14	Power package, tubed
T6828-TBQ	SO14	Power package with head slug, taped and reeled

WIRELESS & µC

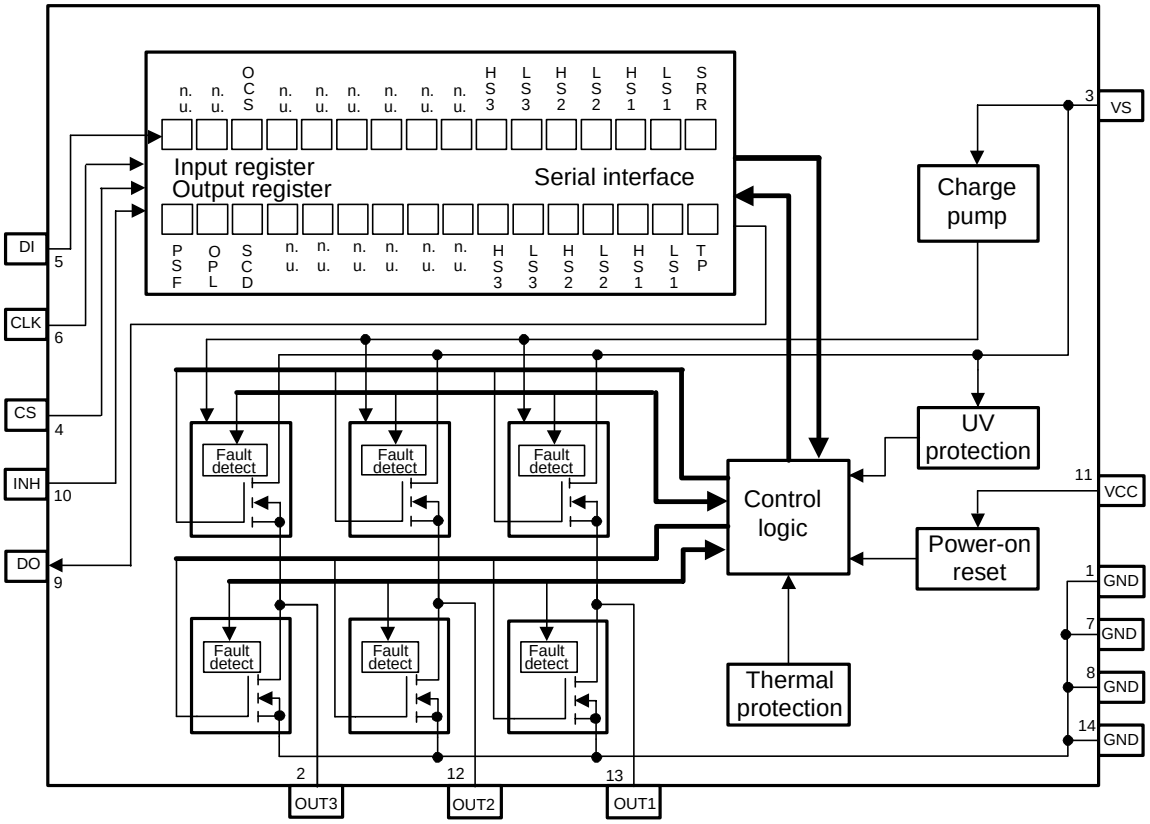
Triple Half Bridge DMOS Output Driver with Serial Input Control

T6818
T6828

Rev. A1, 07-Nov-01

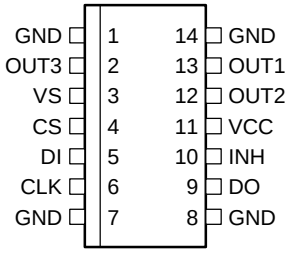
Block Diagram

Figure 1.



Pin Configuration

Figure 2.



Pin Description

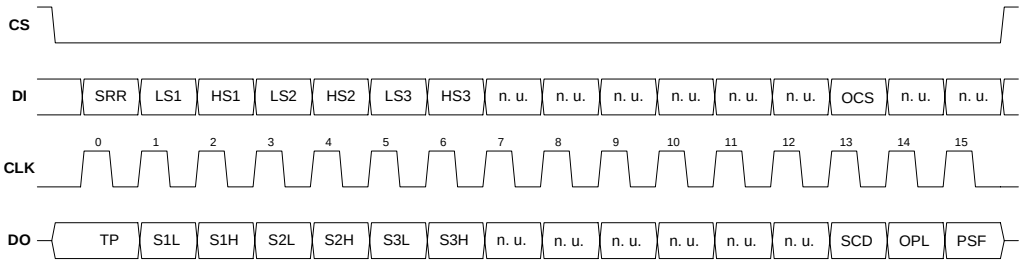
Pin	Symbol	Function
1	GND	T6818: Ground; reference potential; internal connection to Pin 7, 8 and 14; cooling tab T6828: Additional connection to heat slug
2	OUT3	Half bridge-output 3; formed by internally connected Power-MOS high-side switch 3 and low-side switch 3 with internal reverse diodes; short circuit protection; overtemperature protection; diagnosis for short and open load
3	VS	Power supply for output stages OUT1, OUT2 and OUT3, internal supply
4	CS	Chip select input; 5-V CMOS logic level input with internal pull up; low = serial communication is enabled, high = disabled
5	DI	Serial data input; 5-V CMOS logic level input with internal pull down; receives serial data from the control device; DI expects a 16-bit control word with LSB being transferred first
6	CLK	Serial clock input; 5-V CMOS logic level input with internal pull down; controls serial data input interface and internal shift register (f_{max} = 2 MHz)
7	GND	Ground; see Pin 1
8	GND	Ground; see Pin 1
9	DO	Serial data output; 5-V CMOS logic level tristate output for output (status) register data; sends 16-bit status information to the µC (LSB is transferred first); output will remain tristated, unless device is selected by CS = low, therefore, several ICs can operate on one data output line only.
10	INH	Inhibit input; 5-V logic input with internal pull down; low = stand-by, high = normal operating
11	VCC	Logic supply voltage (5V)
12	OUT2	Half bridge-output 2; see Pin 2
13	OUT1	Half bridge-output 1; see Pin 2
14	GND	Ground; see Pin 1

Functional Description

Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and are accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, Pin DO is in tristate condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Figure 3. Data transfer



Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF, OPL and SCD in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	n. u.	Not used
8	n. u.	Not used
9	n. u.	Not used
10	n. u.	Not used
11	n. u.	Not used
12	n. u.	Not used
13	OCS	Overcurrent shutdown (high = overcurrent shutdown is active)
14	n. u.	Not used
15	n. u.	Not used

Output Data Protocol

Bit	Output (Status) Register	Function
0	TP	Temperature prewarning: high = warning
1	Status LS1	high = output is on, low = output is off; not affected by SRR
2	Status HS1	high = output is on, low = output is off; not affected by SRR
3	Status LS2	Description see LS1
4	Status HS2	Description see HS1
5	Status LS3	Description see LS1
6	Status HS3	Description see HS1
7	n. u.	Not used
8	n. u.	Not used
9	n. u.	Not used
10	n. u.	Not used
11	n. u.	Not used
12	n. u.	Not used
13	SCD	Short circuit detected: set high, when at least one high-side or low-side switch is switched off by a short circuit condition. Bits 1 to 6 can be used to detect the shorted switch.
14	OPL	Open load detected: set high, when at least one active high side- or low side-switch sinks/sources a current below the open load threshold current.
15	PSF	Power-supply fail: undervoltage at Pin VS detected

After power-on reset, the input register has the following status

Bit 15	Bit 14	Bit 13 (OCS)	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
x	x	H	x	x	x	x	x	x	L	L	L	L	L	L	L

Power-Supply Fail

In case of undervoltage at Pin VS the Power-Supply Fail bit (PSF) in the output register is set and all outputs are disabled. An undervoltage condition is only detected if it occurs over the undervoltage detection delay time t_{dUV}. After the undervoltage occurred the outputs are enabled immediately. The PSF bit keeps high until it is reset by the SRR bit in the input register.

Open-Load Detection

If the current through a high side or low side switch in ON-state does not reach the open load detection threshold, the open load detection bit (OPL) in the output register is set.

The OPL bit keeps high until it is reset by the SRR bit in the input register. An open load condition is only detected if it occurs over the open load detection delay time t_{dSd}.

Overtemperature Protection

If the junction temperature at one or more switches exceeds the thermal prewarning threshold $T_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When

temperature falls below the thermal prewarning threshold $T_{jPW\ reset}$, the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word: with CS = high to low the state of TP appears at Pin DO. After the µC has read this information CS is set high and the data transfer is interrupted without affecting the state of input and output registers.

If the junction temperature at one or more switches exceeds the thermal shutdown threshold $T_{j\ switch\ off}$, all outputs are disabled and the corresponding bits in the output register are set to low. The outputs can be enabled again when the temperature falls below the thermal shutdown threshold $T_{jswitchon}$ and writing a high to the SRR bit in the input register. Thermal prewarning and shutdown threshold have hysteresis.

Short-Circuit Protection

The output currents are limited by a current regulator. If the overcurrent shutdown bit (OCS) in the input register is set, the concerned output is switched off after a short delay time (t_{dSd}) when the current exceeds the overcurrent limitation and shutdown threshold. In this case the short-circuit detection bit (SCD) is set and the corresponding status bit in the output register is set to low. For OCS = low the overcurrent shutdown is inactive. In this case the SCD bit is set also if the current exceeds the overcurrent limitation and shutdown threshold, but the outputs are not affected. By writing a high to the SRR bit in the input register the SCD bit is reset and the disabled outputs are enabled.

Inhibit

To inhibit the T6818 / T6828, switch Pin 10 (INH) to 0 V.

In this case all output switches are turned off and the data in the output register are deleted. The current consumption is reduced to less than 10 µA out of VS and less than 20 µA out of VCC. The outputs are switched to tristate. The output switches can be activated again by switching Pin 10 (INH) to 5 V which initiates an internal power-on reset.

Absolute Maximum Ratings

All values refer to GND pins

Parameter		Symbol	Value	Unit
Supply voltage	Pin 3	V_{VS}	-0.3 to 40	V
Supply voltage t<0.5s; IS>-2A	Pin 3	V_{VS}	-1	V
Logic supply voltage	Pin 11	V_{VCC}	-0.3 to 7	V
Logic input voltage	Pins 4 to 6, 10	V_{CS},V_{DI}, V_{CLK}, V_{INH}	-0.3 to V_{VCC}+0.3	V
Logic output voltage	Pin 9	V_{DO}	-0.3 to V_{VCC}+0.3	V
Input current	Pins 4 to 6, 10	I_{CS},I_{DI}, I_{CLK}, I_{INH}	-10 to +10	mA
Output current	Pin 9	I_{DO}	-10 to +10	mA
Output current	Pins 2, 12 and 13	I_{Out3}, I_{Out2}, I_{Out1}	Internal limited, see output specification	
Reverse conducting current (tpulse = 150 µs)	Pins 2, 12 and 13 towards Pin 3	I_{Out3}, I_{Out2}, I_{Out1}	17	A
Junction-temperature range		T_J	-40 to 150	°C
Storage-temperature range		T_{STG}	-55 to 150	°C

Thermal Resistance

Parameter	Test Conditions	Symbol	Value	Unit
T6818				
Junction – pin	Measured to GND Pins 1, 7, 8, 14	R_{thJP}	30	K/W
Junction – ambient		R_{thJA}	65	K/W
T6828				
Junction – pin	Measured to heat slug, GND Pins 1, 7, 8, 14	R_{thJP}	5	K/W
Junction – ambient		R_{thJA}	30	K/W

Operating Range

Parameter	Symbol	Value	Unit
Supply voltage	V_{VS}	V_{UV} [1)] to 40	V
Logic supply voltage	V_{VCC}	4.75 to 5.25	V
Logic input voltage	V_{CS},V_{DI}, V_{CLK}, V_{INH}	-0.3 to V_{VCC}	V
Serial interface clock frequency	f_{CLK}	2	MHz
Junction-temperature range	T_j	-40 to 150	°C

Noise and Surge Immunity

Parameter	Test Conditions	Value
Conducted interferences	ISO 7637–1	Level 4 [1)]
Interference suppression	VDE 0879 Part 3	Level 6
ESD (Human Body Model)	ESD S 5.1	2 kV
ESD (Machine Model)	JEDEC A115A	200 V

Electrical Characteristics

7.5 V < V_{VS} < 40 V; 4.5 V < V_{VCC} < 5.5 V; INH = High; -40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Current Consumption**								
1.1	Quiescent current (VS)	V_{VS} < 16 V, INH = low	3	I_{VS}		1	5	µA	A
1.2	Quiescent current (VCC)	4.75 V < V_{VCC} < 5.25 V, INH = low	11	I_{VCC}		15	25	µA	A
1.3	Supply current (VS)	V_{VS} <16 V normal operating, all outputs off	3	I_{VS}		4	6	mA	A
1.4	Supply current (VCC)	4.75 V < V_{VCC} < 5.25 V, normal operating	11	I_{VCC}		350	500	µA	A
2	**Undervoltage Detection, Power-On Reset**								
2.1	Power-on reset threshold		11	V_{VCC}	3.4	3.9	4.4	V	A
2.2	Powe-on reset delay time	After switching on V_{CC}		t_{dPor}	30	95	160	µs	A
2.3	Undervoltage-detection threshold	V_{CC} = 5 V	3	V_{Uv}	5.5		7.0	V	A
2.4	Undervoltage-detection hysteresis	V_{CC} = 5 V	3	ΔV_{Uv}		0.6		V	B
2.5	Undervoltage-detection delay time			t_{dUV}	10		40	µs	A
3	**Thermal Prewarning and Shutdown**								
3.1	Thermal prewarning			$T_{jPW\ set}$	120	145	170	°C	B
3.2	Thermal prewarning			$T_{jPW\ reset}$	105	130	155	°C	B
3.3	Thermal prewarning hysteresis			ΔT_{jPW}		15		°C	B
3.4	Thermal shutdown			$T_{j\ switch\ off}$	150	175	200	°C	B
3.5	Thermal shutdown			$T_{j\ switch\ on}$	135	160	185	°C	B
3.6	Thermal shutdown hysteresis			$\Delta T_{j\ switch\ off}$		15		°C	B
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Electrical Characteristics

7.5 V < V_{VS} < 40 V; 4.5 V < V_{VCC} < 5.5 V; INH = High; -40°C < T_j < 150°C; unless otherwise specified,
all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.7	Ratio thermal shutdown / thermal prewarning			$T_{j\ switch\ off}$ / $T_{jPW\ set}$	1.05	1.2			B
3.8	Ratio thermal shutdown / thermal prewarning			$T_{j\ switch\ on}$ / $T_{jPW\ reset}$	1.05	1.2			B
4	**Output Specification (OUT1-OUT3)**								
4.1	On resistance	I_{Out} = 1.5 A	2, 12, 13	$R_{DS\ On\ L}$			1	Ω	B
4.2	On resistance	I_{Out} = -1.5 A	2, 12, 13	$R_{DS\ On\ H}$			1	Ω	B
4.3	Source output leakage current	V_{Out1-3} = 0 V, output stages off	2, 12, 13	I_{Out1-3}	-15			µA	A
4.4	Sink output leakage current	V_{Out1-3} = V_{VS}, output stages off	2, 12, 13	I_{Out1-3}			300	µA	A
4.5	High-side switch reverse diode forward voltage	I_{Out} = 1.5 A	2, 12, 13	V_{Out1-3}–V_{VS}			1.3	V	A
4.6	Low-side switch reverse diode forward voltage	I_{Out} = -1.5 A	2, 12, 13	V_{Out1-3}	-1.3			V	A
4.7	Source overcurrent limitation and shutdown threshold		2, 12, 13	I_{Out1-3}	-2.5	-2	-1.5	A	A
4.8	Sink overcurrent limitation and shutdown threshold		2, 12, 13	I_{Out1-3}	1.5	2	2.5	A	A
4.9	Overcurrent shutdown delay time			t_{dSd}	10		40	µs	A
4.10	Source open-load detection threshold		2, 12, 13	I_{Out1-3}	-45	-30	-15	mA	A
4.11	Sink open-load detection threshold		2, 12, 13	I_{Out1-3}	15	30	45	mA	A
4.12	Open-load detection delay time			t_{dSd}	200		600	µs	A
4.13	Source output switch on delay [1)]	V_{VS} = 13 V, R_{Load} = 30 Ω		t_{don}		5	15	µs	A
4.14	Sink output switch on delay [1)]	V_{VS} = 13 V, R_{Load} = 30 Ω		t_{don}		15	25	µs	A
4.15	Source output switch off delay [1)]	V_{VS} = 13 V, R_{Load} = 30 Ω		t_{doff}		5	15	µs	A
4.16	Sink output switch off delay [1)]	V_{VS} = 13 V, R_{Load} = 30 Ω		t_{doff}		1	2	µs	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Electrical Characteristics

7.5 V < V_{VS} < 40 V; 4.5 V < V_{VCC} < 5.5 V; INH = High; -40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.17	Dead time between corresponding high- and low-side switches	V_{VS} = 13 V, R_{Load} = 30 Ω		t_{don} -t_{doff}	1			µs	B
5	**Logic Inputs DI, CLK, CS, INH**								
5.1	Input voltage low-level threshold		4-6, 10	V_{IL}	0.3 × V_{VCC}			V	A
5.2	Input voltage high-level threshold		4-6, 10	V_{IH}			0.7 x V_{VCC}	V	A
5.3	Hysteresis of input voltage		4-6, 10	ΔV_I	50		500	mV	B
5.4	Pull-down current Pin DI, CLK, INH	V_{DI}, $V_{CLK,}$ V_{INH} = V_{CC}	5, 6, 10	I_{PD}	10		60	µA	A
5.5	Pull-up current Pin CS	V_{CS} = 0 V	4	I_{PU}	-50		-10	µA	A
6	**Serial Interface – Logic Output DO**								
6.2	Output-voltage high level	I_{OL} = -2 mA	9	V_{DOH}	V_{VCC}- 0.7 V			V	A
6.3	Leakage current (tristate)	V_{CS} = V_{CC} 0V < V_{DO} < V_{VCC}	9	I_{DO}	-10		10	µA	A
7	**Inhibit Input - Timing**								
7.1	Standby setup time			$t_{lINHsethl}$			100	µs	A
7.2	Standby setup time			$t_{lINHsetlh}$			100	µs	A

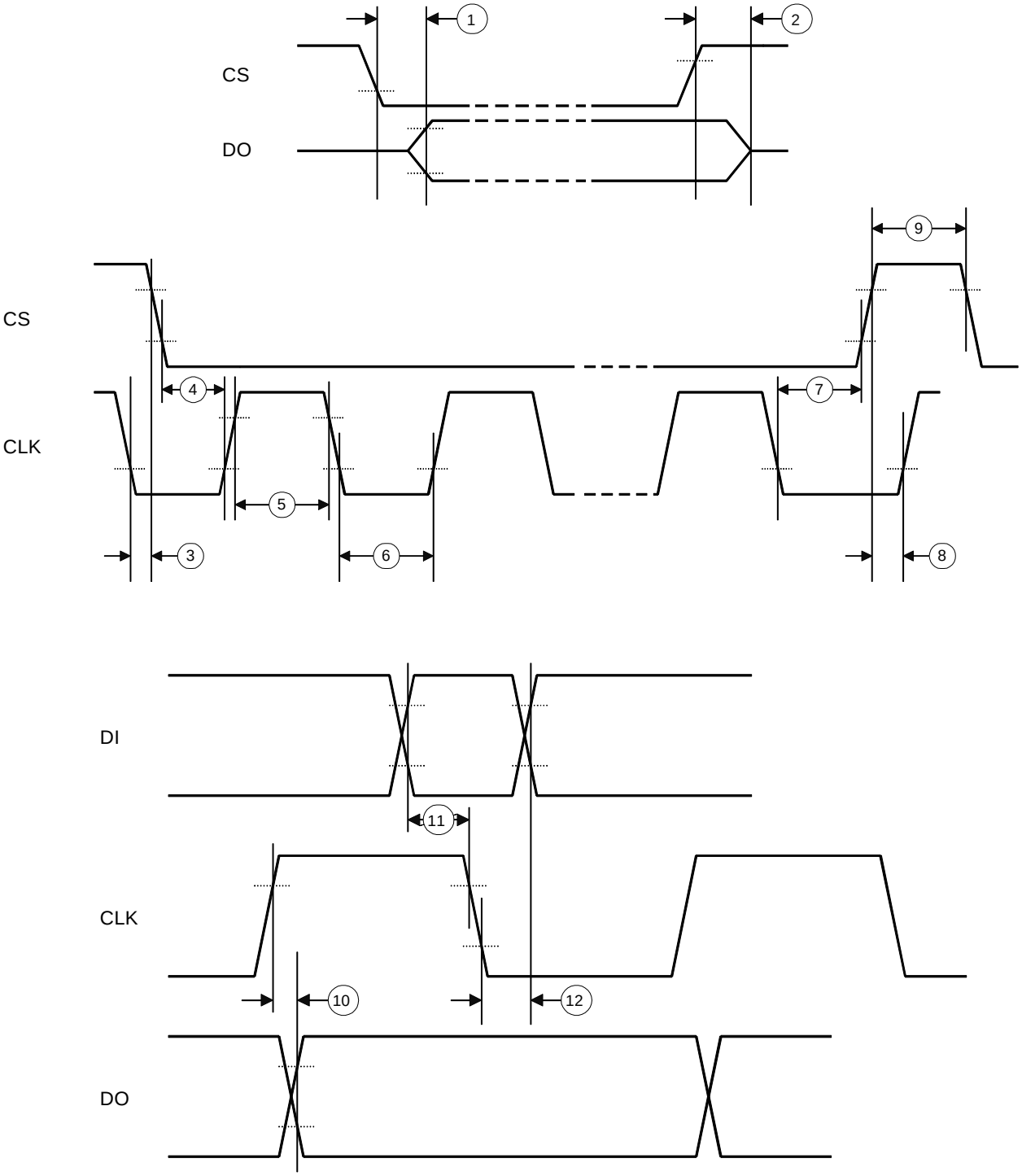
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Delay time between rising edge of CS after data transmission and switch on output stages to 90% of final level. Device not in stand-by for t >1ms

Serial Interface – Timing

Parameters	Test Conditions	Timing Chart No.	Symbol	Min.	Typ.	Max.	Unit
DO enable after CS falling edge	C_{DO} = 100 pF	1	t_{ENDO}			200	ns
DO disable after CS rising edge	C_{DO} = 100 pF	2	t_{DISDO}			200	ns
DO fall time	C_{DO} = 100 pF	-	t_{DOf}			100	ns
DO rise time	C_{DO} = 100 pF	-	t_{DOr}			100	ns
DO valid time	C_{DO} = 100 pF	10	t_{DOVal}			200	ns
CS setup time		4	$t_{CSSethl}$	225			ns
CS setup time		8	$t_{CSSetlh}$	225			ns
CS high time		9	t_{CSh}	500			ns
CLK high time		5	t_{CLKh}	225			ns
CLK low time		6	t_{CLKl}	225			ns
CLK period time		-	t_{CLKp}	500			ns
CLK setup time		7	$t_{CLKSethl}$	225			ns
CLK setup time		3	$t_{CLKSetlh}$	225			ns
DI setup time		11	t_{DIset}	40			ns
DI hold time		12	t_{DIHold}	40			ns

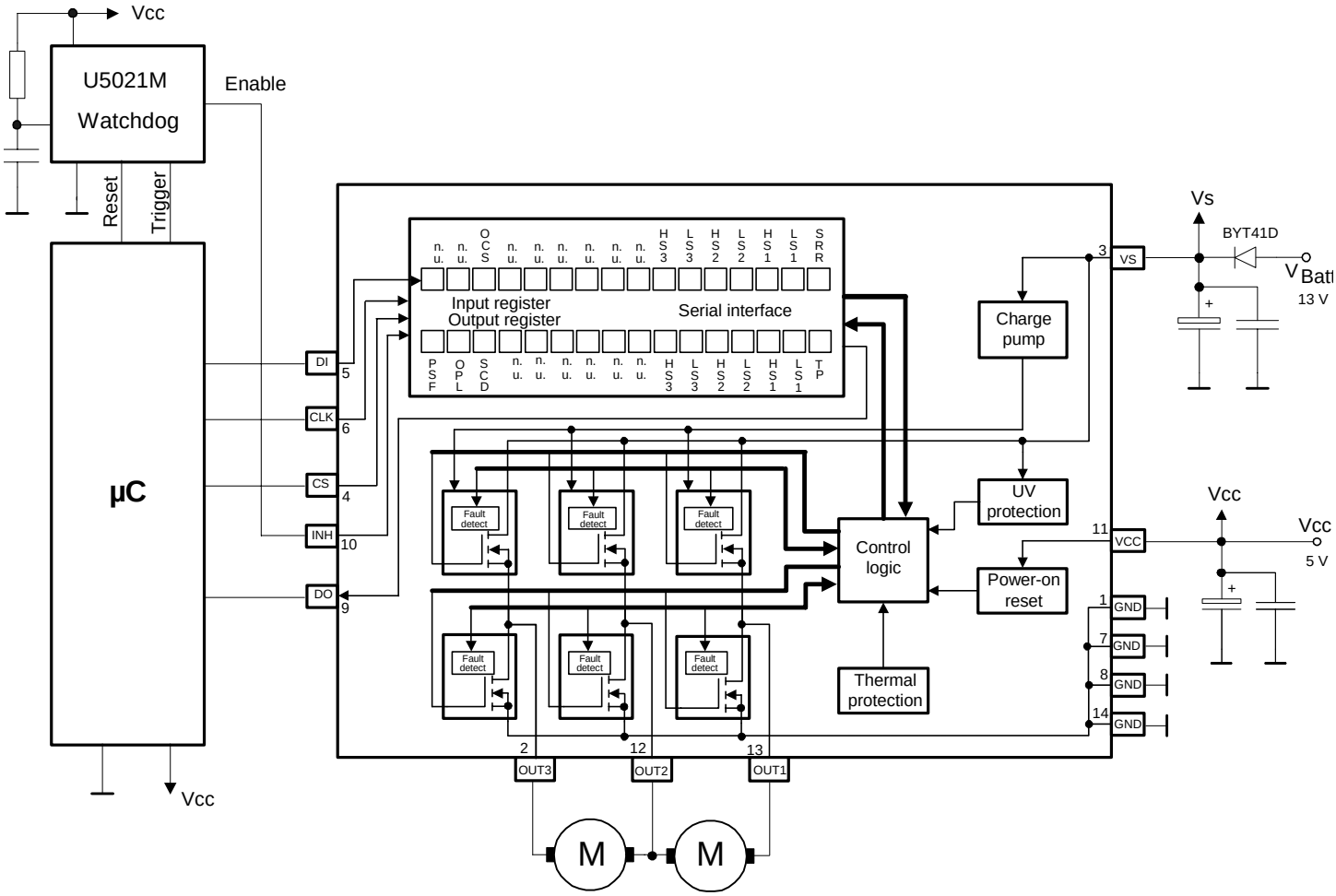
Figure 4. Serial interface timing with chart numbers



Inputs DI, CLK, CS: High level = 0.7 x $V_{CC,}$ low level = 0.3 x V_{CC}
Output DO: High level = 0.8 x V_{CC}, low level = 0.2 x V_{CC}

Application Circuit

Figure 5.



Application Notes

It is strongly recommended to connect the blocking capacitors at V_{CC} and V_S as close as possible to the power supply and GND pins.

Recommended value for capacitors at V_S:

Electrolytic capacitor C > 22 µF in parallel with a ceramic capacitor C = 100 nF. Value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current I_{Outzx} (see Absolute Maximum Ratings).

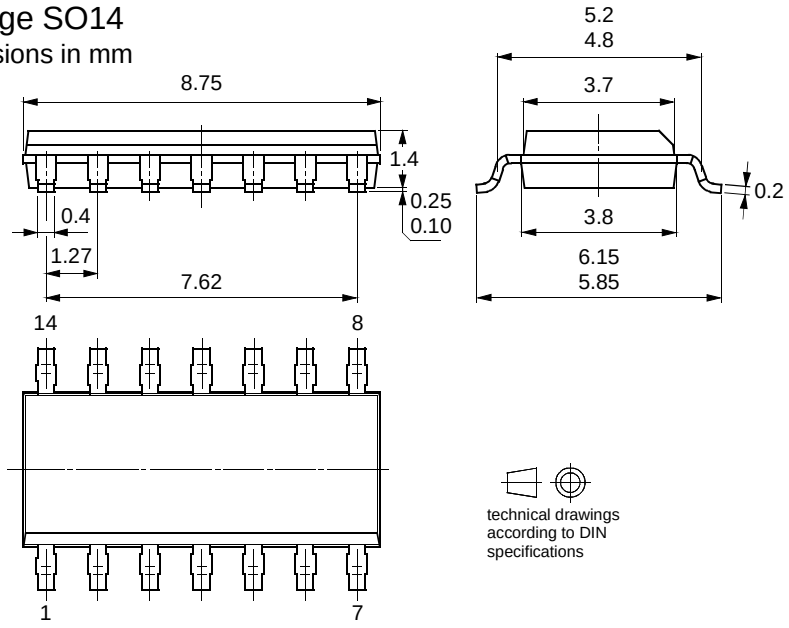
Recommended value for capacitors at V_{CC}:

Electrolytic capacitor C > 10 µF in parallel with a ceramic capacitor C = 100 nF.

To reduce thermal resistance it is recommended to place cooling areas on the PCB as close as possible to GND pins.

Package Information

Package SO14
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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Data sheets can also be retrieved fron the Internet: http://www.atmel-wm.com

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