Modulation PLL for GSM, DCS and PCS Systems

Description

The U2894B is a monolithic integrated circuit manufactured using TEMIC Semiconductors' advanced silicon bipolar UHF5S technology. The device integrates a mixer, an I/Q modulator, a phase-frequency detector (PFD) with two synchronous programmable dividers, and a charge pump. The U2894B is designed for cellular phones such as GSM900, DCS1800, and PCS1900, applying a transmitter architecture at which the VCO operates at the TX output frequency. No duplexer is needed since the out-of-band noise is very low. The U2894B exhibits low power consumption. Broadband operation provides high flexibility for multi-band frequency mappings. The IC is available in a shrinked small-outline 28-pin package (SSO28).
The U2893B offers the same functionality with other divider ratios.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Supply-voltage range 2.7 V to 5.5 V
- Current consumption 50 mA
- Power-down functions
- High-speed PFD and charge pump (CP)
- Small CP saturation voltages (0.5/0.6 V)
- Programmable dividers and CP polarity
- Low-current standby mode

Benefits

- Novel TX architecture saves filter costs
- Extended battery operating time without duplexer
- Less board space (few external components)
- VCO control without voltage doubler
- Small SSO28 package
- One device for all GSM bands

Block Diagram

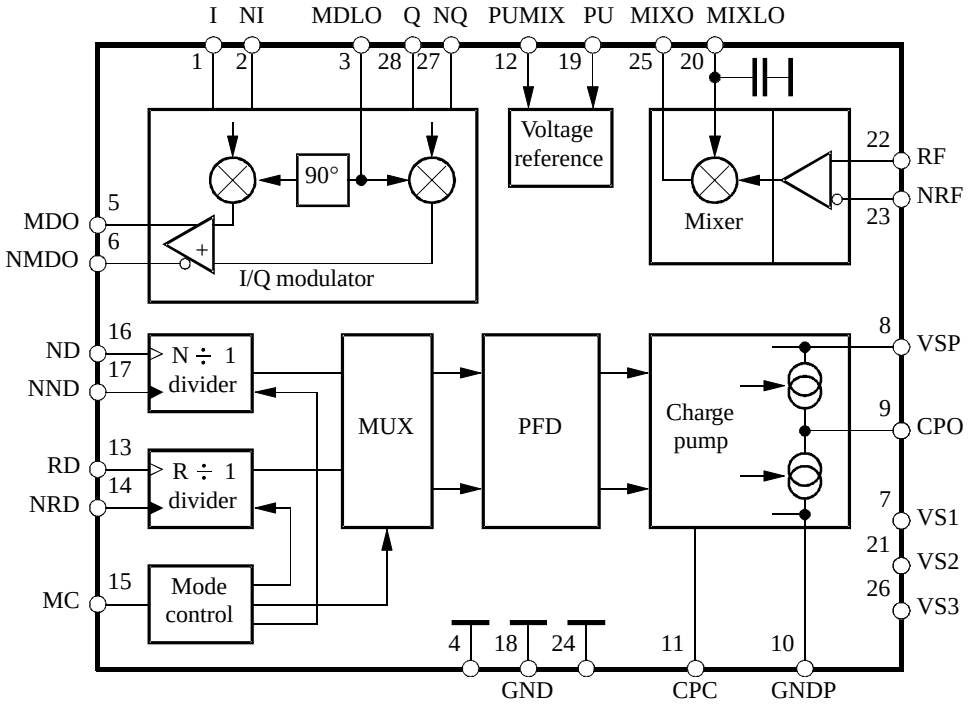


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2894B-AFS	SSO28	Tube
U2894B-AFSG3	SSO28	Taped and reeled

Pin Description

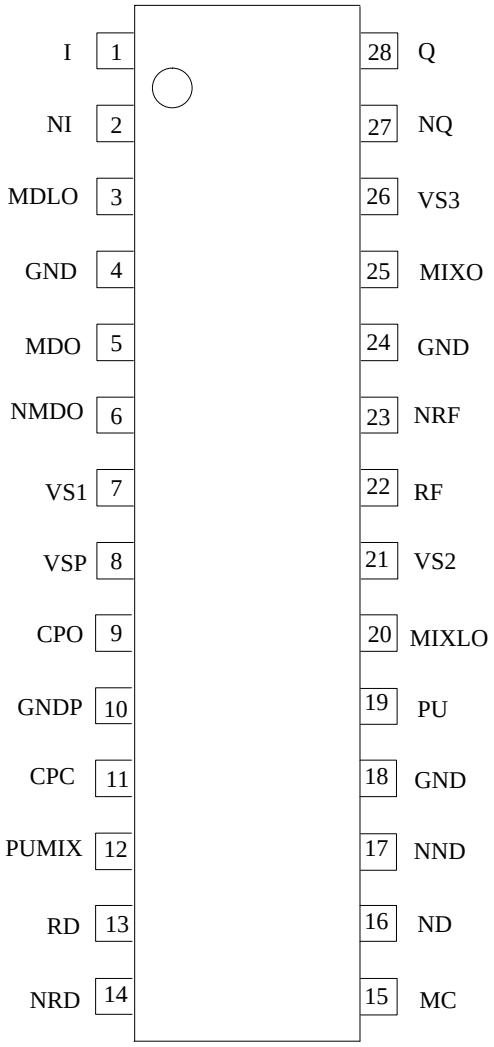


Figure 2. Pinning

Pin	Symbol	Function
1	I	In-phase baseband input
2	NI	Complementary to I
3	MDLO	I/Q-modulator LO input
4	GND [1)]	Negative supply
5	MDO	I/Q-modulator output
6	NMDO	Complementary to MDO
7	VS1 [3)]	Positive supply (I/Q MOD)
8	VSP	Pos. supply charge pump
9	CPO	Charge-pump output
10	GNDP [2)]	Neg. supply charge pump
11	CPC	Charge-pump current control (input)
12	PUMIX	Power-up, mixer only
13	RD	R-divider input
14	NRD	Complementary to RD
15	MC	Mode control
16	ND	N-divider input
17	NND	Complementary to ND
18	GND [1)]	Negative supply
19	PU	Power-up, whole chip except mixer
20	MIXLO	Mixer LO input
21	VS2 [3)]	Positive supply (MISC.)
22	RF	Mixer RF-input
23	NRF	Complementary to RF
24	GND [1)]	Negative supply
25	MIXO	Mixer output
26	VS3 [3)]	Positive supply (mixer)
27	NQ	Complementary to Q
28	Q	Quad.-phase baseband input

1) All GND pins must be connected to GND potential. No DC voltage between GND pins!

2) Max. voltage between GNDP and GND pins $\leq$ 200 mV

3) The maximum permissible voltage difference between pins VS1, VS2 and VS3 is $\leq$ 200 mV.

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage VS1, VS2, VS3	$V_{VS\#}$	≤ V_{VSP}	V
Supply voltage charge pump VSP	V_{VSP}	5.5	V
Voltage at any input	$V_{Vi\#}$	–0.5 ≤ V_{VS} +0.5 ≤ 5.5	V
Current at any input / output pin except CPC	$\mid I_{I\#} \mid$ $\mid I_{O\#} \mid$	2	mA
CPC output currents	$\mid I_{CPC} \mid$	5	mA
Ambient temperature	T_{amb}	–20 to +85	°C
Storage temperature	T_{stg}	–40 to +125	°C

Operating Range

Parameters	Symbol	Value	Unit
Supply voltage	$V_{VS\#}$, V_{VSP}	2.7 to 5.5	V
Ambient temperature	T_{amb}	–20 to +85	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO28	R_{thJA}	130	K/W

Electrical Characteristics

T_{amb} = 25°C, V_S = 2.7 to 5.5 V

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
DC supply						
Supply voltages VS#	V_{VS1} = V_{VS2} = V_{VS3}	$V_{VS\#}$	2.7		5.5	V
Supply voltage VSP		V_{VSP}	$V_{VS\#}$ – 0.3		5.5	V
Supply current I_{VS1}	Active (V_{PU} = VS)	I_{VS1A}		18	23	mA
	Standby (V_{PU} = 0)	I_{VS1Y}			20	µA
Supply current I_{VS2}	Active (V_{PU} = VS)	I_{VS2A}		17	22	mA
	Standby (V_{PU} = 0)	I_{VS2Y}			20	µA
Supply current I_{VS3}	Active (V_{PUMIX} = VS)	I_{VS3A}		13	17	mA
	Standby (V_{PUMIX} = 0)	I_{VS3Y}			30	µA
Supply current I_{VSP} 1)	Active (V_{PU} = VS, CPC open)	I_{VSPA}		1.4	1.8	mA
	Standby (V_{PU} = 0)	I_{VSPY}			20	µA
N & R divider inputs ND, NND & RD, NRD						
N:1 divider frequency	50-Ω source	f_{ND}	100		600	MHz
R:1 divider frequency	50-Ω source	f_{RD}	100		600	MHz
Input impedance	Active & standby	Z_{RD}, Z_{ND}	1 kΩ		2 pF	–
Input sensitivity	50-Ω source	V_{RD}, V_{ND}	20		200	mV_{rms}

1) Mean value measured with F_{ND} = 151 MHz, F_{RD} = 150 MHz, current vs. time, figure 3.

Electrical Characteristics (continued)

T_{amb} = 25°C, V_S = 2.7 to 5.5 V

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Phase-frequency detector (PFD)						
PFD operation	f_{ND} = 450 MHz, N = 2 f_{RD} = 450 MHz, R = 2	f_{PFD}	50		225	MHz
Frequency comparison only [3]	f_{ND} = 600 MHz, N = 2 f_{RD} = 450 MHz, R = 2	f_{FD}			300	MHz
I/Q modulator baseband inputs I, NI & Q, NQ						
DC voltage	Referred to GND	V_I, V_{NI}, V_Q, V_{NQ}	1.35	VS1/2	VS1/2 + 0.1	V
MD_IQ	Frequency range	f_{IO}	DC		1	MHz
AC voltage [4]	Referred to GND	AC_I, AC_{NI}, AC_Q, AC_{NQ}		200		mV_{pp}
	Differential (preferres)	AC_{DI}, AC_{DQ}		400		mV_{pp}
I/Q modulator LO input MDLO						
MDLO	Frequency range	f_{MDLO}	50		450	MHz
Input impedance	Active & standby	Z_{MDLO}		250		Ω
Input level	50-Ω source	P_{MDLO}	–11	–8	–5	dBm
I/Q modulator outputs MDO, NMDO						
DC current	V_{MDO}, V_{NMDO} = VS	I_{MDO}, I_{NMDO}		2.4		mA
Voltage compliance	V_{MDO}, V_{NMDO} = VC	VC_{MDO}, VC_{NMDO}	V_S – 0.7		5.5	V
MDO output level (differential)	500 Ω to VS [5]	P_{MDO}	120		150	mV_{rms}
Carrier suppression [5]		CS_{MDO}	–32	–35		dBc
Sideband suppression [5]		SS_{MDO}	–35	–40		dBc
IF spurious [5]	$f_{LO} \pm 3 \times f_{mod}$	SP_{MDO}		–50	–45	dBc
Noise [5]	@ 400 kHz off carrier	N_{MDO}			–115	dBc/Hz
Frequency range		f_{MDO}	50		450	MHz
Mixer (900 MHz)						
RF input level	900 MHz	$P9_{RF}$	–23		–17	dBm
LO-spurious at RF/NRF port	@ $P9_{MIXLO}$ = –10 dBm @ $P9_{RF}$ = –15 dBm	$SP9_{RF}$			–40	dBm
MIXLO input level	0.05 to 2 GHz	$P9_{MIXLO}$	–22		–12	dBm
MIXO (100-Ω load)	Frequency range	f_{MIXO}	50		450	MHz
Output level [6]	@ $P9_{MIXLO}$ = –15 dBm	$P9_{MIXO}$		70		mV_{rms}
Carrier suppression	@ $P9_{MIXLO}$ = –15 dBm	$CS9_{MIXO}$	–20			dBc

3) PFD can be used as a frequency comparator until 300 MHz for loop acquisition

4) Single-ended operation (complementary baseband input is AC-grounded) leads to reduced linearity (degrading suppression of odd harmonics)

5) With typical drive levels at MDLO- & I/Q-inputs

6) –1 dB compression point (CP-1)

Electrical Characteristics (continued)

T_{amb} = 25°C, V_S = 2.7 to 5.5 V

Parameters	Test Conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Mixer (1900 MHz)						
RF input level	0.5 to 2 GHz	$P19_{RF}$	–23		–17	dBm
LO-spurious at RF/NRF ports	@ $P19_{MIXLO}$ = –10 dBm @ $P19_{RF}$ = –15 dBm	$SP19_{RF}$			–40	dBm
MIXLO input level	0.05 to 2 GHz	$P19_{MIXLO}$	–22		–12	dBm
MIXO (100 Ω load)						
Output level [6]	@ $P19_{MIXLO}$ = –17 dBm	$P19_{MIXO}$		55		mVrms
Carrier suppression	@ $P19_{MIXLO}$ = –17 dBm	$CS19_{MIXO}$	–20			dBc
Charge-pump output CPO (V_{VSP} = 5 V; V_{CPO} = 2.5 V)						
Pump-current pulse	CPC open for DC	$\lvert I_{CPO} \rvert$	0.7	1	1.3	mA
	R_{CPC} = 2.2 kΩ [7]	$\lvert I_{CPO\,2} \rvert$	1.4	2	2.6	mA
	P_{CPC} = 680 Ω [7]	$\lvert I_{CPO\_4} \rvert$	3	4	5	mA
TK pump current		$Tk\_\lvert I_{CPC} \rvert$			15	%/100°K
Mismatch source / sink current	$(I_{CPOSI} - I_{CPOSO})/I_{CPOSI}$ $I_{CPOSO} = I_{sourc}$ $I_{CPOSI} = I_{sink}$	M_{ICPO}			0.1	–
Sensivity to VSP	$\lvert\frac{\Delta I_{CPO}}{I_{CPO}}\rvert \;/\; \lvert\frac{\Delta VSP}{VSP}\rvert$	S_{ICPO}			0.1	–
V_{CPO} voltage range		V_{CPO}	0.5		V_{VSP}–0.6	V
Charge-pump control input CPC						
Compensation capacitor		C_{CPC}	500			pF
Short-circuit current [8]	CPC grounded	$\lvert I_{CPCK} \rvert$	1.6			mA
Mode control						
Sink current	V_{MC} = VS	I_{MC}		60		µA
Power-up input PU (power-up for all functions, except mixer)						
Settling time	Output power within 10% of steady state values	S_{PU}		5	10	µs
High level	Active	V_{PUH}	2.4			V
Low level	Standby	V_{PUL}	0		0.4	V
High-level current	Active, V_{PUH} = 2.7 V	I_{PUH}			0.26	mA
Low-level current	Standby, V_{PUL} = 0.4 V	I_{PUL}	–1		20	µA
Power-up input PUMIX (power-up for mixer only)						
Settling time	Output power within 10% of steady state values	t_{setl}		5	10	µs
High level	Active	V_{PUMIXH}	2.4		V_{S2}	V
Low level	Standby	V_{PUMIXL}	0		0.4	V
High-level current	Active, V_{PUMIXH} = 2.7 V	I_{PUMIXH}			0.26	mA
Low-level current	Standby, V_{PUMIXL} = 0.4 V	I_{PUMIXL}	–1		20	µA

6) – 1 dB compression point (CP – 1)

7) R_{CPC}: external resistor to GND for charge–pump current control

8) See figure 7.

Supply Current of the Charge Pump I_{VSP} vs. Time

Due to the pulsed operation of the charge pump, the current into the charge-pump supply Pin VSP is not constant. Depending on I (see figure 7) and the phase difference at the phase detector inputs, the current I_{VSP} over time varies. Basically, the total current is the sum of the quiescent current, the charge-/discharge current, and – after each phase comparison cycle – a current spike (see figure 3).

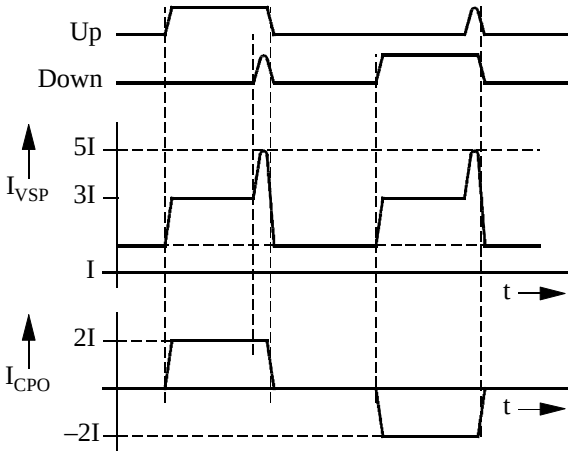


Figure 3. Supply current of the charge pump = f(t)

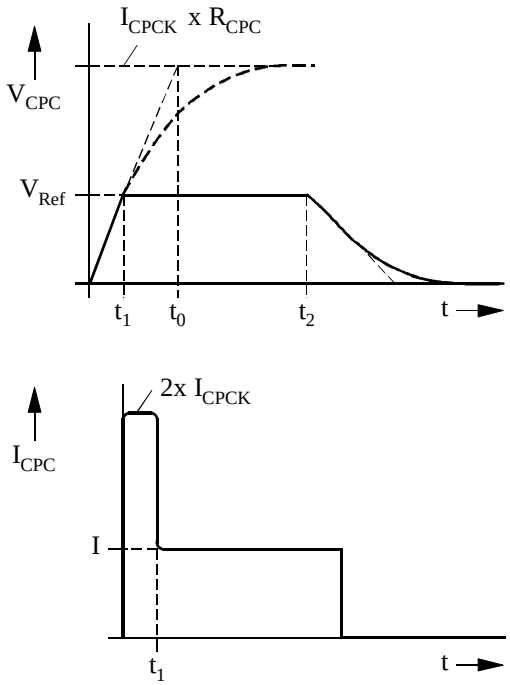
Internal current, I, $|I_{CPC}|$ and I_{CPC} vs. R_{CPC}

R_{CPC}	I	$\|I_{CPCO}\|$	I_{CPC}
CPC open	0.5 mA	1 mA	0
2.2 kΩ	1.0 mA	2 mA	–0.5 mA
680 Ω	2.0 mA	4 mA	–1.5 mA

(typical values)

Initial Charge-Pump Current after Power-Up

Due to stability reasons, the reference current generator for the charge pump needs an external capacitor (>500 pF from CPC to GND). After power-up, only the on-chip generated current $I = I_{CPCK}$ is available for charging the external capacitor. Due to the charge pump's architecture, the charge-pump current will be $2 \times I = 2 \times I_{CPCK}$ until the voltage on CPC has reached the reference voltage (1.1 V). The following figures illustrate this behavior.



Time t_1 can be calculated as $t_1 \approx (1.1\ V \times C_{CPC})/I_{CPCK}$
e.g., C_{CPC} = 1 nF, I_{CPCK} = 2.7 mA → $t_1 \approx$ 0.4 µs.
Time t_2 can be calculated as $t_2 \approx (R_{CPC}/2200\ \Omega) \times C_{CPC}$
e.g., C_{CPC} = 1 nF, R_{CPC} = 2200 Ω → $t_2 \approx$ 1.1 µs

Figure 4.

The behavior of $|I_{CPO}|$ after power-up can be very advantageous for a fast settling of the loop. By using larger capacitors (>1 nF), an even longer period with maximum charge-pump current is possible.

Ramp-up time for the internal band gap reference is about 1 µs. This time has to be added to the times calculated for the charge-pump reference.

Mode Selection

The device can be programmed to different modes via an external resistor RMODE (including short, open) from Pin MC to VS2. The mode is distinguished from specific N-, R-divider ratios, and the polarity of the charge-pump current.

Mode Selection		N-Divider	R-Divider	CPO Current Polarity [4]		Application
Mode	Resistance between Pin MC and Pin VS2			$f_N < f_R$ [1]	$f_N > f_R$ [1]	
1	0 (<50 Ω)	1:1	1:1	Sink	Source	
2	2.7 kΩ (±5%)	1:1	1:1	Source	Sink	
3	10 kΩ (±5%)	1:1	2:1	Source	Sink	
4	36 kΩ (±5%)	2:1	2:1	Source	Sink	PCN/PCS [2]
5	∞ (>1 MΩ)	2:1	2:1	Sink	Source	GSM [3]

1) Frequencies referred to PFD input
2) LO frequencies below VCO frequency
3) LO frequencies above VCO frequency
4) Sink current into Pin CPO. Source: current out from Pin CPO.

Equivalent Circuits at the IC's Pins

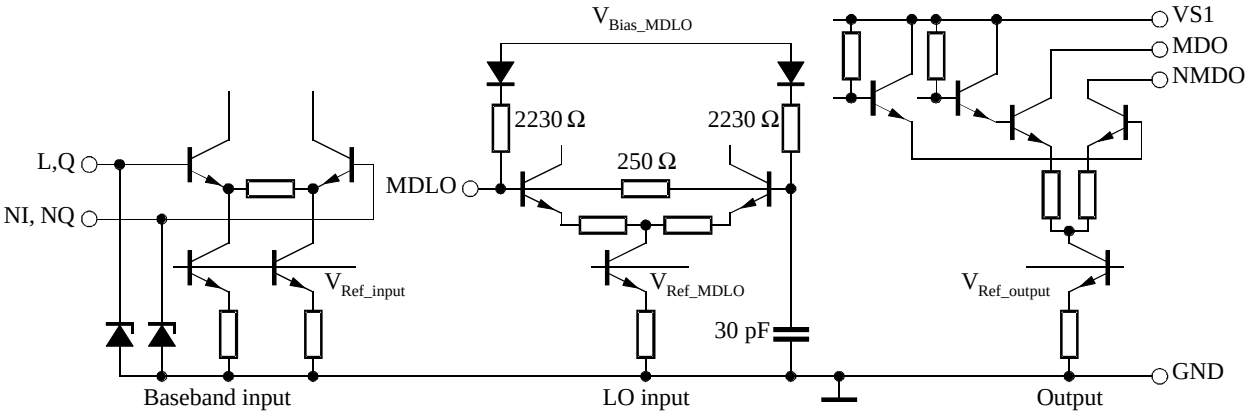


Figure 5. I/Q modulator

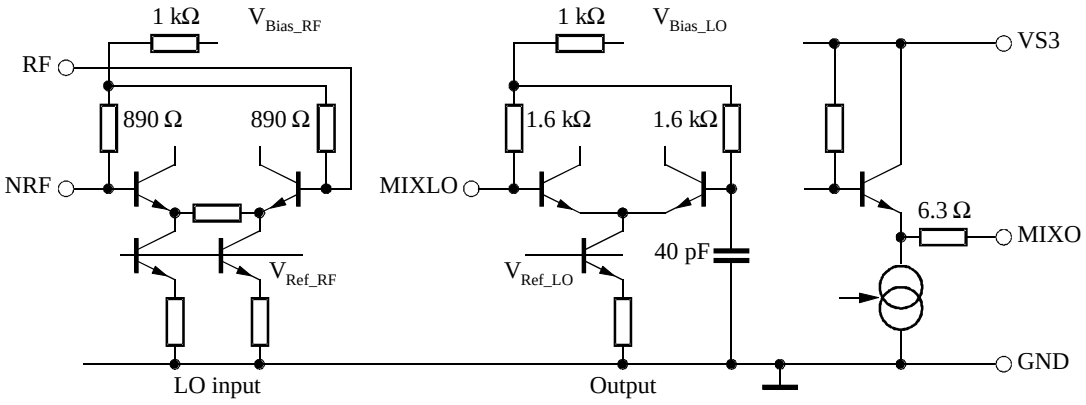


Figure 6. Mixer

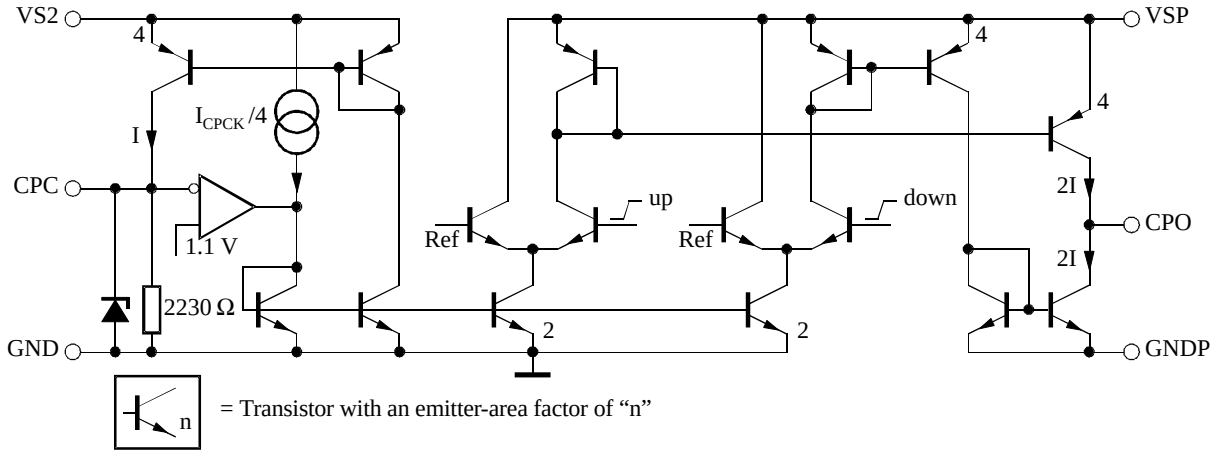


Figure 7. Charge pump

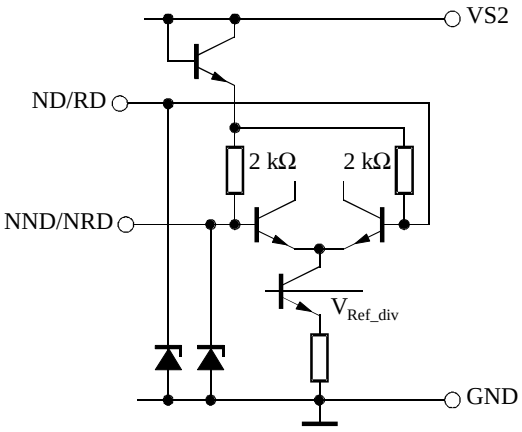


Figure 8. Dividers

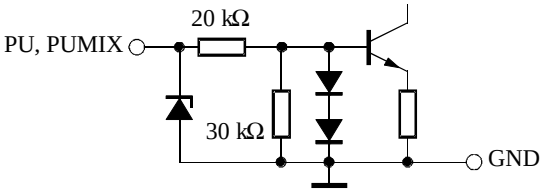


Figure 9. Power-up

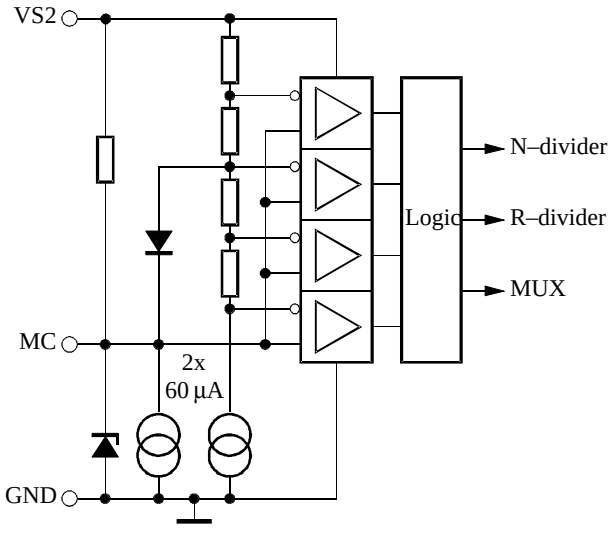
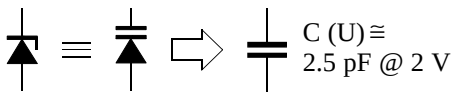


Figure 10. Mode control



C (U) is a non-linear junction capacitance

Figure 11. ESD-protection diodes

Test Circuit

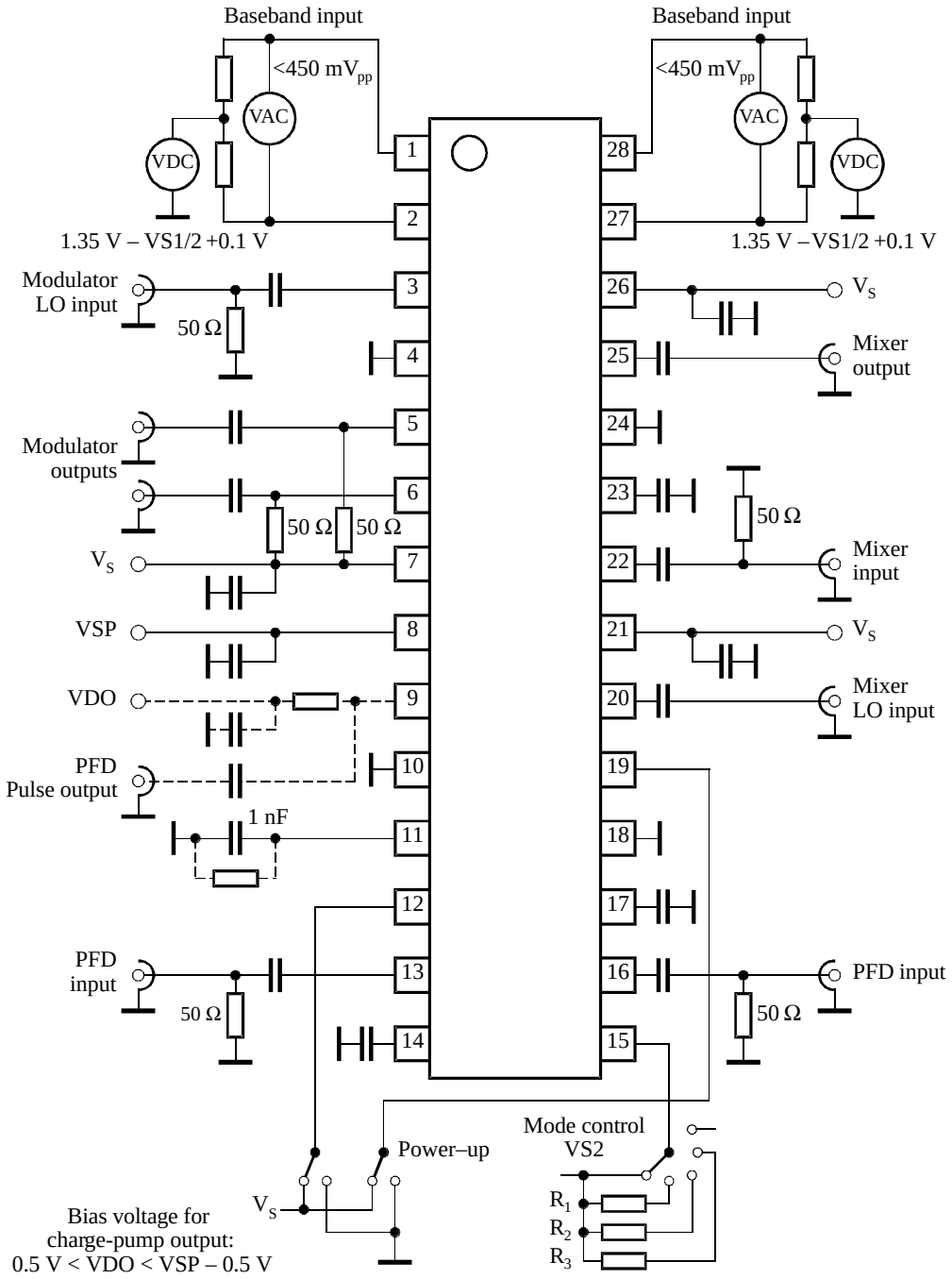


Figure 12. Test circuit

Application Hints

Interfacing

For some baseband ICs it may be necessary to reduce the I/Q voltage swing so that it can be handled by the U2894B. In those cases, the following circuitry can be used.

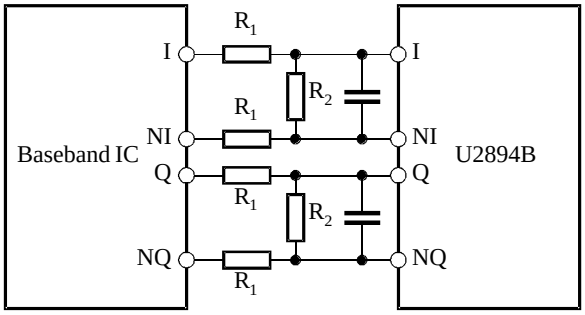


Figure 13. Interfacing the U2894B to I/Q baseband circuits

Due to a possible current offset in the differential baseband inputs of the U2894B the best values for the carrier suppression of the I/Q modulator can be achieved with voltage driven I/NI-, and Q/NQ-inputs. A value of $R_{source} = R2/2 \times R_S \leq 1.5\ k\Omega$ should be realized. R_S is the sum of R1 (above drawing) and the output resistance of the baseband IC.

Charge-Pump Current Programming

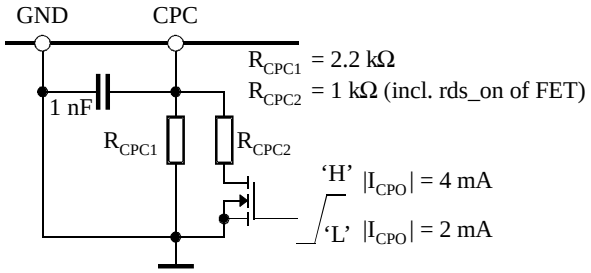


Figure 14. Programming the charge-pump current

Mode Control

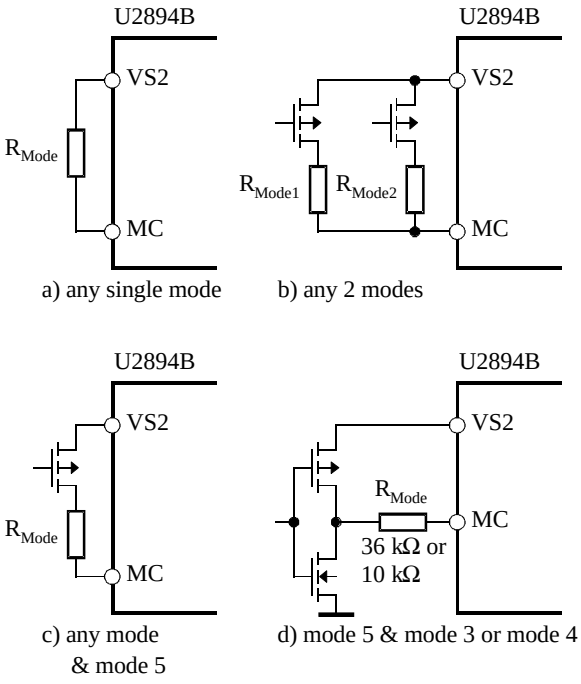


Figure 15. Application examples for programming different modes

Application Circuit for DCS1800 (1710 – 1785 MHz)

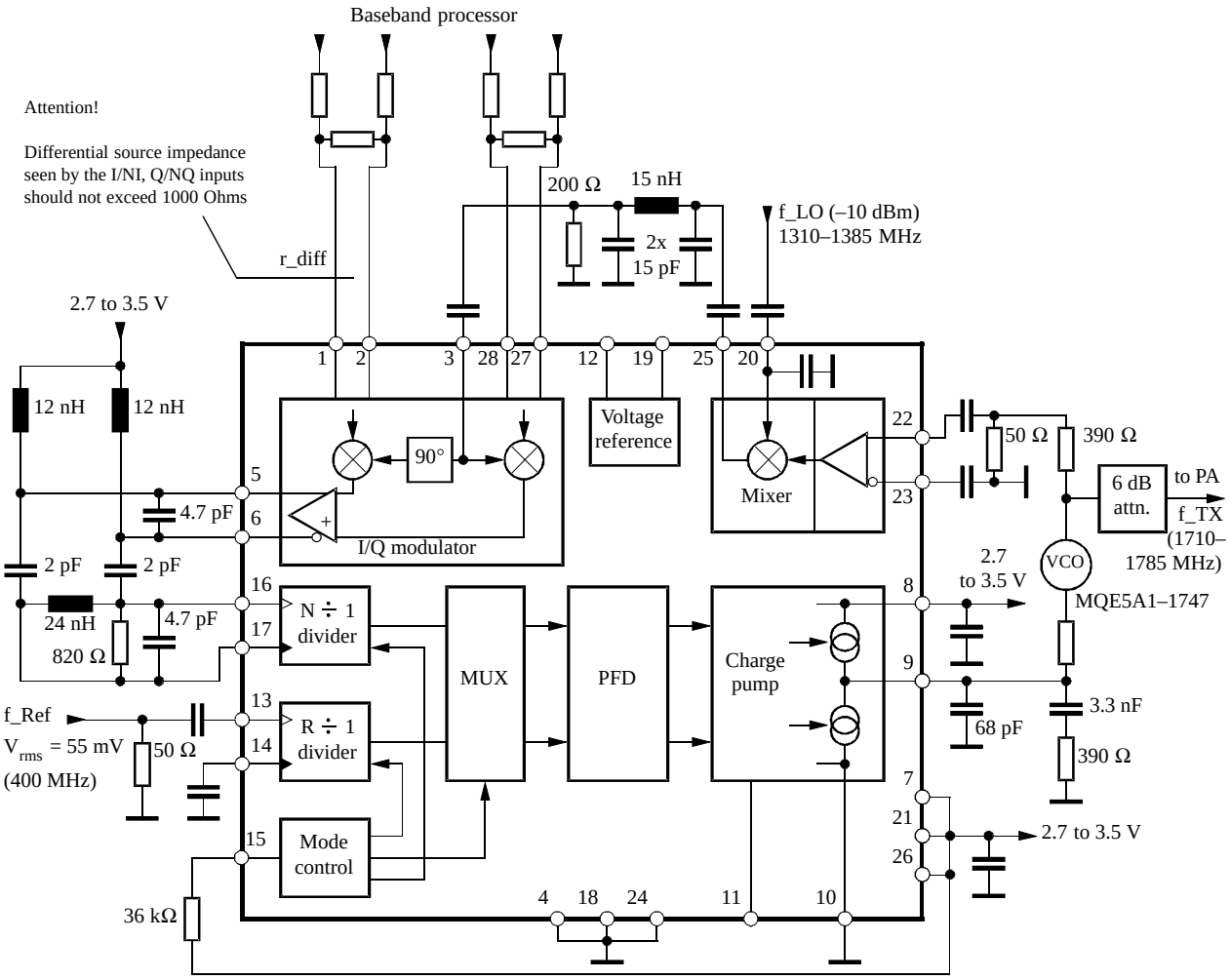
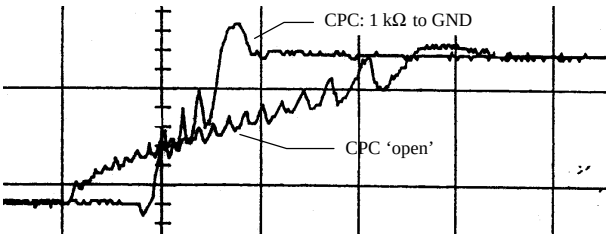


Figure 16. Application circuit (power-up and charge-pump control is not shown)

Measurements

Modulation-Loop Settling Time

As valid for all PLL loops, the settling time depends on several factors. Figure 17 is an extraction from measurements performed in an arrangement like the application circuit. It shows that a loop settling time of a few µs can be achieved.



Vertical: VCO tuning voltage 1 V/Div
Horizontal: Time 1 µs/Div

Figure 17.

Modulation Spectrum & Phase Error

Application for GSM900

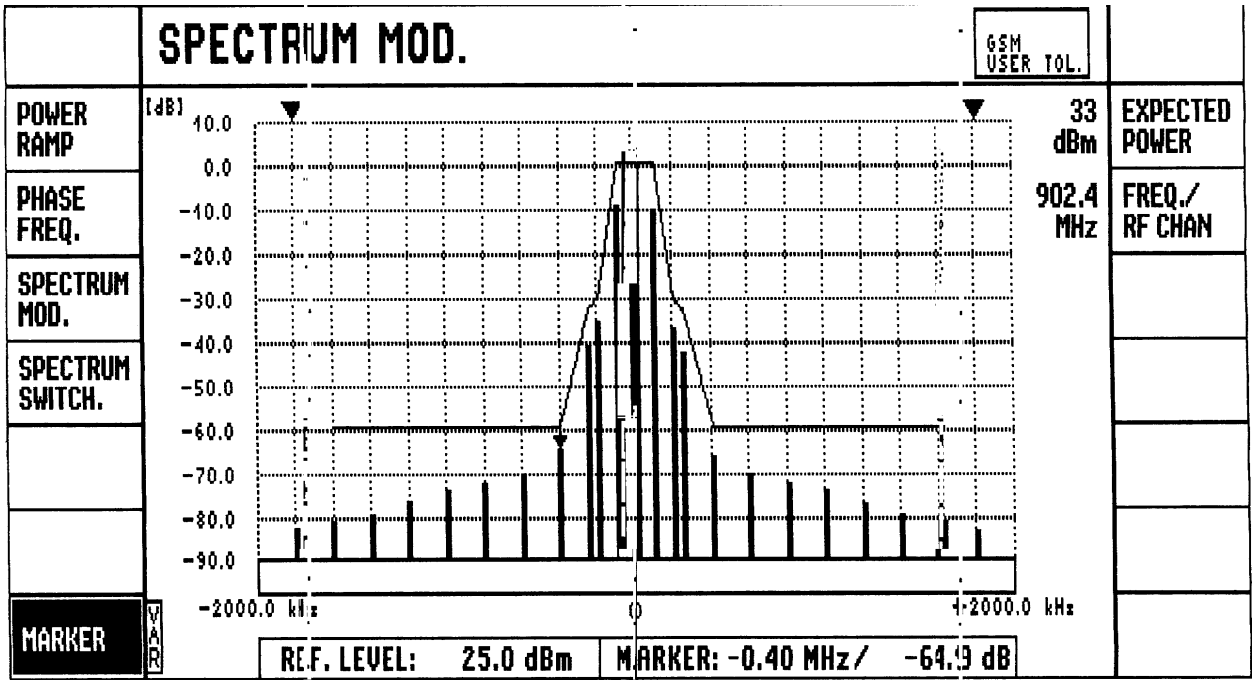


Figure 18. Modulation spectrum

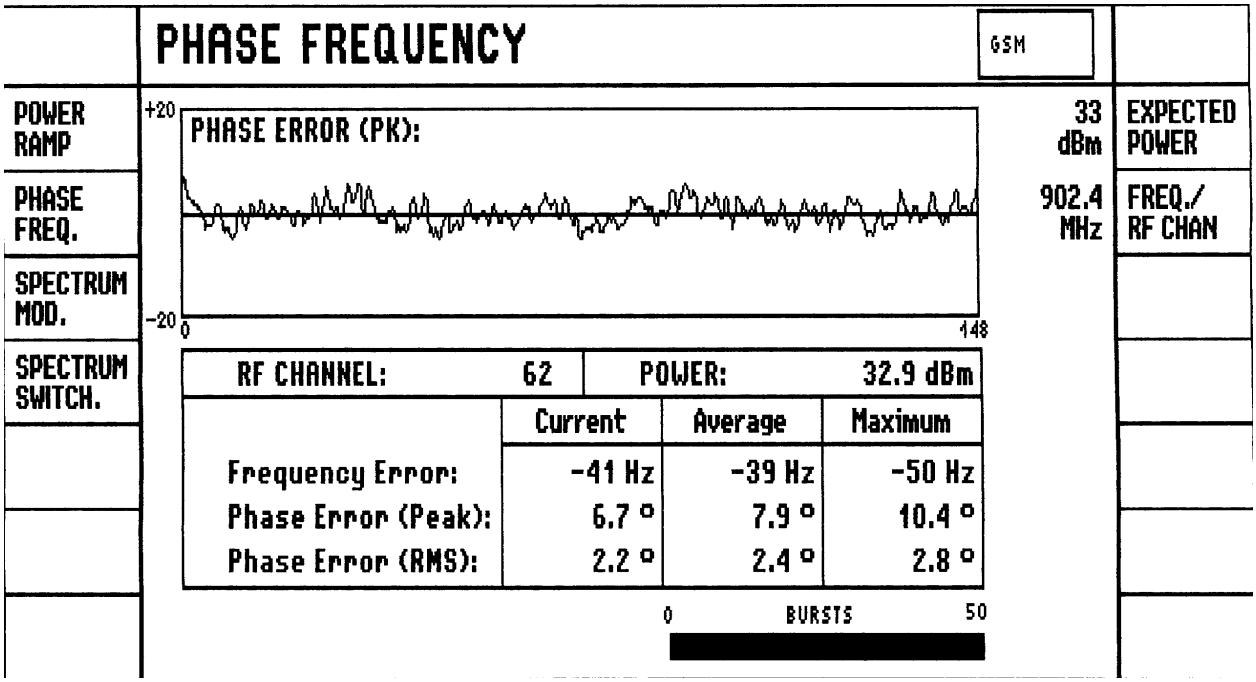


Figure 19. Phase error

Application for DCS1800

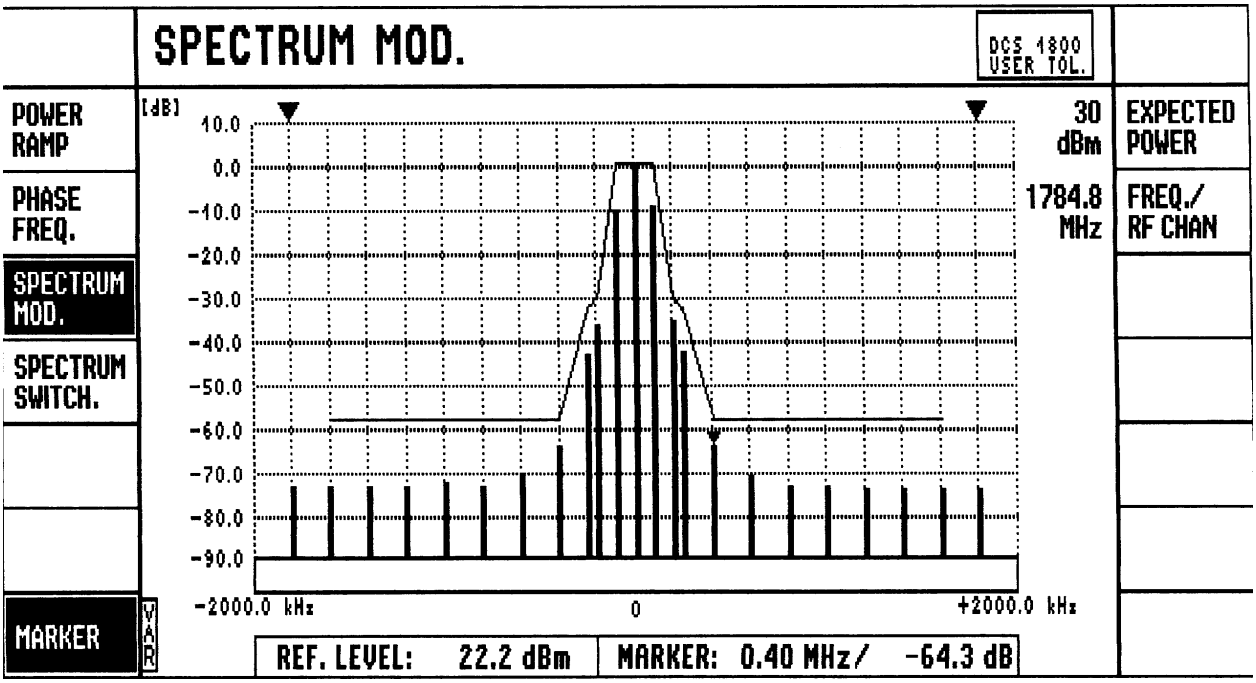


Figure 20. Modulation spectrum

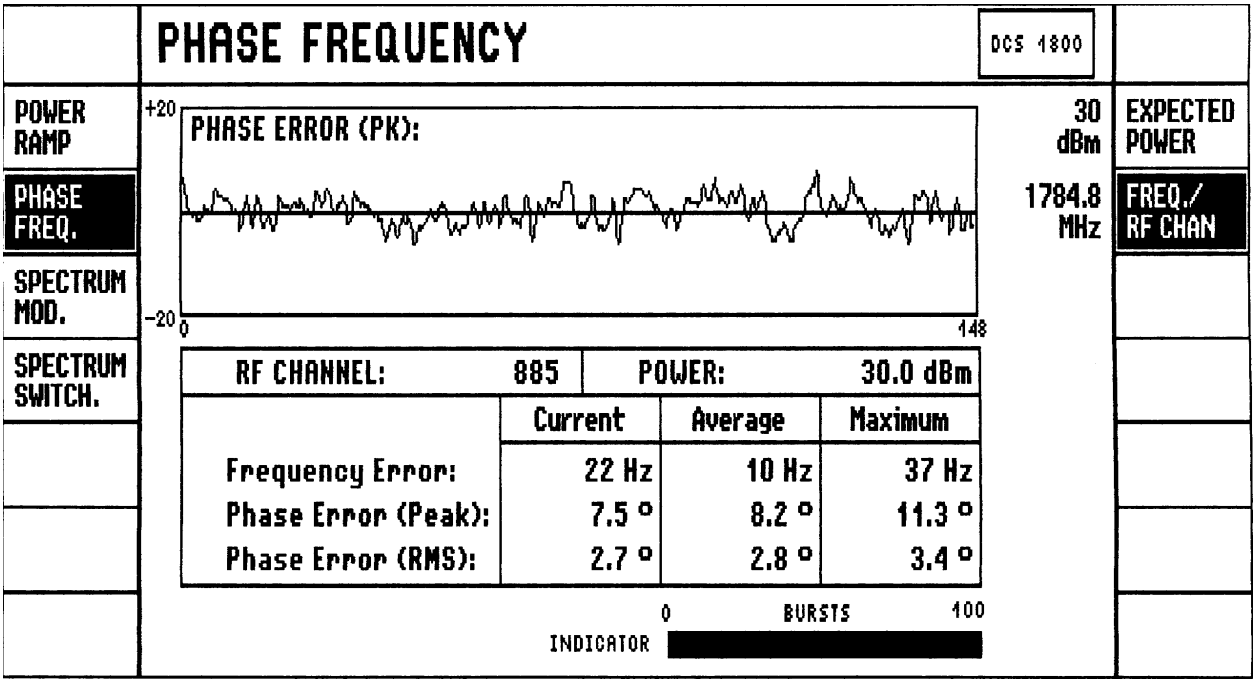


Figure 21. Phase error

Application for PCS1900

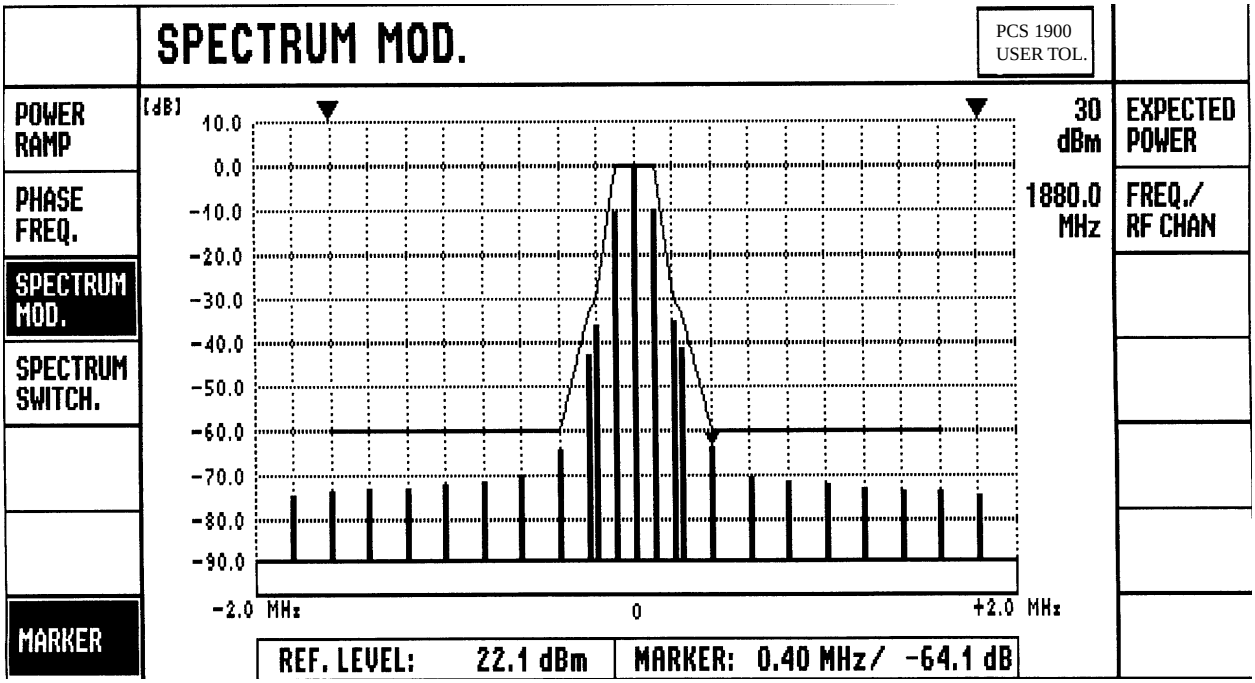


Figure 22. Modulation spectrum

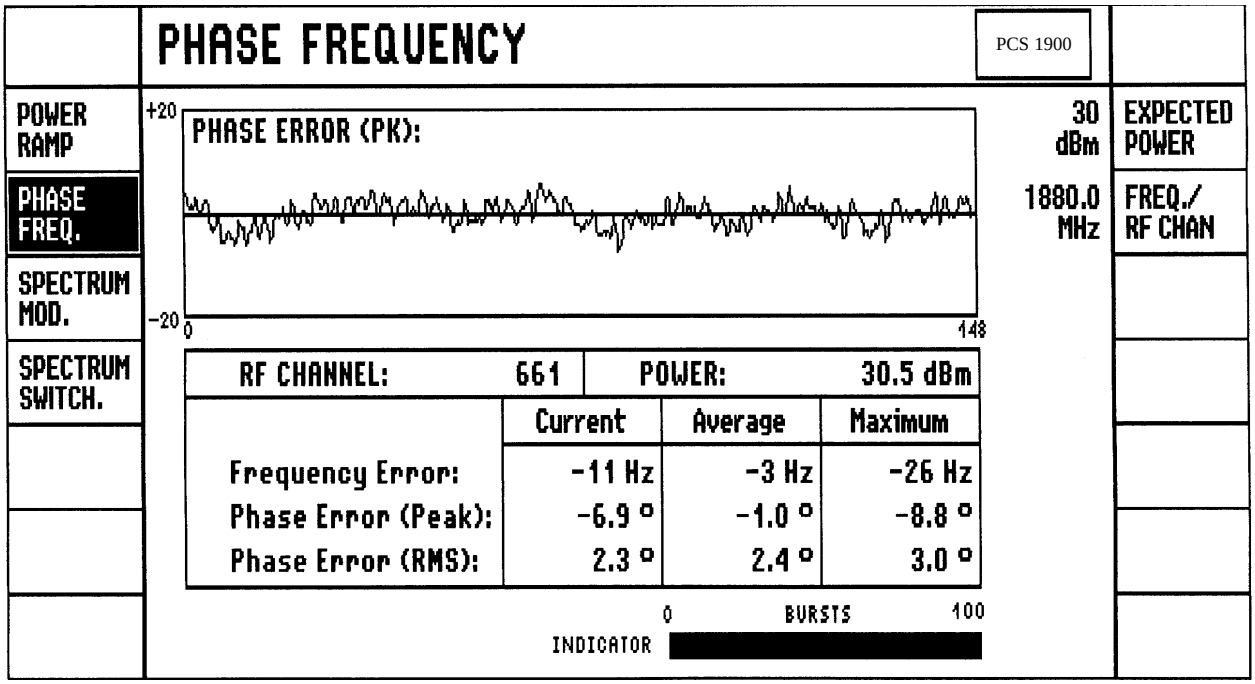
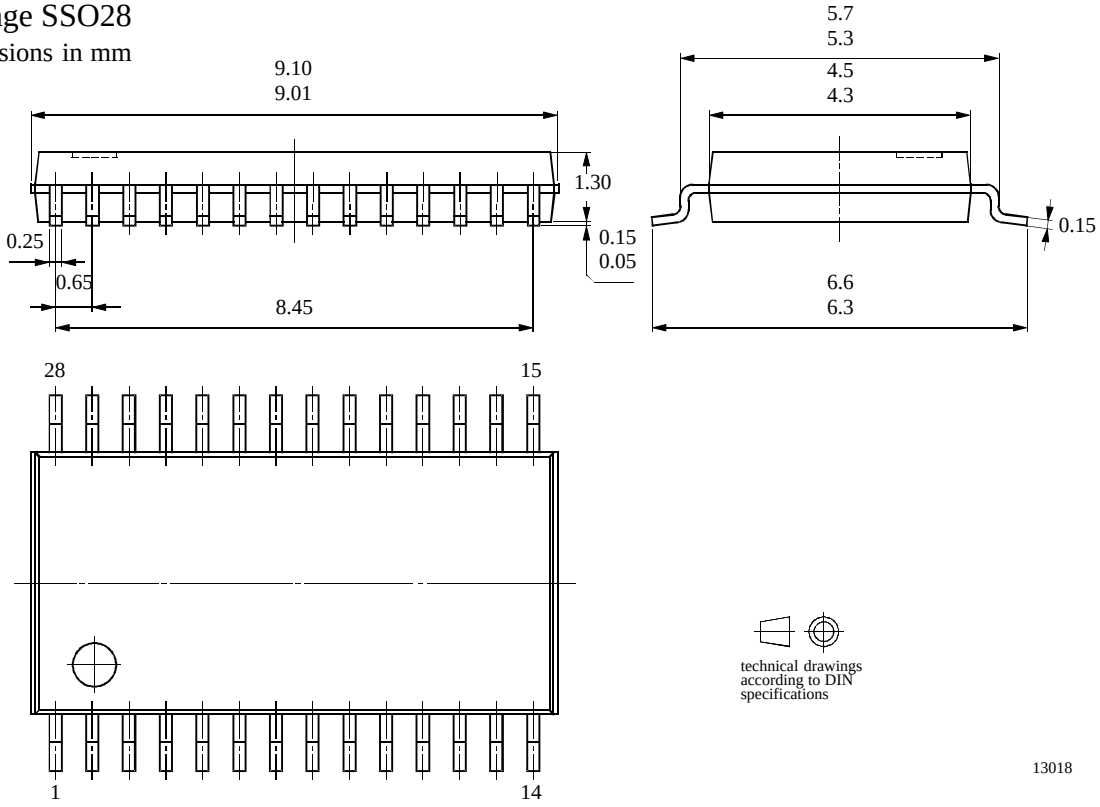


Figure 23. Phase error

Complete transmitters (including PA) were measured. The test equipment was the R & S CMD55 performing standard approval tests. Typically, the spectrum @ 400 kHz off the center carrier frequency is approximately –65 dB attenuated (–60 dB according specificarion). The corresponding rms phase error is about 3°. Dimensioning the loop-filters allows to optimize spectral-and phase error performance.

Package Information

Package SSO28
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.temic–semi.com

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