UJA1023

LIN-I/O slave

Rev. 03 — 9 February 2006 Preliminary data sheet

1. General description

The UJA1023 is a stand-alone Local Interconnect Network (LIN) I/O slave that replaces basic components commonly used in electronic control units for input and output handling. The UJA1023 contains a LIN 2.0 controller, an integrated LIN transceiver which is LIN 2.0 / SAE J2602 compliant and LIN 1.3 compatible, a 30 kΩ termination resistor necessary for LIN-slaves, and eight I/O ports which are configurable via the LIN bus.

An automatic bit rate synchronization circuit adapts to any (master) bit rate between 1 kbit/s and 20 kbit/s. For this, an oscillator is integrated.

The LIN protocol will be handled autonomously and both Node Address (NAD) and LIN frame Identifier (ID) programming will be done by a master request and an optional slave response message in combination with a daisy chain or plug coding function.

The eight bidirectional I/O pins are configurable via LIN bus messages and can have the following functions:

- Input:
  - Standard input pin
  - Local wake-up
  - Edge capturing on falling, rising or both edges
  - Analog input pin
  - Switch matrix (in combination with output pins)
- Output:
  - Standard output pin as high-side driver, low-side driver or push-pull driver
  - Cyclic sense mode for local wake-up
  - PWM mode, for example, for back light illumination
  - Switch matrix (in combination with input pins)

On entering a low-power mode it is possible to hold the last output state or to change over to a user programmable output state. In case of a failure (e.g. LIN bus short to ground) the output changes over to a user programmable limp home output state and the low-power Limp home mode will be entered.

Due to the advanced low-power behavior the power consumption of the UJA1023 in low-power mode is minimal.

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2. Features

- Automatic bit rate synchronization to any (master) bit rate between 1 kbit/s and 20 kbit/s
- Integrated LIN 2.0 / SAE J2602 transceiver (including 30 kΩ termination resistor)
- Eight bidirectional I/O pins
- 4 × 2, 4 × 3, or 4 × 4 switch matrix to support reading and supplying a maximum number of 16 switches
- Outputs configurable as high-side and/or low-side driver and as cyclic or PWM driver
- 8-bit ADC
- Advanced low-power behavior
- On-chip oscillator
- Node Address (NAD) configuration via daisy chain or plug coding
- Inputs supporting local wake-up and edge capturing
- Configurable Sleep mode
- Limp home configuration in case of error conditions
- Extremely low electromagnetic emission
- High immunity against electromagnetic interference
- Bus line protected in accordance with ISO 7637
- Extended ambient temperature range (–40 °C to +125 °C)

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	supply voltage on pin BAT	all operating modes		6.5	-	27	V
I_{BAT}	supply current on pin BAT	LH sleep, Sleep and Limp home mode	[1]	-	45	65	µA
V_{LIN}	voltage on pin LIN	DC value		–27	-	+40	V
T_{vj}	virtual junction temperature		[2]	–40	-	+150	°C
V_{esd}	electrostatic discharge voltage on pins LIN, BAT, C1, C2 and C3	human body model; C = 100 pF; R = 1.5 kΩ		–8	-	+8	kV

[1] All outputs turned off, LIN recessive, V_{th1} selected.

[2] Junction temperature in accordance with IEC60747-1. An alternative definition of $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value to be used for calculating T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
UJA1023T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Block diagram

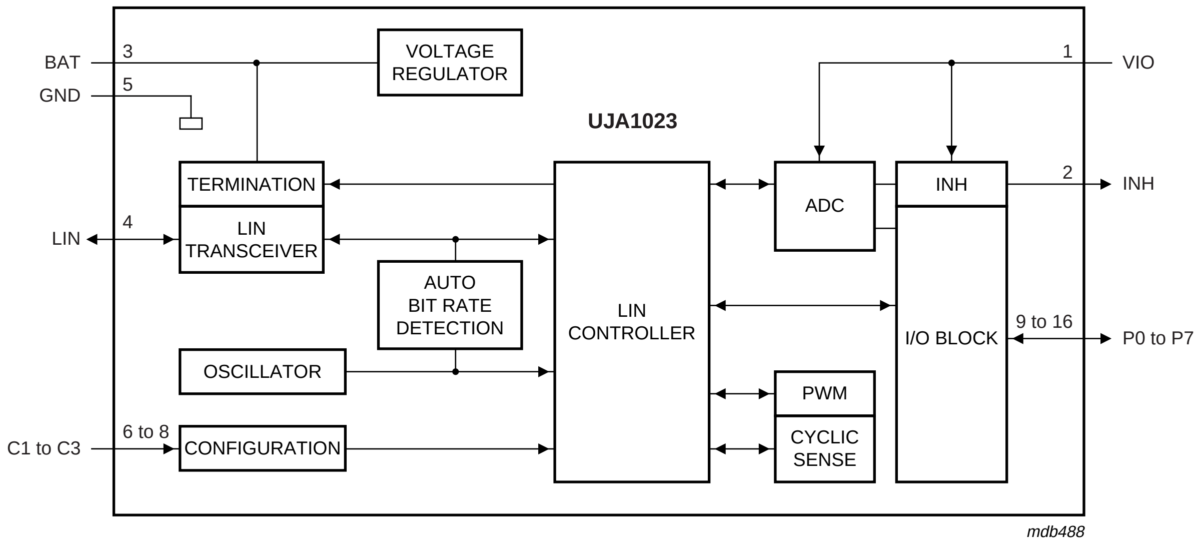


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

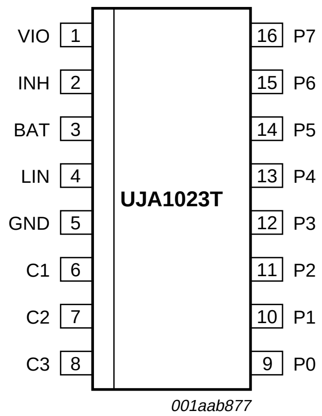


Fig 2. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Type [1]	Description
VIO	1	I	reference input for level adaptation of the I/O pins P0 to P7
INH	2	O	inhibit output for controlling an external voltage regulator or internal ADC
BAT	3	I	battery supply
LIN	4	I/O	LIN bus line
GND	5	I	ground
C1	6	I	configuration input 1 for LIN slave NAD assignment
C2	7	I	configuration input 2 for LIN slave NAD assignment
C3	8	I/O	configuration input / output 3 for LIN slave NAD assignment
P0	9	I/O	bidirectional I/O pin 0
P1	10	I/O	bidirectional I/O pin 1
P2	11	I/O	bidirectional I/O pin 2
P3	12	I/O	bidirectional I/O pin 3
P4	13	I/O	bidirectional I/O pin 4
P5	14	I/O	bidirectional I/O pin 5
P6	15	I/O	bidirectional I/O pin 6
P7	16	I/O	bidirectional I/O pin 7

[1] I = input;
O = output;
I/O = input or output.

7. Functional description

The UJA1023 combines all blocks necessary to work as a stand-alone LIN slave. Various I/O functions typically used in a car are supported. For a more detailed description refer to Section 7.2 to Section 7.6. The block diagram is shown in Figure 1.

7.1 Short description of the UJA1023

7.1.1 LIN controller

The LIN 2.0 controller monitors and evaluates the LIN messages in order to process the LIN commands. It supervises and executes the NAD assignment, ID assignment and I/O-configuration and controls the operating modes of the UJA1023.

The NAD configuration is done by a combination of a LIN master request frame and a setting done by either a daisy chain or plug ID code.

7.1.2 LIN transceiver (including termination)

The LIN transceiver, which is LIN 2.0 / SAE J2602 compliant, is the interface between the internal LIN controller and the physical LIN bus. The transmit data stream of the LIN controller is converted into a bus signal with an optimized wave shape to minimize electromagnetic emission. The required LIN slave termination of 30 kΩ is already integrated. In case of LIN bus faults the UJA1023 switches to the low-power Limp home mode.

7.1.3 Automatic bit rate detection

The automatic bit rate detection adapts to the LIN master's bit rate. Any bit rate between 1 kbit/s and 20 kbit/s can be handled. This block checks whether the synchronization break and synchronization field are valid. If not, the message will be rejected.

7.1.4 Oscillator

The on-chip oscillator provides the internal clock signal for some digital functions and is the time reference for the automatic bit rate detection.

7.1.5 I/O block

The I/O block controls the configuration of the I/O pins. The LIN master configures the I/O pin functionality by means of a master request frame and an optional slave response frame.

Besides the standard level input and output behavior the following functions are also handled by the UJA1023: local wake-up, cyclic input, edge capture, PWM output, switch matrix I/O and AD conversion.

7.1.6 ADC

With three external components an 8-bit ADC function can be implemented. Each of the eight bidirectional I/O pins can be used as input for the ADC, one at a time.

7.1.7 PWM

Each pin can be configured with a Pulse Width Modulation (PWM) function. The resolution is 8-bit and the base frequency is approximately 2.7 kHz.

7.1.8 Cyclic sense

To reduce current consumption, the cyclic sense function can be used to read a switch. The switch will be supplied and read back periodically.

7.2 LIN controller

7.2.1 Configuration

In this data sheet basic knowledge of the *"LIN diagnostic and configuration specification, Rev. 2.0"* is expected.

7.2.1.1 Message sequence

The UJA1023 conforms to the *"LIN diagnostic and configuration specification, Rev. 2.0"* and is compatible with LIN 1.3.

The UJA1023 can be configured via the LIN command frames 'Master Request' (MasterReq) and 'Slave Response' (SlaveResp). Both frames consist of eight data bytes. The MasterReq is used to send configuration data from the master to the slaves, whereas the slave being addressed by the prior MasterReq will answer with the related data on demand.

Depending on the usage of the MasterReq the meaning of the data bytes can be different. Thus each LIN slave evaluates these data bytes.

Using MasterReq and SlaveResp for the UJA1023 configuration flow, as shown in Figure 3, is a so-called ‘handshake’ concept. The slave echoes its received MasterReq data in the SlaveResp, so the master can review slave configuration data. The use of the SlaveResp is optional.

The configuration flow is not disturbed if LIN commands other than shown in Figure 3 are sent to other LIN slave nodes. Thus the LIN master can transmit other LIN messages while it (re)configures the UJA1023.

Remarks:

- The I/O configuration will be enabled during the first usage of the UJA1023 message frames (see Section 7.2.5) of the PxResp or PxReq.
- Notation Px is used in this document when referring to a function or property of any of the I/O pins P0 to P7.
- For correct I/O configuration, the configuration requests must be sent in sequential order of first, second and third configuration data block.

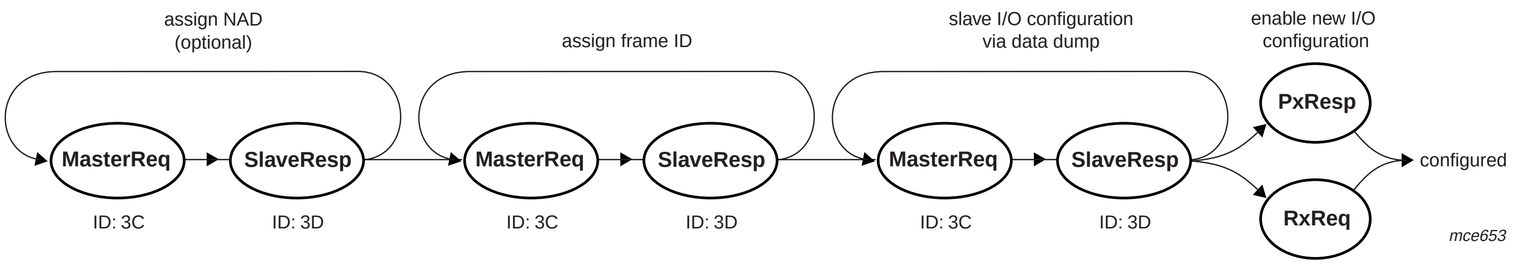


Fig 3. Typical configuration flow

7.2.1.2 LIN slave node address assignment

The default slave Node Address (NAD) after power-on depends on the input levels of the configuration pins C1, C2 and C3. These pins will be sampled directly after the power-on event. The relation between the configuration pins and the NAD is shown in Table 4.

Table 4: Default NAD after power-on

Configuration pins			Default NAD (hex)
C3	C2	C1	
0	0	0	60
0	0	1	61
0	1	0	62
0	1	1	63
1	0	0	64
1	0	1	65
1	1	0	66
1	1	1	67

In case a different NAD is necessary the assign NAD command has to be used. The assign NAD request is carried out if the Service Identifier (SID) in the third data byte of the MasterReq is the assign NAD request and the fourth to seventh data bytes are the LIN supplier codes of Philips (0x0011) and UJA1023 function ID (0x0000).

Table 5: Data bytes of assign NAD request [1]

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	d	d	d	d	d	d	d	d	08
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	0	0	0	B0
D3	0	0	0	1	0	0	0	1	11
D4	0	0	0	0	0	0	0	0	00
D5	0	0	0	0	0	0	0	0	00
D6	0	0	0	0	0	0	0	0	00
D7	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD

[1] d = different values possible; see Table 6.

Table 6: Bit description of assign NAD request

Byte	Bit	Symbol	Description
D0	7 to 0	C[3:1]	Initial NAD. This byte defines the initial NAD, refer to the related items topics
			0x08 to 0x0F (D0[0] = C1, D0[1] = C2 and D0[2] = C3) defines Plug ID; D0[3] = 1 for Plug ID configuration
			0x20 = daisy chain on; enable daisy chain pin drivers and receivers
			0x21 = assign NAD via daisy chain
			0x23 = daisy chain off; disable daisy chain pin drivers and receivers
D1	7 to 0	PCI	Protocol control information.
D2	7 to 0	SID	Service identifier. As SlaveResp the RSID code will be 0xF0.
D3 and D4	7 to 0	-	Supplier ID. Fixed code 0x0011 for Philips.
D5 and D6	7 to 0	-	Function ID. For the UJA1023 this code is fixed as 0x0000.
D7	7 to 0	NAD[7:0]	Slave Node Address (NAD). NAD values are in the range 1 to 127, while 0 and 128 to 255 are reserved for other purposes.

The format of the positive response is shown in Table 7.

Table 7: Positive response assign NAD request [1]

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	d	d	d	d	d	d	d	d	08
D1	0	0	0	0	0	0	0	1	01
D2	1	1	1	1	0	0	0	0	F0
D3	1	1	1	1	1	1	1	1	FF
D4	1	1	1	1	1	1	1	1	FF
D5	1	1	1	1	1	1	1	1	FF
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

[1] d = different values possible; see Table 6.

The NAD assignment can be done via Daisy Chain (DC), (see Section "Daisy chain NAD assignment") as well as via Plug ID (see Section "Plug ID NAD assignment"). The type of NAD assignment can be distinguished on the value of the initial NAD, which is the first data byte D0 of the MasterReq assign NAD request. For reliability reasons the assignment mode decision is valid only if the combination of D0 to D6 (see Table 5) is true. After power-on the UJA1023 message identifiers PxReq and PxResp (see Section 7.2.5) are disabled. This is also true for NAD reassignment. In this case the message identifiers PxReq, PxResp and I/O configuration are disabled.

Daisy chain NAD assignment: Once the UJA1023 receives the assign NAD MasterReq frame and the type of configuration is daisy chain, the following actions can take place, depending on the initial NAD value:

- Initial NAD 0x20: Daisy chain on, the C1 to C3 pin drivers are enabled.
- Initial NAD 0x21: The input level on the configuration pin C1 and the status flag of the internal DC-switch is read. The UJA1023 will be configured if C1 is LOW and the DC-switch is open (see slave 2 in Figure 4). The UJA1023 under daisy chain configuration uses the data byte D7 as new NAD for its further LIN configuration requests (e.g. Assign Frame ID). After the NAD assignment the DC-switch at pin C3 is closed, which puts through the daisy chain signal to the next slave. The switch will be opened again as soon as an Assign NAD request with initial NAD daisy chain off has been received.
- Initial NAD 0x23: Daisy chain off, the C1 to C3 pin drivers are disabled.

After the NAD assignment, for example, the 'assign frame ID' can be used to assign specific ID numbers.

The internal pull-up resistors at pin C1 to C3 are active during the assign NAD process only. Thus it causes no permanent current (see also Section 7.4) and reduces power consumption especially in the low-power modes.

Remark: There is no slave response to assign NAD requests using the initial NAD 0x20 and NAD 0x23.

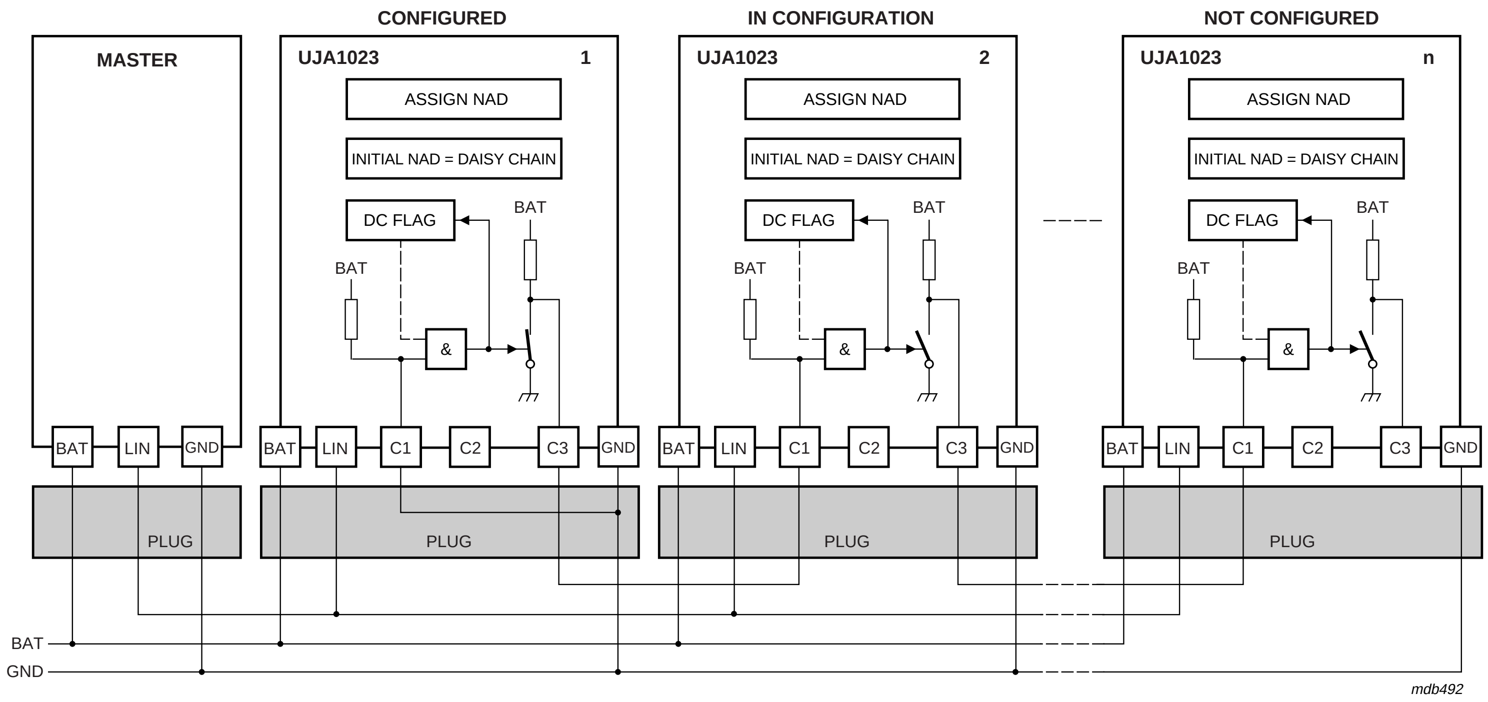


Fig 4. Daisy chain ID

Plug ID NAD assignment: Here the UJA1023 can be addressed via the pins C1, C2, and C3. Once the assign NAD MasterReq with the initial NAD 'Plug ID configuration' is received, the UJA1023 compares the values of the configuration pins C3, C2, and C1 with the values of the data bits D0[2:0]. If the values are equal and bits D0[7:4] are logic 0 and D0[3] is logic 1, the value of D7 is used as new NAD for the UJA1023.

Next, for example, the 'assign frame ID' can be used to assign specific ID numbers.

The internal pull-up resistors at pin C1 to C3 are active during the assign NAD process only. Thus it causes no permanent current (see also Section 7.4) and reduces power consumption especially in the low-power modes.

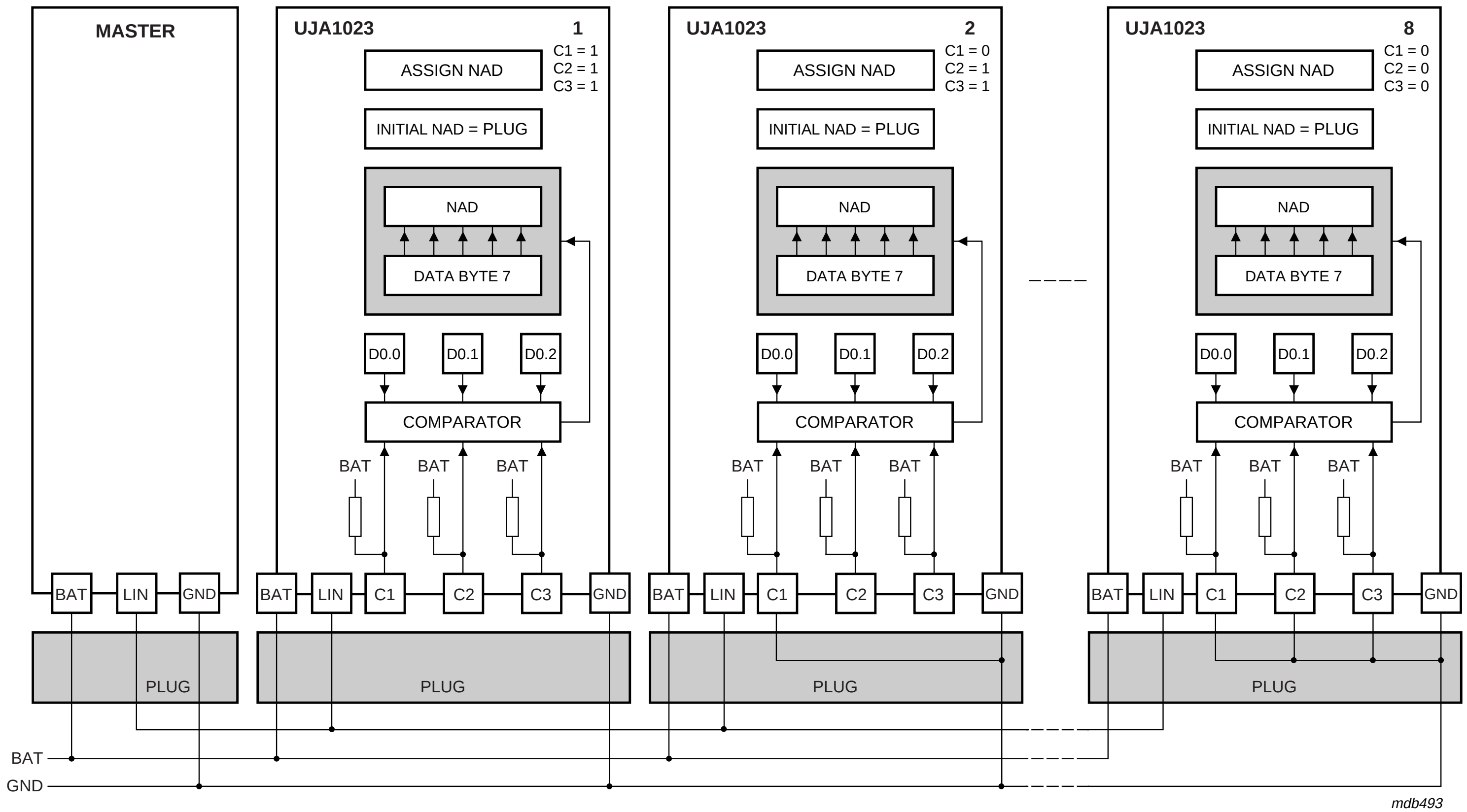

MASTER
BAT
LIN
GND
PLUG
UJA1023
1
C1 = 1
C2 = 1
C3 = 1
ASSIGN NAD
INITIAL NAD = PLUG
NAD
DATA BYTE 7
D0.0
D0.1
D0.2
COMPARATOR
BAT
C1
C2
C3
UJA1023
2
C1 = 0
C2 = 1
C3 = 1
UJA1023
8
C1 = 0
C2 = 0
C3 = 0
BAT
GND
mdb493

Fig 5. Plug ID

7.2.1.3 Assign frame ID

By means of the assign frame ID command the LIN message identifier PxReq and PxResp can be changed to the desired values.

Table 8: Assign frame ID request bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	0	0	1	B1
D3	0	0	0	1	0	0	0	1	11
D4	0	0	0	0	0	0	0	0	00
D5	0	0	0	0	0	0	0	0	00
D6	0	0	0	0	0	0	0	0	00
D7	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	protected ID

Table 9: Assign frame ID request bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave Node Address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID code will be 0xF1.
D3 and D4	7 to 0	-	Supplier ID. Fixed to 0x0011 for Philips.
D5 and D6	7 to 0	-	Message ID. Defines the assignment of the protected ID to PxResp and PxReq
			0x0000: PxReq = protected ID; PxResp = protected ID + 1
			0x0001: PxReq = unchanged; PxResp = protected ID
			0x0002: PxReq = protected ID; PxResp = unchanged
D7	7 to 0	ID[7:0]	Protected ID. Defines the protected ID.

The format of the positive response is shown in Table 10.

Table 10: Positive response assign frame ID

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	0	0	1	01
D2	1	1	1	1	0	0	0	1	F1
D3	1	1	1	1	1	1	1	1	FF
D4	1	1	1	1	1	1	1	1	FF
D5	1	1	1	1	1	1	1	1	FF
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

7.2.1.4 Read by identifier

It is possible to read the supplier identifier, function identifier and the variant of the UJA1023 by means of the read by identifier request. The format for this request is shown in Table 11. The positive response is shown in Table 13, the negative response is shown in Table 14.

Table 11: Read by identifier (LIN product identification)

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	0	1	0	B2
D3	0	0	0	0	0	0	0	0	00
D4	0	0	0	1	0	0	0	1	11
D5	0	0	0	0	0	0	0	0	00
D6	0	0	0	0	0	0	0	0	00
D7	0	0	0	0	0	0	0	0	00

Table 12: Read by identifier bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave Node Address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID code will be 0xF2 for a positive response and 0x7F for a negative response.
D3	7 to 1	-	Identifier. Only the LIN product identifier 0x00 is supported.
D4 and D5	7 to 0	-	Supplier ID. Fixed to 0x0011 for Philips.
D6 and D7	7 to 0	-	Function ID. For the UJA1023 this code is fixed to 0x0000.

Table 13: Read by identifier positive response

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	1	1	1	0	0	1	0	F2
D3	0	0	0	1	0	0	0	1	11
D4	0	0	0	0	0	0	0	0	00
D5	0	0	0	0	0	0	0	0	00
D6	0	0	0	0	0	0	0	0	00
D7	d	d	d	d	d	d	d	d	variant

Table 14: Read by identifier negative response

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	0	1	1	03
D2	0	1	1	1	1	1	1	1	7F
D3	1	0	1	1	0	0	1	0	B2
D4	0	0	0	1	0	0	1	0	12
D5	1	1	1	1	1	1	1	1	FF
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

7.2.1.5 I/O configuration

The I/O configuration is done via the LIN configuration request ‘Data Dump’, where the first data byte of the MasterReq contains the slave node address NAD. The I/O-pin configuration process starts only, if the received slave node address matches the own UJA1023 node address and if data byte D2 (SID) is 0xB4.

As with the other configuration commands, the master transmits the I/O-pin configuration data via the MasterReq message. Due to the limited amount of data bytes within the LIN configuration command ‘Data Dump’, the configuration and diagnosis is split-up into four blocks. The configuration and diagnosis blocks are distinguished on bits 6 and 7 of data byte D3. The master can review the new configuration data via the SlaveResp message. Finally if the master considers the received configuration data of the LIN-I/O to be correct, it can enable the slave I/O-configuration by using the UJA1023 message frames (see Section 7.2.5) PxResp or PxReq.

It should be noted that for correct I/O configuration, the configuration requests must be sent in sequential order of: first, second and third configuration data block.

Table 15: First I/O configuration data block bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	1	0	0	B4
D3	0	0	IM1	IM0	RxDL	ADCIN2	ADCIN1	ADCIN0	00
D4	HSE7	HSE6	HSE5	HSE4	HSE3	HSE2	HSE1	HSE0	00
D5	LSE7	LSE6	LSE5	LSE4	LSE3	LSE2	LSE1	LSE0	00
D6	OM0_7	OM0_6	OM0_5	OM0_4	OM0_3	OM0_2	OM0_1	OM0_0	00
D7	OM1_7	OM1_6	OM1_5	OM1_4	OM1_3	OM1_2	OM1_1	OM1_0	00

Table 16: First I/O configuration data block bit description

Byte	Bit	Symbol	Description		
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).		
D1	7 to 0	PCI[7:0]	Protocol control information.		
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID value will be 0xF4.		
D3	7 and 6	-	00 for first configuration data block.		
	5 and 4	IM[1:0]	Pin INH mode. Mode will be changed after PxReq or PxResp		
			00 = external regulator (control of external voltage regulator)		
			01 = ADC		
			10 = reserved, if selected both bits will be logic 1		
			11 = switch open		
	3	RxDL	Receive data length. Message PxReq contains two data bytes if RxDL = 0 and three data bytes if RxDL = 1.		
	2 to 0	ADCIN[2:0]	Analog source channel selection. The number of ADCIN[2:0] determines which of the P7 to P0 input is used. For example if ADCIN[2:0] = 101 then P5 will be the input. ADCIN[2:0] is used only if ADC mode is selected (IM[1:0] = 01) and RxDL = 0 (No analog input selection at PxReq).		
D4	7 to 0	HSE[7:0]	High-side enable for I/O pin Px.		
D5	7 to 0	LSE[7:0]	Low-side enable for I/O pin Px.		
D6 and D7	7 to 0	OM0_[7:0], OM1_[7:0]	Output mode for I/O pin Px.		
			OM1_x	OM0_x	
			0	0	level
			0	1	reserved
			1	0	cyclic sense
			1	1	PWM

The second configuration data block (shown in Table 17) is selected only if D3.7 = 0 and D3.6 = 1.

Table 17: Second I/O configuration data block bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	1	0	06
D2	1	0	1	1	0	1	0	0	B4
D3	0	1	LSLP	TxDL	SMC	SMW	SM1	SM0	40
D4	CM0_7	CM0_6	CM0_5	CM0_4	CM0_3	CM0_2	CM0_1	CM0_0	00
D5	CM1_7	CM1_6	CM1_5	CM1_4	CM1_3	CM1_2	CM1_1	CM1_0	00
D6	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	TH2/TH1	00
D7	LWM7	LWM6	LWM5	LWM4	LWM3	LWM2	LWM1	LWM0	00

Table 18: Second I/O configuration data block bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID value will be 0xF4.
D3	7 and 6	-	01 for the second configuration data block.
	5	LSLP	Limp home sleep mode. If LSLP = 1, the Limp home sleep mode is enabled. In this case the Limp Home value (LH) is automatically used as output value if the Sleep mode is entered.
	4	TxDL	Transmit data length. Message PxResp contains two data bytes if TxDL = 0 and four data bytes if TxDL = 1.
	3	SMC	Switch matrix capture. If SMC = 1, the Switch matrix capture mode is enabled.
	2	SMW	Switch matrix wake-up. If SMW = 1, the switch matrix wakes up upon changed input level.
	1 and 0	SM[1:0]	Switch matrix enable
			00 = no switch matrix
			01 = 4 × 2: P3 to P0 input and P5 and P4 strong pull down
			10 = 4 × 3: P3 to P0 input and P6 to P4 strong pull down
			11 = 4 × 4: P3 to P0 input and P7 to P4 strong pull down
			Unassigned pins can be used as I/O. It should be noted, however, that for the unassigned pins, which are configured in Capture mode, the captured edge value will not be transferred.

Table 18: Second I/O configuration data block bit description *...continued*

Byte	Bit	Symbol	Description		
D4 and D5	7 to 0	CM0_[7:0], CM1_[7:0]	Capture mode for I/O pin Px.		
			CM1_x	CM0_x	
			0	0	no capture
			0	1	falling edge
			1	0	rising edge
			1	1	both edges
D6	7 to 0	TH2 and TH1	Threshold select. If logic 0 (= TH1), selects V_{th1} as input threshold. If logic 1 (= TH2) selects V_{th2} as input threshold, except in Cyclic sense mode, then V_{th3} is selected.		
D7	7 to 0	LWM_[7:0]	Local wake-up mask. If LWM_x = 1, the corresponding Px pin is configured as local wake-up pin. LWM_x is ignored if Px is configured as switch matrix.		

Table 19 shows the third configuration data block, that is used to define the slope of the transmitter, selection between classic or enhanced checksum model, limp home output value and PWM initial value. It is selected only if D3.7 = 1 and D3.6 = 0.

Table 19: Third I/O configuration data block bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	0	0	04
D2	1	0	1	1	0	1	0	0	B4
D3 [1]	1	0	r	r	r	r	LSC	ECC	80
D4	LH7	LH6	LH5	LH4	LH3	LH2	LH1	LH0	00
D5	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0	00
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

[1] r = reserved, must be ‘0’.

Table 20: Third I/O configuration data block bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier. As SlaveResp the RSID value will be 0xF4.

Table 20: Third I/O configuration data block bit description *...continued*

Byte	Bit	Symbol	Description
D3	7 and 6	-	10 for the third configuration data block.
	5 to 2	-	Reserved. Must be 0.
	1	LSC	LIN slope control
			0 = up to 20 kbit/s (default)
			1 = up to 10.4 kbit/s
	0	ECC	Enhanced checksum control
			0 = classic checksum (default)
			1 = enhanced checksum
D4	7	LH[7:0]	Limp home value. Output value in Limp home and Limp home sleep mode.
D5	7 to 0	PWM[7:0]	PWM initial value.
D6 and D7	7 to 0	-	Not used.

Table 21 shows the fourth data block, that is selected if D3.6 = 1 and D3.7 = 1. It is not used for I/O-pin configuration but to provide the master with diagnosis data of the UJA1023. It is a read-only data block. If the slave node address matches and the fourth data block is selected, the UJA1023 transmits its diagnosis data via the SlaveResp message.

Table 21: Fourth I/O diagnostic data block request frame bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	0	1	0	02
D2	1	0	1	1	0	1	0	0	B4
D3	1	1	0	0	0	0	0	0	C0
D4	1	1	1	1	1	1	1	1	FF
D5	1	1	1	1	1	1	1	1	FF
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

Table 22: Fourth I/O diagnostic data block request frame bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	SID[7:0]	Service identifier.
D3	7 and 6	-	11 for the fourth configuration data block.
	5 to 0	-	Not used.
D4 to D7	7 to 0	-	Not used.

Table 23: Fourth I/O diagnostic data block response frame bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	NAD7	NAD6	NAD5	NAD4	NAD3	NAD2	NAD1	NAD0	NAD
D1	0	0	0	0	0	1	0	0	04
D2	1	1	1	1	0	1	0	0	F4
D3	1	1	0	0	0	0	0	0	C0
D4	P	RxB	CS	TxB	u [1]	NVM	LHE	ERR	00
D5	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00
D6	1	1	1	1	1	1	1	1	FF
D7	1	1	1	1	1	1	1	1	FF

[1] Undefined.

Table 24: Fourth I/O diagnostic data block response frame bit description

Byte	Bit	Symbol	Description
D0	7 to 0	NAD[7:0]	Slave node address (NAD). NAD values are in the range from 1 to 127, while 0 and 128 to 255 are reserved for other purposes. The slave node address is assigned with the assign NAD command (see Table 5).
D1	7 to 0	PCI[7:0]	Protocol control information.
D2	7 to 0	RSID[7:0]	Response service identifier.
D3	7 and 6	-	11 for the fourth configuration data block.
	5 to 0	-	Not used.
D4 [1]	7	P	Parity error. Set if identifier parity bits are erroneous.
	6	RxB	Receive error. Set if start or stop bits are erroneous during reception.
	5	CS	Checksum error. Set if checksum is erroneous.
	4	TxB	Transmit error. Set if start, data or stop bits are erroneous during transmission.
	3	undefined	-
	2	NVM	No valid message. Set if there is bus activity, but no valid message frame for longer than $t_{to(idle)}$.
	1	LHE	Set if Limp home mode is entered.
	0	ERR	Response error. Sets internal signal Response_Error if there is an RxB, CS or TxB during a response frame.
D5	7 to 0	PL[7:0]	PxOut latch value.
D6 and D7	7 to 0	-	Not used.

[1] All diagnosis flags in byte D4 are reset after data access from master.

7.2.1.6 Configuration examples

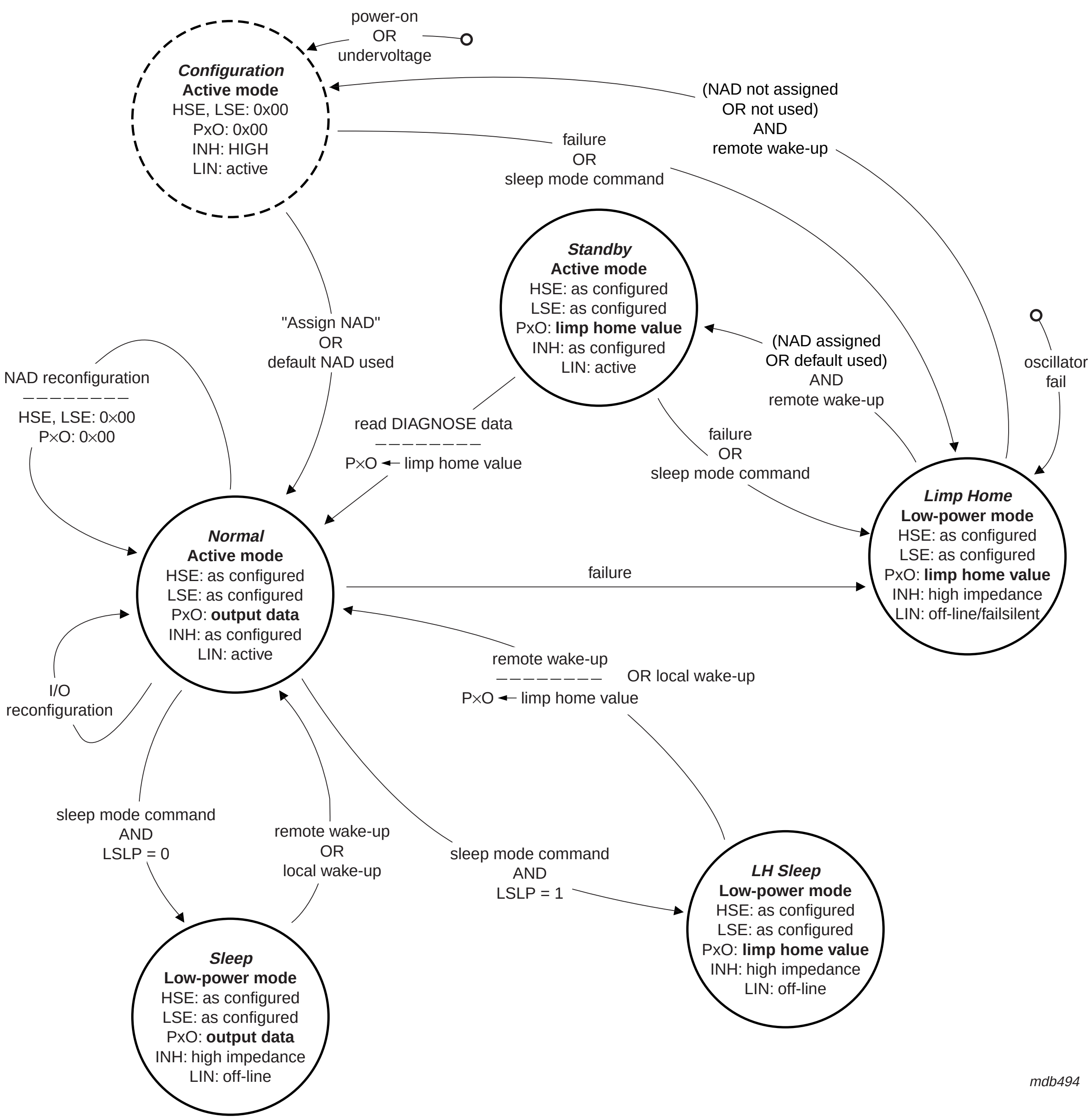
Example 1, UJA1023 configuration with eight low-side outputs.

```
//
//Example 8 LSE and walking ‘1’ pattern
//C1, C2 and C3 are GND
//SB = SyncBreak; SF = SyncField
//
SB SF 3C 60 06 B1 11 00 00 00 04 D2   // Assign frameID, default NAD used and
                                      // ID(PxReq) = 04,ID(PxResp) = 05
SB SF 7D 60 01 F1 FF FF FF FF FF AC   // Positive response
SB SF 3C 60 06 B4 00 00 FF 00 00 E4   // Datadump1, 8 × LSE
SB SF 7D 60 06 F4 00 00 FF 00 00 A4   // Read back configuration sent
SB SF 3C 60 06 B4 40 00 00 00 00 A4   // Datadump2, no capture and
                                      // threshold select (optional)
SB SF 7D 60 06 F4 40 00 00 00 00 64   // Read back configuration sent
SB SF 3C 60 04 B4 80 55 10 FF FF 01   // Data dump3, LH value = 0x55, default
                                                          PWM = 0x10 (optional)
SB SF 7D 60 04 F4 80 55 10 FF FF C0   // Read back configuration sent
SB SF 3C 60 06 B2 00 11 00 00 00 D5   // Read by identifier request (optional)
SB SF 7D 60 06 F2 11 00 00 00 02 93   // Positive response
SB SF C4 01 80 7E                     // IO configuration enabled and low-side
                                      // switch P0 on
SB SF C4 02 80 7D                     // Low-sideswitch P1 on
SB SF C4 04 80 7B                     // Low-sideswitch P2 on
SB SF C4 08 80 77                     // Low-sideswitch P3 on
SB SF C4 10 80 6F                     // Low-sideswitch P4 on
SB SF C4 20 80 5F                     // Low-sideswitch P5 on
SB SF C4 40 80 3F                     // Low-sideswitch P6 on
SB SF C4 80 80 FE                     // Low-sideswitch P7 on
```

Example 2, UJA1023 configuration with eight inputs and edge capture.

```
//
//Example 8 inputs with capture
//C1, C2 and C3 are GND
//SB = SyncBreak; SF = SyncField
//
SB SF 3C 60 06 B1 11 00 00 00 04 D2   // Assign frameID, default NAD used and
                                      // ID(PxReq) = 04,ID(PxResp) = 05
SB SF 7D 60 01 F1 FF FF FF FF FF AC   // Positive response
SB SF 3C 60 06 B4 00 00 00 00 00 E4   // Datadump1, all outputs disabled (optional)
SB SF 7D 60 06 F4 00 00 00 00 00 A4   // Read back configuration sent
SB SF 3C 60 06 B4 40 FF FF 00 FF A4   // Datadump2, all both edge capture and
                                      // inputs as wake-up
SB SF 7D 60 06 F4 40 FF FF 00 FF 64   // Read back configuration sent
SB SF 3C 60 04 B4 80 55 10 FF FF 01   // Data dump3, LH value = 0x55, default
                                                          PWM = 0x10 (optional)
SB SF 7D 60 04 F4 80 55 10 FF FF C0   // Read back configuration sent
SB SF 3C 60 06 B2 00 11 00 00 00 D5   // Read by identifier request (optional)
SB SF 7D 60 06 F2 11 00 00 00 02 93   // Positive response
SB SF 85 00 00 FF                     // IO configuration enabled and read inputs
SB SF 80                              // Dummy message
SB SF 80                              // Dummy message and input 0 changes
SB SF 85 01 01 FD                     // Input 0 set and edge detected
SB SF 80                              //
SB SF 85 01 00 FE                     // Input 0 still set
```

7.2.2 Operating modes



HSE = High-Side Enable

LSE = Low-Side Enable

PxO = PxOut

LSLP = Limp-home sleep

LWM = Local Wake-up Mask

Failure: bus idle time-out or bus dominant time-out

Local: [(LWM = 1) AND (t > $t_{wake(local)}$; after edge capture) causes transmission of LIN wake-up request] AND [reception of LIN header]

Remote: [(t > $t_{wake(bus)}$; after falling edge) AND recessive again] AND [reception of LIN header].

Fig 6. Overview of operating modes

7.2.2.1 Configuration mode

The Configuration mode can be seen as initial state after power-on or undervoltage detection. The UJA1023 configuration values are in the default settings. The I/O pins P0 to P7 (Px) are set to high-impedance behavior and the INH is in its External regulator mode, which outputs a HIGH-level in order to switch on an external voltage regulator.

In Configuration mode the UJA1023 is not configured and it has no valid identifier and, depending on the configuration pins, a default NAD. Thus, with the exception of the MasterReq command, all LIN slave commands are disabled. Once the UJA1023 NAD is assigned, via the assign NAD request, or the default NAD is used for the first time, the Normal mode is entered. If a LIN bus failure is present (bus idle time-out or bus dominant time-out) or the sleep command has been received, the UJA1023 enters its low-power (Limp home) mode.

7.2.2.2 Normal mode

In Normal mode the UJA1023 receives and/or transmits input/output data as well as configuration data.

A UJA1023 in Configuration mode enters the Normal mode only after its NAD assignment or the first usage of the default NAD. After a NAD reconfiguration, all ports that are configured in Output mode will be set to high-impedance.

Coming from Sleep mode or Limp home sleep mode the Normal mode can be entered via local or remote wake-up. The output register of each I/O pin P0 to P7 (PxOut) keeps its values of the Sleep mode or Limp home sleep mode. If the INH is in External regulator mode, it outputs a HIGH-level to switch on an external voltage regulator.

For a mode transition from Standby mode to Normal mode the diagnostic data must be read via a SlaveResp. With this request the master acknowledges the previous failure. The PxOut registers keep their limp home values.

7.2.2.3 Sleep mode

The UJA1023 enters its Sleep mode when the ‘Sleep mode command’ has been received and the limp home sleep bit LSLP is reset (LSLP = 0). In Sleep mode the UJA1023 keeps the current status on its Px. The INH will switch to high-impedance state.

After a local wake-up event the UJA1023 sends a ‘wake-up signal’ to wake up the master. In Sleep mode the PWM and ADC are reset. The first LIN message will be lost due to waking up the UJA1023.

7.2.2.4 Limp home sleep mode

Some applications may need dedicated HIGH and/or LOW output levels during Sleep mode in order to achieve the lowest power dissipation of the application. Therefore the UJA1023 provides the Limp home sleep mode (LH sleep mode). By enabling the LSLP bit, the LH sleep mode output behavior can be configured. The LH sleep mode is enabled if the configuration bit LSLP (D3.5) is set (LSLP = 1, see Table 18).

After a local wake-up event the UJA1023 sends a ‘wake-up signal’ to wake up the master. In the LH sleep mode the output registers (PxOut) of the UJA1023 are loaded with the limp home value. After a wake-up event (local or remote wake-up) the PxOut keep their limp home value.

In LH sleep mode the PWM and ADC are reset. The first LIN message will be lost due to waking up the UJA1023.

7.2.2.5 Limp home mode and Standby mode

Limp home mode and Standby mode differ in the output of pin INH if the INH is configured in External regulator mode. Where in Limp home mode pin INH is high-impedance and in Standby mode pin INH is HIGH. In contrast to the Standby mode the Limp home mode is a low-power mode.

The limp home value specifies the PxOut values in case LIN bus communication fails. The Px configuration push-pull, open-drain or high-impedance keeps unchanged in Limp home mode.

The Limp home mode will be entered from Normal mode if the LIN bus is short-circuited to ground for a time exceeding the bus dominant time-out ($t_{to(dom)}$) or if the bus idle time-out ($t_{to(idle)}$) expires.

Coming from Limp home mode the Standby mode is entered after remote wake-up if the UJA1023 is configured. In case the UJA1023 is not configured, it enters the Configuration mode after remote wake-up.

In Standby and Configuration mode the UJA1023 enters the Limp home mode again if the configuration fails or if the ‘Sleep mode command’ has been received.

7.2.3 I/O pin modes

7.2.3.1 Input

Inputs can always be read via a PxResp frame (see Section 7.2.5). The input threshold is determined by the TH bits in the second I/O configuration block (see Table 17).

7.2.3.2 Level mode

In Level mode the PxOut register of the UJA1023 can be set or reset. Depending on the Px configuration the PxOut value is output.

7.2.3.3 PWM mode

The PWM mode provides a PWM signal with 8-bit resolution to the I/O-stage. The base frequency is typically 700 kHz divided by 256 (8-bit) and becomes approximately 2.7 kHz. The mode is entered via both mode configuration bits OM0 and OM1. The PWM signal is common for all assigned outputs.

In the low-power modes (Sleep mode, LH sleep mode and Limp home mode) the PWM value is reset (PWM = 0x00) and the previous PWM value is lost.

7.2.3.4 Cyclic sense mode

The Cyclic sense mode is used to supply and read back external switches. In this mode the Px pin is configured as a switched supply to reduce the power consumption. It is primarily intended to supply wake-up switches.

A Px pin in Cyclic sense mode has to be configured with the High-Side Enable register (HSE) in HIGH-state and the Low-Side Enable register (LSE) in LOW-state. The PxOut flip-flop is being cyclically switched (see Figure 7).

The Cyclic sense mode can be configured via the Output mode bits OM0 and OM1 in the configuration data bytes (see Table 16). In case threshold TH2 is selected then threshold TH3 will be used instead. This feature is used for diagnosis purposes to check the presence of a switch with an integrated parallel resistor (typical value is 4300 Ω). The switch can be detected by selecting first TH1 and then TH2.

All Px pins in Cyclic sense mode are sampled simultaneously. The Cyclic sense mode timing is specified in Section 11. No wake-up will occur when the local wake-up mask is set and Sleep mode is entered when the Px pin is LOW. A wake-up will be issued when in Sleep mode and the Px input level changes.

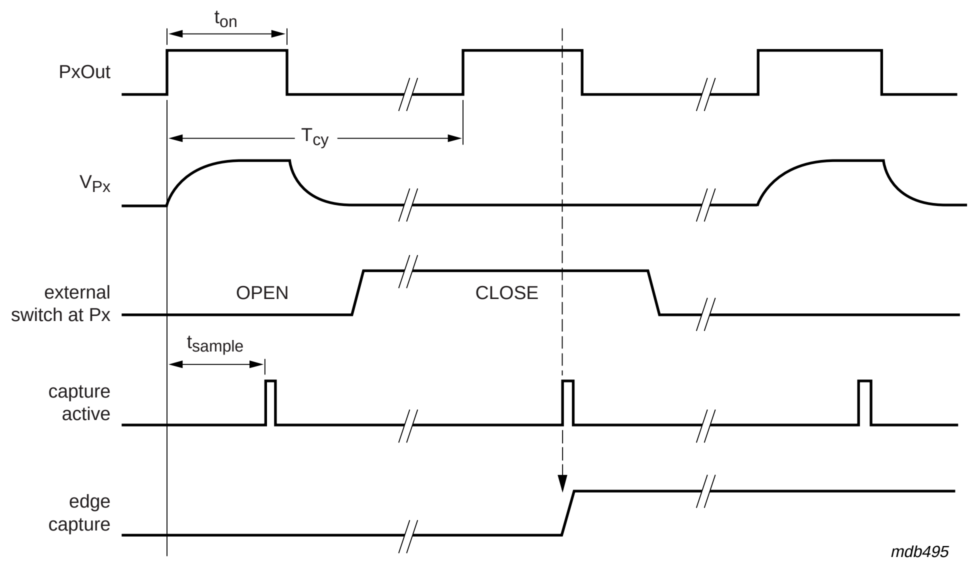


Fig 7. Cyclic sense mode

7.2.3.5 Switch matrix mode

Figure 8 shows an application example of a 4 × 4 switch matrix with the UJA1023. The drive capability of the I/O-pins Px supports the use of a 4 × 4 switch matrix without extra components. The I/O pins from P0 to P3 provide a weak but sufficient pull-up for switch applications and the pins from P4 to P7 are used as strong pull-down in case a switch is pushed.

The Switch matrix mode can be enabled for the I/O-pins Px via data byte D3 of the second configuration data block (see Table 18).

The data bits SM0 and SM1 configure P0 to P3 as an input with a weak but sufficient pull-up for switch applications and P4 to P7 as strong pull-down in order to detect an activated switch (see Table 18).

In Normal mode when a valid sync break and sync field is received, automatically a matrix scan starts:

- Immediately if the slave is not addressed
- When addressed, after the LIN message is handled

This means that the scan matrix value is determined directly after the previous LIN message.

In case two or more switches are closed simultaneously, extra diodes have to be added to prevent the ‘short-circuit’ of neighbor switches.

For the switch matrix inputs a ‘quasi’ capture mode can be configured via the data bit SMC (D3.3) of the second configuration block. If a matrix switch input value has been changed the changed value is captured until the master reads the switch matrix value via the UJA1023 command PxResp. Note that two readings are necessary for proper initialization.

A switch matrix can be configured as local wake-up. If the data bit SMW (D3.2) of the second configuration block is set to logic 1, a change of a matrix switch input value causes a wake-up of the UJA1023. If in addition the Switch matrix capture mode is enabled via SMC the switch matrix value of PxResp represents the local wake-up source switch of the switch matrix.

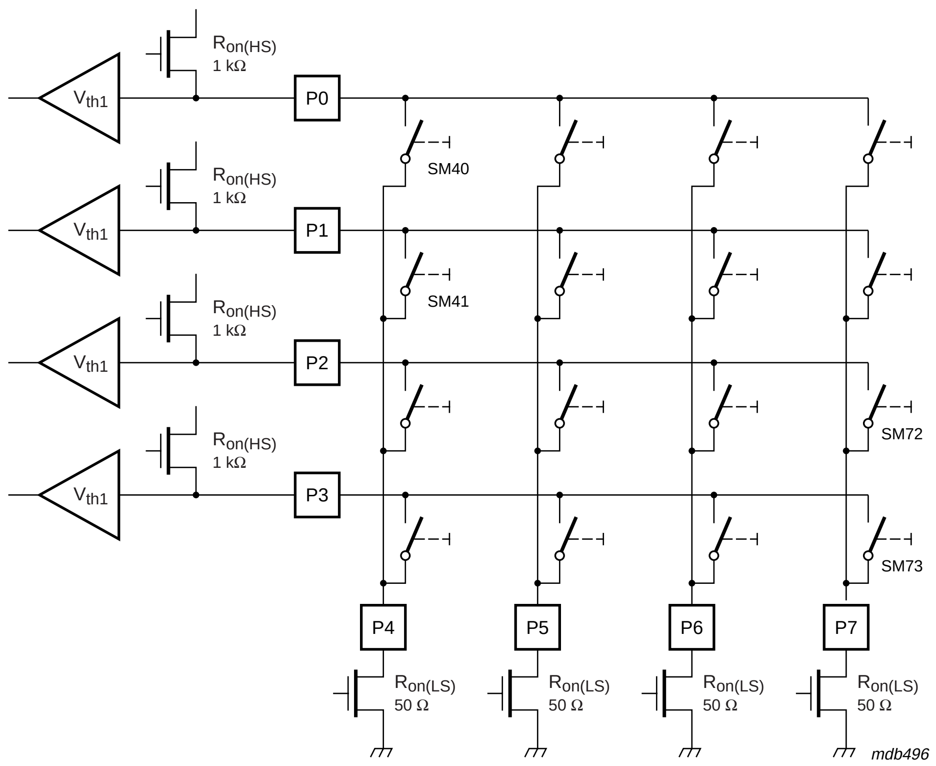


Fig 8. Switch matrix principle

7.2.3.6 ADC mode

The principle of the bit stream ADC is shown in Figure 9. Only three external components are needed per analog input, which should be dimensioned as: R_i = R1 = 100 kΩ; C1 = 10 nF. All eight inputs can be used as analog input, one at a time. ADC values are referenced to V_{VIO}. A register/counter is used to count the ratio of HIGH and LOW phases of the bit stream. This ratio represents the analog voltage V_A. The upper counter is used to define the measurement period, typically 1.5 ms.

The inverted bit stream of the ADC comparator generates the quasi-analog output voltage on pin INH, which can be used to control the analog voltage V_A via a low-pass filter.

An analog-to-digital conversion will have following steps:

1. Select an input channel via PxReq, see Section 7.2.5. Not needed in case a fixed ADC-input is selected (see Table 16 for RxDL = 0 and ADCIN[2:0]).
2. The internal multiplexer switches over to the selected input; note that some time is needed to stabilize the loop, due to the RC network time constant.
3. In case a valid sync break and sync field is received, an analog-to-digital conversion starts. The data is available in the next LIN message, implying the ADC value is sampled during the **previous** LIN message.

To reduce current consumption, the $0.5V_{VIO}$ reference voltage is turned off in the low-power modes.

7.2.4 INH pin mode

The External regulator mode, IM0 = IM1 = 0 (see Table 16), can be used to control an external voltage regulator. In Configuration mode, Normal mode and Standby mode the INH outputs a HIGH level, and in the low-power modes (Sleep, LH sleep and Limp home) the INH pin becomes high-impedance.

Switching between the INH modes ‘external regulator’ and ‘switch open’ the INH pin can be used as high-side switch.

In ADC mode the INH pin is configured internally as follows: the high-side switch is put in high-impedance state and a special symmetrical push-pull output is activated. Next, the ADC mode enables an ADC control loop. The output level of the push-pull stage is defined via the V_{VIO} voltage.

7.2.5 LIN-I/O message frames

The UJA1023 uses one LIN command to receive data PxReq and one to transmit data PxResp respectively. The IDs for PxReq and PxResp are configured by means of the ‘assign frame ID’ command as described in Section 7.2.1.3.

Please note that the I/O configuration will be enabled during the first usage of the PxResp or PxReq.

The PxReq and PxResp data bytes are described in Table 25 to Table 28.

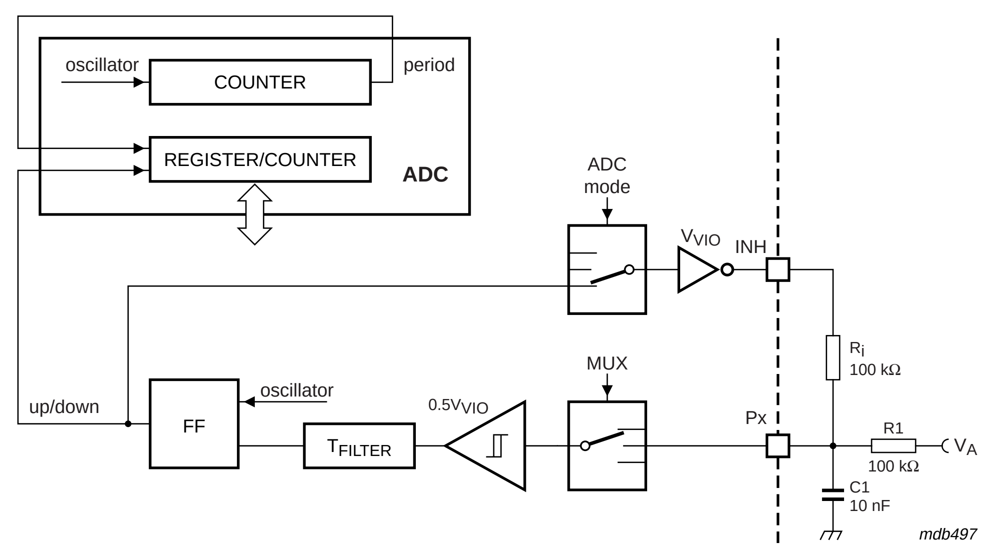


Fig 9. Analog-to-digital converter

Table 25: PxReq frame bit allocation

Data byte	7	6	5	4	3	2	1	0	Default value (hex)
D0	P7	P6	P5	P4	P3	P2	P1	P0	00
D1	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0	00
D2	-	-	-	-	-	ADCIN2	ADCIN1	ADCIN0	00

Table 26: PxReq frame bit description

Byte	Bit	Symbol	Description
D0	7 to 0	P[7:0]	Px output value. The Px output value is ignored if Px is configured in cyclic sense or PWM mode.
D1	7 to 0	PWM[7:0]	PWM value.
D2	7 to 3	-	Not used.
	2 to 0	ADCIN[2:0]	ADC analog source channel selection. For example, 000 selects input 0, 001 selects input 1 and 111 selects input 7. The ADC input source is observed only if the INH output is in ADC mode. The UJA1023 expects to receive data byte D2 only if bit RxDL = 1 (bit 3 of byte D3 in the first I/O configuration data block, see Table 15 and Table 16).

Table 27: PxResp frame bit allocation

Data byte	7	6	5	4	3	2	1	0
D0	P7	P6	P5	P4	P3	P2	P1	P0
D1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
	SM53	SM52	SM51	SM50	SM43	SM42	SM41	SM40
D2	PxL7	PxL6	PxL5	PxL4	PxL3	PxL2	PxL1	PxL0
	SM73	SM72	SM71	SM70	SM63	SM62	SM61	SM60
D3	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

Table 28: PxResp frame bit allocation

Byte	Bit	Symbol	Description
D0	7 to 0	P[7:0]	Px input value.
Bytes D1 and D2 if switch matrix is not configured (default) [1]			
D1	7 to 0	EC[7:0]	Edge capture value.
D2	7 to 0	PxL[7:0]	PxOut latch value.
Bytes D1 and D2 if switch matrix is configured [1]			
D1	7 to 0	SMxx	Switch matrix value 0. Refer to Figure 8.
D2	7 to 0	SMxx	Switch matrix value 1.
Byte D3 [1]			
D3	7 to 0	PWM[7:0]	PWM value.
	7 to 0	ADC[7:0]	ADC value. The ADC value is transmitted only if the INH output is in ADC mode (IM0 = 1, IM1 = 0).

[1] Data bytes D2 and D3 are transmitted only if bit TxDL = 1 (bit 4 of byte D3 in the second I/O configuration data block, see Table 17 and Table 18).

7.3 I/O block

7.3.1 I/O pins P0 to P7

The I/O-pin structure of the UJA1023 is shown in Figure 10.

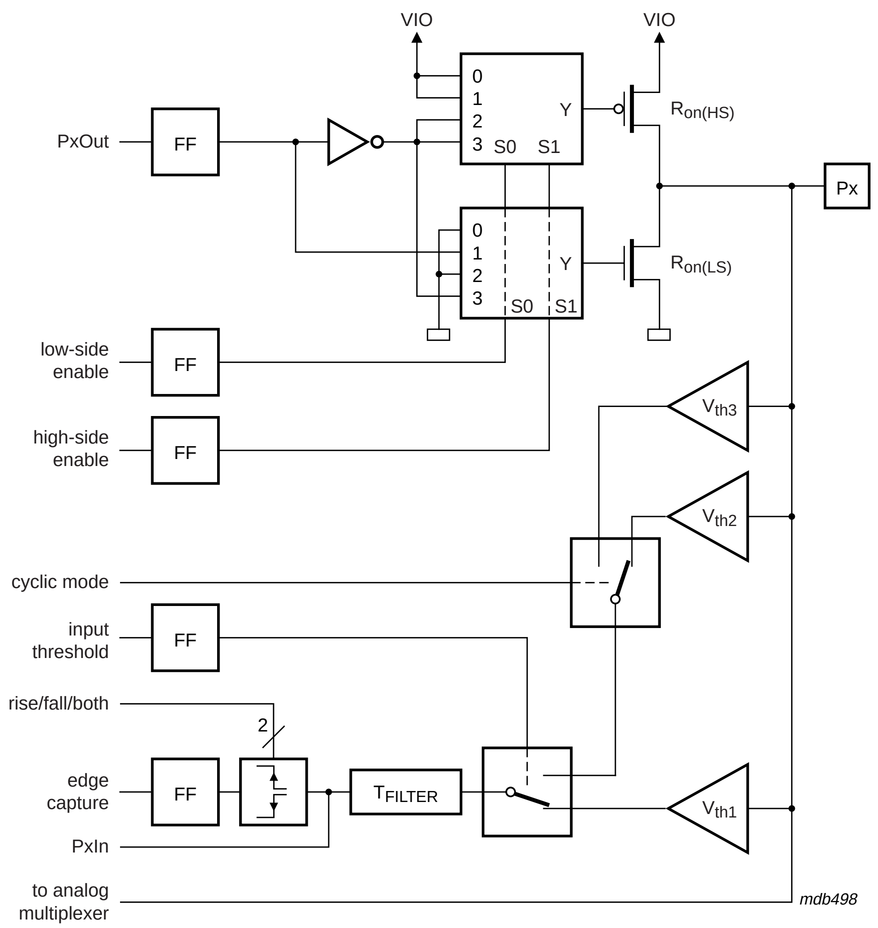


Fig 10. I/O-pin structure

The output is configurable as:

- Push-pull
- High-side switch
- Low-side switch
- High-impedance

The input can be configured:

- To capture on falling, rising or both edges
- To provide an internal pull-up
- With respect to the required threshold V_{th1}, V_{th2} or V_{th3}
- As analog multiplexer for the ADC

Table 29: I/O pin operation [1] [2]

Operation	High-side enable	Low-side enable	PxOut	Input threshold	Edge capture
Power-on condition (high-impedance)	0	0	0	0	none
High-impedance	0	0	X	X	X
Low-side open-state	0	1	0	X	X
Low-side close-state	0	1	1	X	X
High-side open-state (Cyclic sense mode: off-state)	1	0	0	X	X
High-side close-state (Cyclic sense mode: on-state)	1	0	1	X [3]	X
Push-pull HIGH-state	1	1	1	X	X
Push-pull LOW-state	1	1	0	X	X
Input with pull-up	1	0	1	X	X
Input at threshold V_{th1} (typically 3 V)	X	X	X	0	X
Input at threshold V_{th2} (typically 1.5 V)	X	X	X	1	X
Capture edge at falling and rising edge	X	X	X	X	both
Capture edge at falling edge	X	X	X	X	fall
Capture edge at rising edge	X	X	X	X	rise

[1] X = don't care.

[2] The R_{on} values of the high-side and the low-side switches can be found in Section 10. The $R_{on(HS)}$ value is chosen to provide enough pull-up current for switches; thus no external pull-up resistor is needed. The $R_{on(LS)}$ of the low-side driver is much smaller than the $R_{on(HS)}$ of the high-side driver, which enables the low side driver to drive LEDs.

[3] Refer to Table 17 where threshold TH3 is defined in Cyclic sense mode in case threshold TH2 is selected. This feature is used for diagnosis purposes to check the presence of a switch with integrated parallel resistor (a useful resistor value is 3000 Ω ± 1 %).

7.3.2 INH pin

The inhibit pin INH can be configured in three operation modes: ADC mode, Switch open mode and External regulator mode (see Section 7.2.4 and Figure 11). After power-on the INH is in External regulator mode (high-side switch is on).

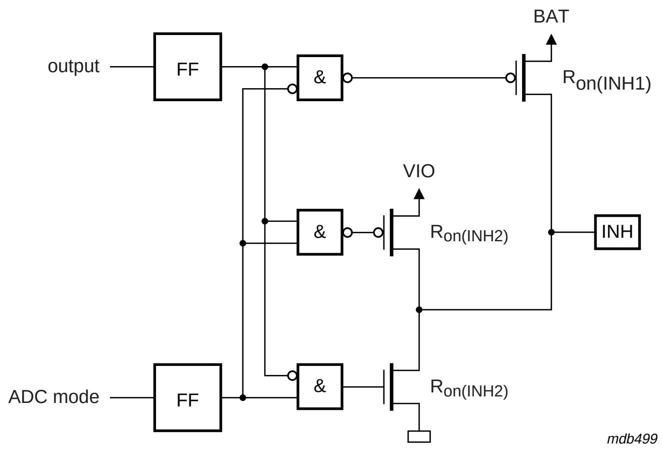


Fig 11. INH structure

7.4 Configuration pins C1 to C3

The structure of the configuration pins C1 to C3 (Cx) is shown in Figure 12. Each pin has a pull-up to the battery. The pull-up is switched on during node address configuration only. In all other cases the Cx have high-impedance behavior.

In order to have a safety margin against ground shift the input threshold of the configuration pins is about $0.5 \times V_{BAT}$.

In addition the configuration pin C3 has a low-side driver to provide the output signal during daisy chain ID configuration.

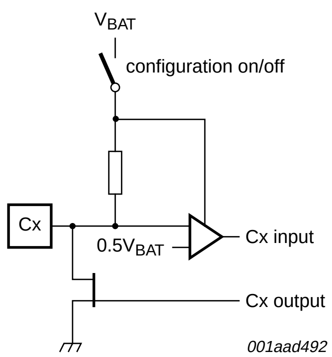


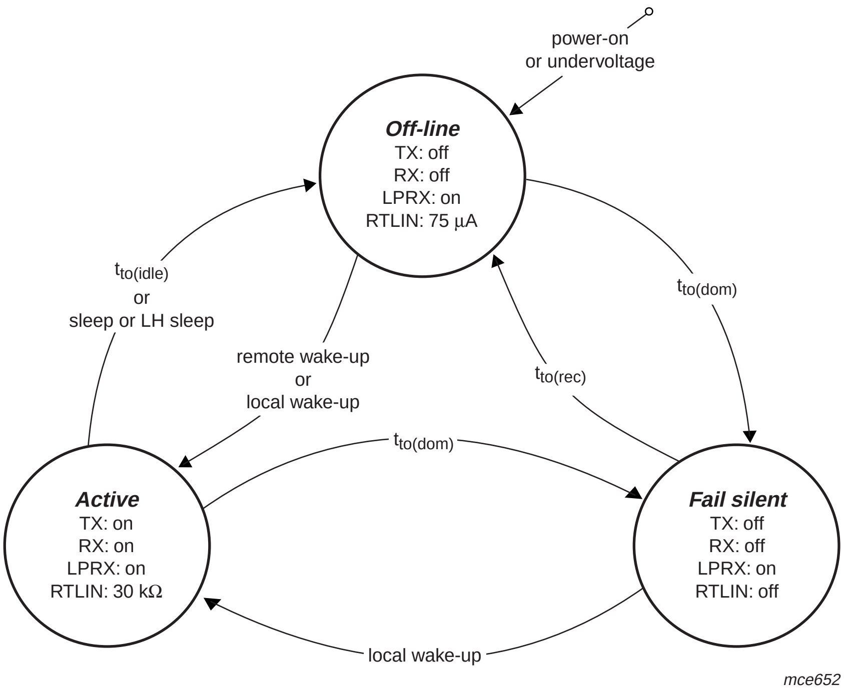
Fig 12. Configuration pin structure

7.5 LIN transceiver

The integrated LIN transceiver of the UJA1023 is compliant with LIN 2.0 / SAE J2602 and provides:

- Integrated 30 kΩ termination resistor
- Internal LIN-termination switch (RTLIN)
- Disabling of termination switch during a short-circuit from LIN to GND

Figure 13 shows the states of the complete LIN transceiver including RTLIN for LIN termination.



TX = Transmitter.

RX = Receiver.

LPRX = Low-power receiver.

RTLIN = LIN termination.

Fig 13. LIN transceiver states

The first mode after power-on is the Off-line mode. The transmitter and receiver are both switched off, but wake-up events will be recognized. Any LIN wake-up event will wake-up the UJA1023.

Within Sleep mode any wake-up event is automatically forwarded to the LIN (protocol) controller, the Normal mode will be entered and the LIN-transceiver automatically enters the Active mode. It should be noted that the first message (wake-up message) will be lost when no wake-up signal has been received before.

The differences between Active, Off-line and Fail silent mode are:

- In Off-line and Fail silent mode the transmitter is off, whereas in Active mode the transmitter is enabled.
- During active state with no short-circuit between LIN and GND the internal termination switch RTLIN provides an internal 30 kΩ pull-up resistor to V_{BAT}. In case the LIN wire is shorted to GND for longer than $t_{to(dom)}$, the RTLIN switch switches off in order to make sure that no current is discharging the battery unintentionally and Fail silent mode will be entered.
- After failure recovery (in fail silent) when the LIN bus is recessive again the Off-line mode is entered and activates a weak termination of 75 µA.

- Entering Active mode out of Off-line mode results always in switching on the internal 30 kΩ pull-up resistor to battery.

7.6 On-chip oscillator

The on-chip oscillator is the time reference for all timers in the LIN controller, auto bit rate detector, ADC and LIN transceiver.

A too-low frequency of the on-chip oscillator or a not-running on-chip oscillator results immediately in Limp home operating mode.

8. Limiting values

Table 30: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BAT}	supply voltage on pin BAT			–0.3	+40	V
V_{VIO}	supply voltage on pin VIO			–0.3	V_{BAT} + 0.3	V
V_{LIN}	voltage on pin LIN	DC value		–27	+40	V
V_{INH}	voltage on pin INH	DC value		–0.3	V_{BAT} + 0.3	V
V_{Cx}	voltage on pins C1 to C3	DC value		–27	+40	V
V_{Px}	voltage on pins P0 to P7	DC value		–0.3	V_{VIO} + 0.3	V
I_{Px}	current on pins P0 to P7	DC value; $V_{Px} > V_{VIO} + 0.3$ V; $V_{Px} < -0.3$ V		–15	+15	mA
$V_{trt(LIN)}$	transient voltages on pin LIN	ISO 7637		–150	+100	V
T_{vj}	virtual junction temperature		[1]	–40	+150	°C
T_{stg}	storage temperature			–55	+150	°C
V_{esd}	electrostatic discharge voltage					
	pins BAT, LIN, C1, C2 and C3	human body model; C = 100 pF; R = 1.5 kΩ		–8	+8	kV
	corner pins	charged device model		–750	+750	V
	other pins	human body model; C = 100 pF; R = 1.5 kΩ		–2	+2	kV
		charged device model		–500	+500	V

[1] Junction temperature in accordance with IEC60747-1. An alternative definition of $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value to be used for calculating T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9. Thermal characteristics

Table 31: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	106	K/W

10. Static characteristics

Table 32: Static characteristics

V_{BAT} = 6.5 V to 27 V; V_{VIO} = 3 V to 27 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are referenced to GND; positive current flows into the IC; unless otherwise specified. [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply: pin BAT							
V_{BAT}	supply voltage on pin BAT	all operating modes		6.5	-	27	V
I_{BAT}	supply current on pin BAT	LH sleep, Sleep and Limp home mode	[2]	-	45	65	µA
		Normal mode; LIN receiving recessive					
		V_{BAT} = 12 V	[3]	-	0.7	1.4	mA
		V_{BAT} = 27 V	[3]	-	1.0	2.0	mA
		Normal mode; LIN receiving dominant					
		V_{BAT} = 12 V	[3]	-	1.1	2.2	mA
		V_{BAT} = 27 V	[3]	-	1.7	3.4	mA
		Normal mode; LIN sending dominant					
		V_{BAT} = 12 V	[3]	-	2.2	4.4	mA
		V_{BAT} = 27 V	[3]	-	3.6	7.5	mA
		Additional current if all high- and low-side switches are activated		-	1040	1280	µA
$V_{BAT(pf)}$	V_{BAT} power fail detection voltage		[4]	4.45	-	5.0	V
I/O reference (Px operating range): pin VIO							
V_{VIO}	supply voltage on pin VIO			3	-	V_{BAT} + 0.3	V
I_{VIO}	supply current on pin VIO	LH sleep, Sleep and Limp home mode; no load at Px					
		high-side switches disabled	[5]	-	1.6	5.0	µA
		high-side switches enabled and active	[5]	-	230	280	µA
		Normal mode; ADC enabled; no load at Px and INH; high-side switches enabled	[5]	-	520	1000	µA
Configuration: pins C1, C2 and C3							
V_{IH}	HIGH-level input voltage			0.6 × V_{BAT}	-	V_{BAT} + 0.3	V
V_{IL}	LOW-level input voltage			−0.3	-	0.4 × V_{BAT}	V
$\lvert I_L \rvert$	leakage current	configuration pins disabled		-	-	5	µA
R_{pu}	internal pull-up resistor	configuration pins enabled		5	11	25	kΩ
$V_{OL(C3)}$	LOW-level output voltage on pin C3	external R_{pu} = 5 kΩ to pin BAT; C3 enabled		-	-	0.2 × V_{BAT}	V

Table 32: Static characteristics *…continued*

V_{BAT} = 6.5 V to 27 V; V_{VIO} = 3 V to 27 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are referenced to GND; positive current flows into the IC; unless otherwise specified. [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{sc(C3)}$	short-circuit current on pin C3	C3 = V_{BAT}; C3 enabled		-	-	50	mA
I/O: pins P0 to P7							
$V_{IH(th1)}$	HIGH-level input voltage V_{th1}	$V_{VIO} \geq 3.7$ V		3.7	-	V_{VIO} + 0.3	V
$V_{IL(th1)}$	LOW-level input voltage V_{th1}	$V_{VIO} \geq 3.7$ V		−0.3	-	+2.1	V
$V_{IH(th2)}$	HIGH-level input voltage V_{th2}			2.0	-	V_{VIO} + 0.3	V
$V_{IL(th2)}$	LOW-level input voltage V_{th2}			−0.3	-	+0.8	V
$V_{IH(th3)}$	HIGH-level input voltage V_{th3}	$V_{VIO} \geq 10$ V		V_{VIO} − 0.8	-	V_{VIO} + 0.3	V
$V_{IL(th3)}$	LOW-level input voltage V_{th3}	$V_{VIO} \geq 10$ V		−0.3	-	V_{VIO} − 2.5	V
$\lvert I_L \rvert$	leakage current	$V_I = V_{VIO}$ or GND		-	-	10	µA
$R_{on(HS)}$	high-side on-state resistance	$V_{Px} = V_{VIO}$ − 1 V; per switch		550	1200	3000	Ω
$I_{sc(HS)}$	high-side short-circuit current	V_{Px} = 0 V	[6]	−3.1	−2.0	−0.8	mA
$R_{on(LS)}$	low-side on-state resistance	V_{Px} = 1 V; per switch		25	50	83	Ω
$I_{sc(LS)}$	low-side short-circuit current	$V_{Px} = V_{VIO}$	[6]	10	23	40	mA
Special function: pin INH							
$V_{BAT-INH}$	voltage drop	INH mode; I_{INH} = −1 mA		-	1.2	1.8	V
$\lvert I_L \rvert$	leakage current	V_{INH} = 0 V		-	-	5	µA
Bus line: pin LIN							
$V_{O(dom)}$	LIN dominant output voltage	7.0 V < V_{BAT} < 18 V		0	-	0.2 × V_{BAT}	V
$I_{L(H)}$	HIGH-level leakage current	7.0 V < V_{BAT} < 18 V; $V_{LIN} = V_{BAT}$		−10	-	+10	µA
$I_{L(L)}$	LOW-level leakage current	Fail silent mode; V_{LIN} = 0 V; $t > t_{to(dom)}$		−10	0	+10	µA
I_{pu}	LIN pull-up current	Off-line mode; V_{LIN} = 0 V; $t < t_{to(dom)}$		−150	−60	−10	µA
$R_{pu(slave)}$	slave termination pull-up	Active mode		20	30	47	kΩ
I_L	leakage current	V_{BAT} = 0 V	[7]	-	0	-	µA
$I_{O(sc)}$	short-circuit output current	LIN dominant; $t < t_{to(dom)}$					
		V_{LIN} = 12 V; V_{BAT} = 12 V		27	40	60	mA
		V_{LIN} = 18 V; V_{BAT} = 18 V		40	60	86	mA
$V_{th(dom)}$	receiver dominant state voltage	Active mode		-	-	0.4 × V_{BAT}	V
$V_{th(rec)}$	receiver recessive state voltage	Active mode		0.6 × V_{BAT}	-	-	V
$V_{cen(RX)}$	receiver center voltage	Active mode		0.475 × V_{BAT}	0.5 × V_{BAT}	0.525 × V_{BAT}	V
$V_{hys(RX)}$	receiver hysteresis voltage	Active mode		0.05 × V_{BAT}	-	0.175 × V_{BAT}	V

[1] All parameters are guaranteed over the virtual junction temperature range by design. Products are 100 % tested at 125 °C ambient temperature on wafer level (pre-testing). Cased products are 100 % tested at 25 °C ambient temperature (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] All outputs turned off, LIN recessive, V_{th1} selected.

[3] All outputs turned off.

[4] Configuration is lost when V_{BAT} is below 5 V.

[5] V_{th1} on, V_{th2} off, V_{th3} off.

[6] Outputs are not temperature protected.

[7] Not tested in production.

11. Dynamic characteristics

Table 33: Dynamic characteristics

V_{BAT} = 6.5 V to 27 V; V_{VIO} = 3 V to 27 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are referenced to GND; unless otherwise specified. [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I/O processing							
$t_{process}$	PxReq to output	after valid LIN message	[2]	-	200	-	µs
$t_{conv(ADC)}$	conversion time ADC		[2] [3]	-	1.5	-	ms
LIN transceiver; see Figure 14 [4]							
δ1	duty cycle 1	$V_{th(rec)(max)} = 0.744 \times V_{BAT}$; $V_{th(dom)(max)} = 0.581 \times V_{BAT}$; LSC = 0; t_{bit} = 50 µs; V_{BAT} = 7 V to 18 V	[5]	0.396	-	-	
δ2	duty cycle 2	$V_{th(rec)(min)} = 0.422 \times V_{BAT}$; $V_{th(dom)(min)} = 0.284 \times V_{BAT}$; LSC = 0; t_{bit} = 50 µs; V_{BAT} = 7.6 V to 18 V	[6]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)} = 0.778 \times V_{BAT}$; $V_{th(dom)(max)} = 0.616 \times V_{BAT}$; LSC = 1; t_{bit} = 96 µs; V_{BAT} = 7 V to 18 V	[5]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)(min)} = 0.389 \times V_{BAT}$; $V_{th(dom)(min)} = 0.251 \times V_{BAT}$; LSC = 1; t_{bit} = 96 µs; V_{BAT} = 7.6 V to 18 V	[6]	-	-	0.590	
$t_{PHL(RX)}$, $t_{PLH(RX)}$	propagation delay of receiver		[7]	-	-	6	µs
$t_{P(RX)(sym)}$	symmetry of receiver propagation delay rising edge with respect to falling edge		[7]	−2	-	+2	µs
LIN protocol controller							
$t_{to(idle)}$	bus idle time-out			4.1	-	18.0	s
$t_{to(dom)}$	bus dominant time-out			32	-	270	ms
$t_{to(rec)}$	bus recessive time-out			15	-	65	µs
$t_{wake(bus)}$	network wake-up signal time	after local wake-up, sent by slave		0.25	-	5	ms
$t_{wake(local)}$	bus wake-up dominant time	Sleep mode, sent by master		30	100	150	µs
Automatic bit rate detection							
$t_{det(syncbrk)}$	sync break detection threshold			-	10	-	t_{bit}

Table 33: Dynamic characteristics *…continued*

V_{BAT} = 6.5 V to 27 V; V_{VIO} = 3 V to 27 V; T_{vj} = –40 °C to +150 °C; $R_{L(LIN-BAT)}$ = 500 Ω; all voltages are referenced to GND; unless otherwise specified. [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{tol(sync)}$	total tolerance slave synchronized	complete message		-	-	2	%
Cyclic function; see Figure 7							
T_{cy}	cycle period			-	16	-	ms
$t_{on(PxOut)}$	PxOut pin turned on			-	350	-	µs
$t_{sample(PxIn)}$	PxIn sample time			-	262	-	µs
ADC function							
E_{ADC}	total ADC error	R = 100 kΩ; C = 10 nF					
		V_{VIO} = 6.5 V to 12 V; V_{BAT} = 6.5 V to 12 V	[8]	-	-	4	LSB
		V_{VIO} = 3 V to 27 V; V_{BAT} = 6.5 V to 27 V	[8]	-	-	6	LSB

[1] All parameters are guaranteed over the virtual junction temperature range by design. Products are 100 % tested at 125 °C ambient temperature on wafer level (pre-testing). Cased products are 100 % tested at 25 °C ambient temperature (final testing). Both pre-testing and final testing use correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] Guaranteed by design.

[3] Analog-to-digital conversion starts when valid sync break and sync field is received.

[4] t_{bit} = selected bit time 50 µs or 96 µs (20 kbit/s or 10.4 kbit/s), depends on LSC bit; bus load conditions are (C parallel to R): C_{bus} = 1 nF and R_{bus} = 1 kΩ, C_{bus} = 6.8 nF and R_{bus} = 660 Ω or C_{bus} = 10 nF and R_{bus} = 500 Ω.

[5] $$\delta_1, \delta_3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$$

[6] $$\delta_2, \delta_4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$$

[7] RXD is an internal signal.

[8] Not tested.

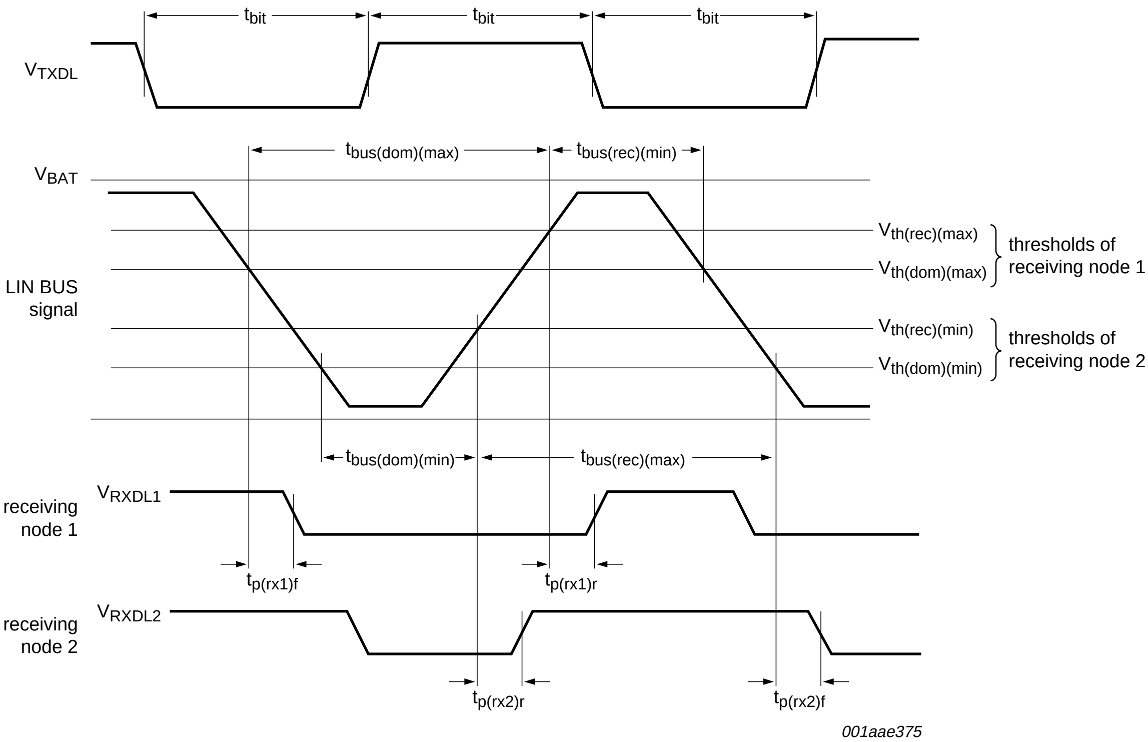


Fig 14. Timing diagram LIN transceiver

12. Application information

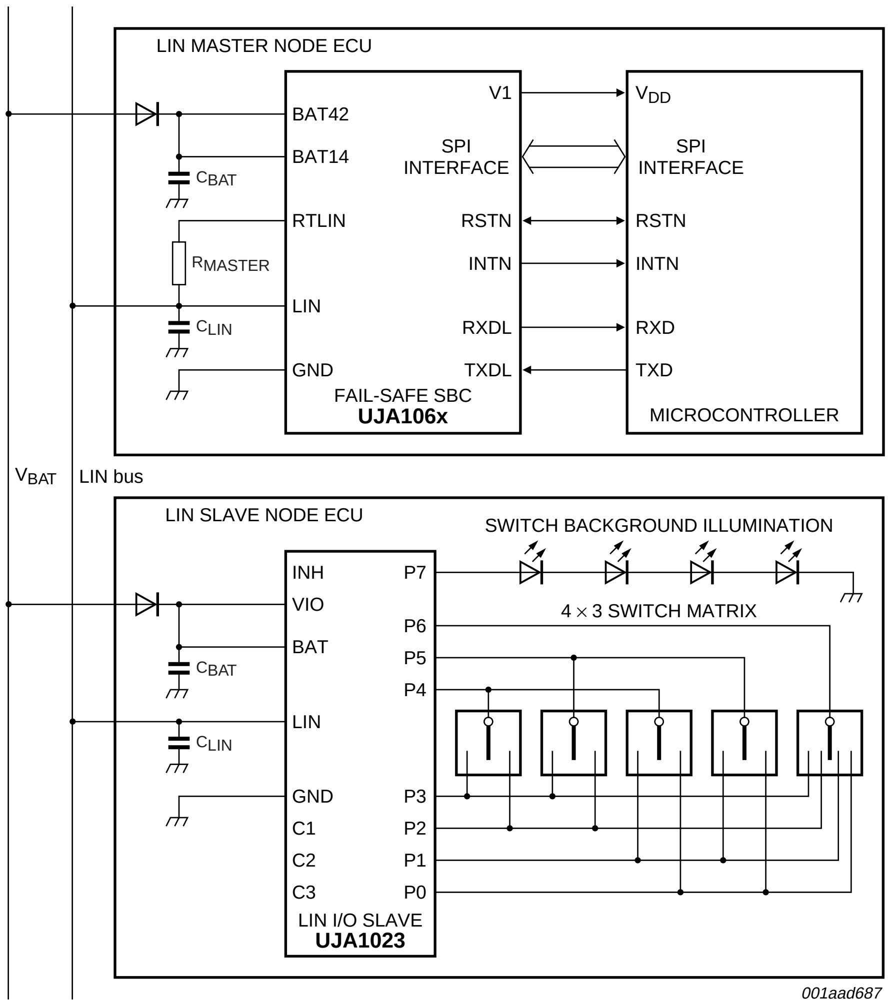


Fig 15. Application Diagram

13. Test information

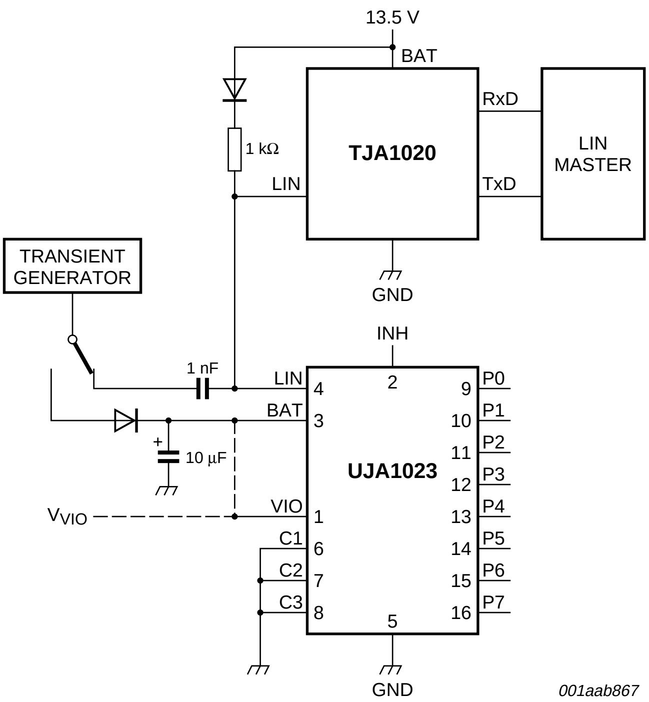


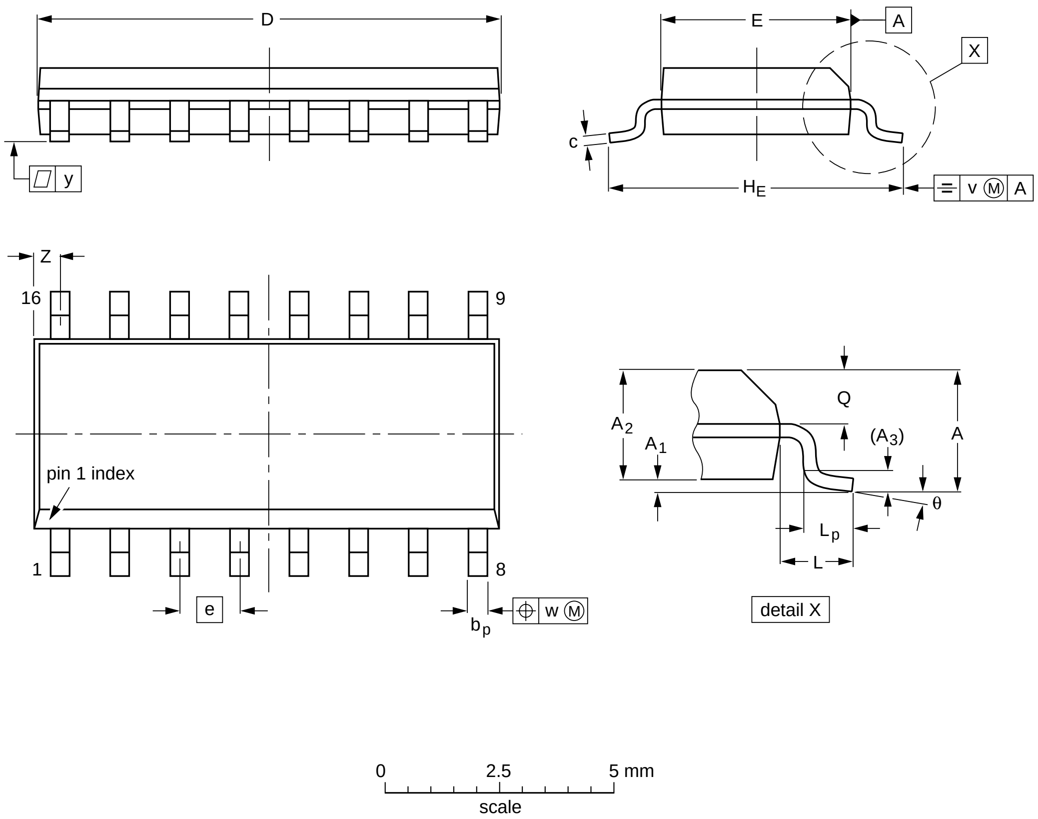
Fig 16. Test circuit for automotive transients

13.1 Quality information

Quality specification in accordance with AEC-Q100.

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT109-1 (SO16)

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

   – smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 34: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	**Soldering method**	
	Wave	**Reflow** [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Revision history

Table 35: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
UJA1023_3	20060209	Preliminary data sheet	-	-	UJA1023_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Table 30 “Limiting values”: updated. • Table 32 “Static characteristics”: updated. • Table 33 “Dynamic characteristics”: updated. • Figure 6 “Overview of operating modes”: updated. • Figure 14 “Timing diagram LIN transceiver”: updated. • Updated various other tables, figures and texts in order to make signal names consistent.				
UJA1023_2	20050203	Objective specification	-	9397 750 12022	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

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