Data Sheet | August 1999 | File Number 4231.2

95MHz, Low Power, A_V = 2, 8 x 8 Video Crosspoint Switch

The HA457 is an 8 x 8 video crosspoint switch suitable for high performance video systems. Its high level of integration significantly reduces component count, board space, and cost. The crosspoint switch contains a digitally controlled matrix of 64 fully buffered switches that connect eight video input signals to any, or all, matrix outputs. Each matrix output connects to an internal, high-speed (275V/µs), gain of two buffer capable of driving 150Ω to ±2.5V.

The HA457 will directly drive a double terminated video cable with some degradation of differential gain and phase. Applications demanding the best composite video performance should drive the cable with a unity gain video buffer, such as the HFA1412 quad buffer (see Figure 7).

This crosspoint's three-state output capability makes it feasible to parallel multiple HA457s and form larger switch matrices.

Features

- Pin Compatible, Cable Driving Upgrade for HA456 and MAX456
- Fully Buffered Inputs and Outputs (A_V = +2)
- Routes Any Input Channel to Any Output Channel
- Switches Standard and High Resolution Video Signals
- Serial or Parallel Digital Interface
- Expandable for Larger Switch Matrices
- Wide Bandwidth 95MHz
- High Slew Rate. 275V/µs
- Low Crosstalk at 10MHz . . . . . -55dB

Applications

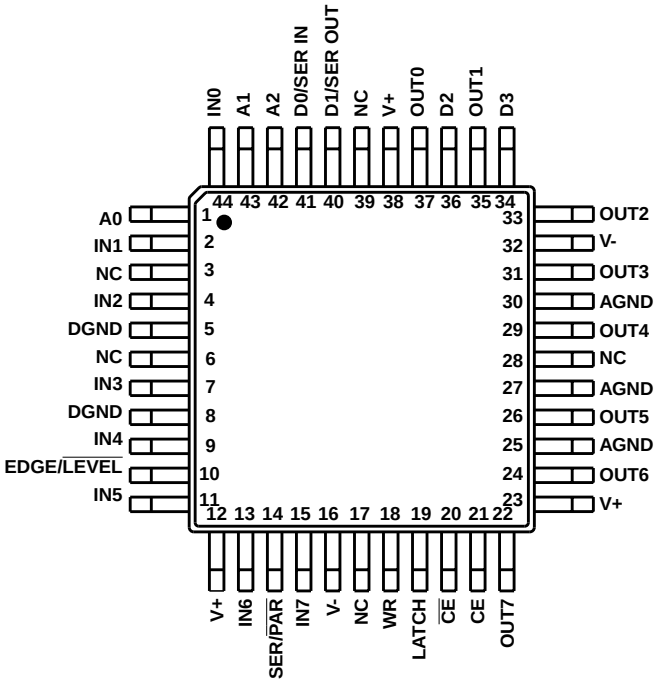
- Video Switching and Routing
- Security and Video Editing Systems

Ordering Information

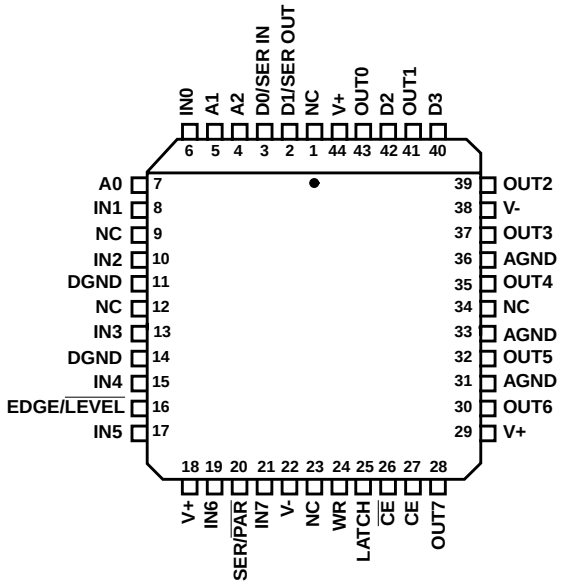
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HA457CN	0 to 70	44 Ld MQFP	Q44.10x10
HA457CM	0 to 70	44 Ld PLCC	N44.65

Pinouts

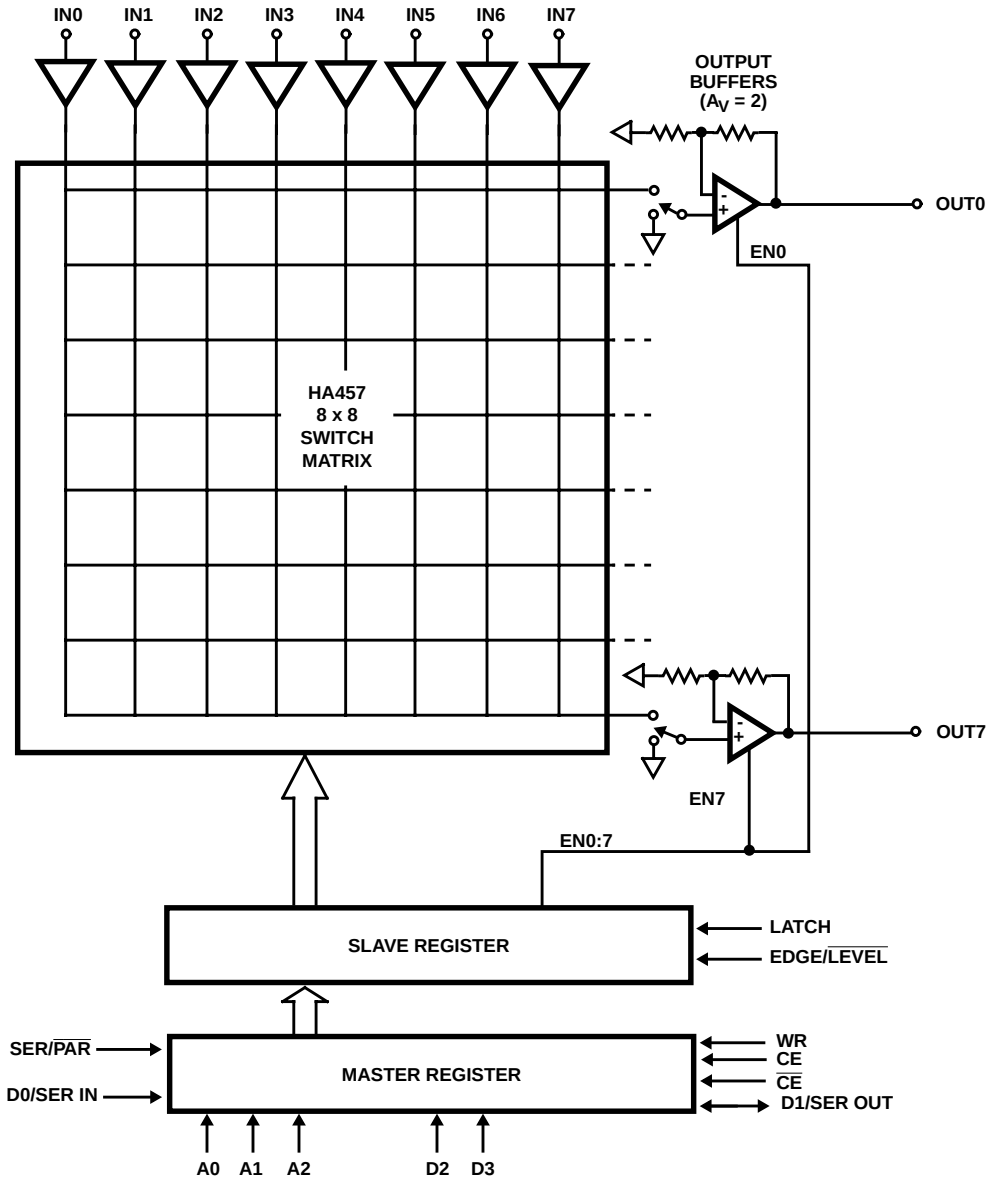
HA457 (MQFP)
TOP VIEW



HA457 (PLCC)
TOP VIEW



Functional Block Diagram



Pin Descriptions

PIN		NAME	FUNCTION
MQFP	PLCC		
3, 6, 17, 28, 39	1, 9, 12, 23, 34	NC	No connect. Not internally connected.
40	2	D1/ SER OUT	Parallel Data Bit input D1 for parallel programming mode. Serial Data Output (MSB of shift register) for cascading multiple HA457s in serial programming mode. Simply connect Serial Data Out of one HA457 to Serial Data In of another HA457 to daisy chain multiple devices.
41	3	D0/SER IN	Parallel Data Bit input D0 for parallel programming mode. Serial Data Input (input to shift register) for serial programming mode.
42, 43, 1	4, 5, 7	A2, A1, A0	Output Channel Address Bits. These inputs select the output being programmed in parallel programming mode.
44, 2, 4, 7, 9, 11, 13, 15	6, 8, 10, 13, 15, 17, 19, 21	IN0-IN7	Analog Video Input Lines.
5, 8	11, 14	DGND	Digital Ground. Connect both DGND pins to AGND.
10	16	EDGE/$\overline{\text{LEVEL}}$	A user strapped input that defines whether synchronous channel switching is edge or level controlled. With this pin strapped high, the slave register loads from the master register (thus changing the switch matrix state) on the rising edge of the LATCH signal. If it is strapped low (level mode), the slave register is transparent while LATCH is low, passing data directly from the master register to the switch state decoders. Strapping EDGE/$\overline{\text{LEVEL}}$ and LATCH low causes the channel switch to execute on the WR rising edge (not recommended for serial mode operation).
12, 23, 38	18, 29, 44	V+	Positive supply voltage. Connect all V+ pins together and decouple each pin to AGND (Figure 6).
14	20	SER/$\overline{\text{PAR}}$	A user strapped input that defines whether the serial (SER/$\overline{\text{PAR}}$=1) or parallel (SER/$\overline{\text{PAR}}$=0) digital programming interface is being utilized.
16, 32	22, 38	V-	Negative supply voltage. Connect both V- pins together and decouple each pin to AGND (Figure 6).
18	24	WR	WRITE Input. In serial mode, data shifts into the shift register (Master Register) LSB from SER IN on the WR rising edge. In parallel mode, the Master Register loads with D3:0 (iff D3:0=0000 through 1000), or the appropriate action is taken (iff D3:0=1011 through 1111), on the WR rising edge (see Table 1).
19	25	LATCH	Synchronous channel switch control input. If EDGE/$\overline{\text{LEVEL}}$ = 1, data is loaded from the Master Register to the Slave Register on the rising edge of LATCH. If EDGE/$\overline{\text{LEVEL}}$ = 0, data is loaded from the Master to the Slave Register while LATCH = 0. In parallel mode, commands 1011 through 1110 execute asynchronously, on the WR rising edge, regardless of the state of LATCH or EDGE/$\overline{\text{LEVEL}}$. Parallel mode command 1111 executes a software “Latch” (see Table 1).
20	26	$\overline{\text{CE}}$	$\overline{\text{Chip Enable}}$. When $\overline{\text{CE}}$ = 0 and CE = 1, the WR line is enabled.
21	27	CE	Chip Enable. When $\overline{\text{CE}}$ = 0 and CE = 1, the WR line is enabled.
22, 24, 26, 29, 31, 33, 35, 37	28, 30, 32, 35, 37, 39, 41, 43	OUT7-OUT0	Analog Video Outputs.
25, 27, 30	31, 33, 36	AGND	Analog Ground.
34	40	D3	Parallel Data Bit Input D3 when SER/$\overline{\text{PAR}}$ = 0. D3 is unused with serial programming.
36	42	D2	Parallel Data Bit Input D2 when SER/$\overline{\text{PAR}}$ = 0. D2 is unused with serial programming.

Absolute Maximum Ratings

Supply Voltage (V+ to V-) 12V
Positive Supply Voltage (V+) Referred to AGND 6V
Negative Supply Voltage (V-) Referred to AGND . . . . . -6V
DGND Voltage . . . . . AGND ±1V
Analog Input Voltage . . . . . $\pm V_{SUPPLY}$
Digital Input Voltage . . . . . (V+ + 0.3V) to (DGND - 0.3V)
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 1.6kV

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
PLCC Package	50
MQFP Package	70

Maximum Junction Temperature (Die) . . . . . 175^{o}C
Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature, Soldering 10s . . . . . 300^{o}C
(Lead Tips Only)

Operating Conditions

Temperature Range . . . . . 0^{o}C to 70^{o}C
Supply Voltage Range (Typical) . . . . . ±4.5V to ±5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±5V, AGND = DGND = 0V, R_L = 400Ω (Note 2), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (^{o}C)	MIN	TYP	MAX	UNITS
Voltage Gain	V_{IN} = -0.75V to +0.75V, Worst Case Switch Configuration, R_L = 150Ω	A	25	1.93	1.97	2.10	V/V
		A	Full	-	-	-	
Channel-to-Channel Gain Mismatch		A	25	-	0.04	0.1	V/V
		A	Full	-	-	-	
Supply Current	All Outputs Enabled, R_L = Open, V_{IN} = 0V, Total for All V+ (3) or V- (2) Pins	A	25	-	68	80	mA
		A	Full	-	71	83	
Disabled Supply Current	All Outputs Disabled, R_L = Open, Total for All V+ (3) or V- (2) Pins	A	25	-	47	65	mA
		A	Full	-	47	67	
Input Voltage Range		A	Full	±2	±2.5	-	V
Analog Input Current	V_{IN} = 0V	A	Full	-	1.6	12	µA
Input Noise (R_S = 75Ω)	DC to 40MHz	B	25	-	0.15	-	mV_{RMS}
	≥10kHz	B	25	-	22	-	$nV/\sqrt{Hz}$
Analog Input Resistance	DC	C	25	-	4	-	MΩ
Analog Input Capacitance (Input Connected to One Output or All Outputs, Note 6)	PLCC Package	B	25	-	3.2	-	pF
	MQFP Package	B	25	-	2.5	-	pF
Input Offset Voltage	V_{IN} = 0V, Worst Case Switch Configuration	A	25	-18	-12	5	mV
		A	Full	-20	-15	6	
Channel-to-Channel Input Offset Voltage Mismatch		A	25	-	4	11	mV
		A	Full	-	8	-	
Input Offset Voltage Drift		B	Full	-	20	-	µV/^{o}C
Output Voltage Swing	V_{IN} = ±1.33V, R_L = 150Ω	A	25	±2.45	±2.6	-	V
		A	Full	-	-	-	V
Output Resistance	Enabled, DC	B	25	-	0.25	-	Ω
	Output Disabled	A	25	1.5	2	-	kΩ
Output Capacitance (Output Disabled)	PLCC Package	B	25	-	3.5	-	pF
	MQFP Package	B	25	-	2.9	-	pF
Power Supply Rejection Ratio	DC, V_S = ±4.5V to ±5.5V, V_{IN} = 0V	A	Full	45	53	-	dB
Digital Input Current (Note 5)	V_{IN} = 0V or 5V	A	Full	-	-	1	µA

Electrical Specifications V_{SUPPLY} = ±5V, AGND = DGND = 0V, R_L = 400Ω (Note 2), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP (^oC)	MIN	TYP	MAX	UNITS
Digital Input Low Voltage		A	Full	-	-	0.8	V
Digital Input High Voltage		A	25	2.0	-	-	V
		A	Full	2.2	-	-	V
SER OUT Logic Low Voltage	Serial Mode, I_{OL} = 1.6mA	A	Full	-	-	0.4	V
SER OUT Logic High Voltage	Serial Mode, I_{OH} = -0.4mA	A	Full	3.0	-	-	V
SER OUT Leakage Current	Output Disabled, V_{OUT} = 2.5V	A	25	-	0.2	5	µA
		A	Full	-	1	10	µA
AC CHARACTERISTICS (Note 4)							
-3dB Bandwidth (Note 6)	V_{OUT} = 200mV_{P-P}	B	25	-	95	-	MHz
	V_{OUT} = 1V_{P-P}	B	25	-	75	-	MHz
	V_{OUT} = 2V_{P-P}	B	25	-	60	-	MHz
	V_{OUT} = 2V_{P-P}, R_L= 150Ω	B	25	-	50	-	MHz
Slew Rate (Note 6)	V_{OUT} = 4V_{P-P}, R_L = 150Ω	B	25	-	275	-	V/µs
All Hostile Crosstalk (Note 6)	10MHz, V_{IN} = 1V_{P-P}, R_L = 150Ω	B	25	-	-55	-	dB
	10MHz, V_{IN} = 1V_{P-P}, R_L = 1kΩ	B	25	-	-58	-	dB
All Hostile Off Isolation (Note 6)	10MHz, V_{IN} = 1V_{P-P}, R_L = 150Ω	B	25	-	95	-	dB
	10MHz, V_{IN} = 1V_{P-P}, R_L = 1kΩ	B	25	-	75	-	dB
Differential Phase	NTSC or PAL, R_L = 150Ω	B	25	-	0.5	-	DEG
	NTSC or PAL, R_L = 1kΩ	B	25	-	0.05	-	DEG
	NTSC or PAL, $R_L \geq$ 10kΩ	B	25	-	0.05	-	DEG
Differential Gain	NTSC or PAL, R_L = 150Ω	B	25	-	0.05	-	%
	NTSC or PAL, R_L = 1kΩ	B	25	-	0.05	-	%
	NTSC or PAL, $R_L \geq$ 10kΩ	B	25	-	0.02	-	%
TIMING CHARACTERISTICS (See Figure 8 for more information)							
Write Pulse Width High (t_{WH})		A	Full	20	-	-	ns
Write Pulse Width Low (t_{WL})		A	Full	20	-	-	ns
Chip-Enable Setup Time to Write (t_{CS})		A	Full	5	-	-	ns
Chip-Enable Hold Time From Write (t_{CH})		A	Full	5	-	-	ns
Data and Address Setup Time to Write (t_{DS})	Parallel Mode	A	Full	20	-	-	ns
	Serial Mode	A	Full	20	-	-	ns
Data and Address Hold Time From Write (t_{DH})		A	Full	25	-	-	ns
Latch Pulse Width (t_L)		A	Full	40	-	-	ns
Latch Delay From Write (t_D)		A	Full	40	-	-	ns
LATCH Edge to Output Disabled (t_{OFF})	Serial Mode	B	Full	-	30	-	ns
LATCH Edge to Output Enabled (t_{ON})	Serial Mode	B	Full	-	185	-	ns
Output Break-Before-Make Delay (t_{ON} - t_{OFF})	Serial Mode	B	Full	-	155	-	ns

NOTES:

2. For the lowest crosstalk, and the best composite video performance, use $R_L \geq$ 1kΩ.
3. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
4. See AC Test Circuits (Figure 1 through Figure 4).
5. Excludes D1/SER OUT which is a bidirectional terminal and thus falls under the higher Output Leakage limit.
6. See Typical Performance Curves for more information.

AC Test Circuits

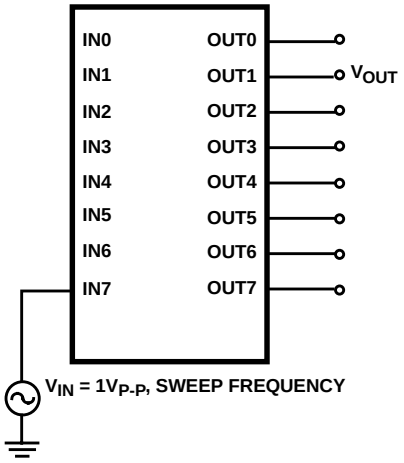


FIGURE 1. -3dB BANDWIDTH (NOTES 7-10)

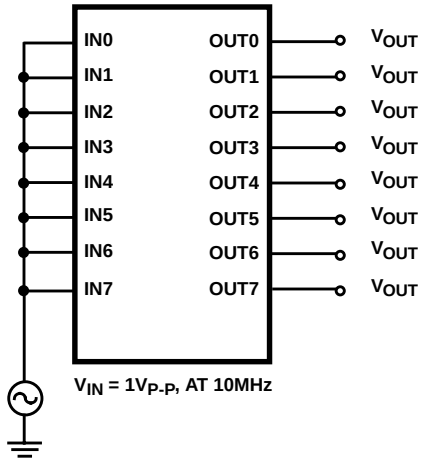


FIGURE 2. ALL HOSTILE OFF ISOLATION (NOTES 10-12)

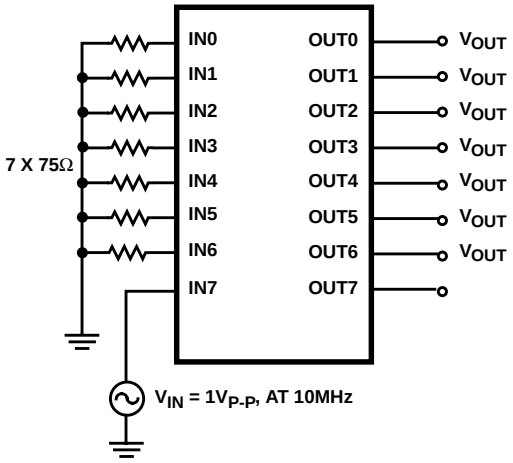


FIGURE 3. SINGLE CHANNEL CROSSTALK (NOTES 10, 13-16)

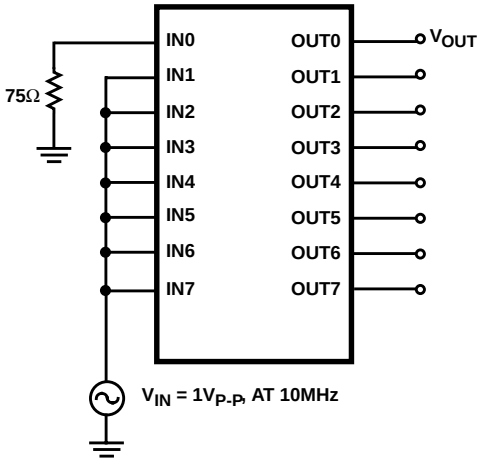


FIGURE 4. ALL HOSTILE CROSSTALK (NOTES 10, 15, 17-19)

NOTES:

7. Program the desired input to output combination (e.g., IN7 to OUT1).
8. Enable the selected output(s).
9. Drive the selected input with V_{IN}, and measure the -3dB frequency at the selected output (V_{OUT}).
10. Load all outputs with the desired R_L.
11. Disable all outputs.
12. Drive all inputs with V_{IN} and measure V_{OUT} at any output; Isolation (in dB) = $-20\log_{10} (V_{OUT}/V_{IN})$.
13. Drive V_{IN} on one input which connects to one output (e.g., IN7 to OUT7).
14. Terminate all other inputs to GND.
15. Enable all outputs.
16. Measure V_{OUT} at any undriven output; Crosstalk (in dB) = $20\log_{10} (V_{OUT}/V_{IN})$.
17. Terminate one input to GND, and connect that input to a single output (e.g., IN0 to OUT0).
18. Drive the other seven inputs with V_{IN}, and connect these active inputs to the remaining seven outputs.
19. Measure V_{OUT} at the quiescent output; Crosstalk (in dB) = $20\log_{10} (V_{OUT}/V_{IN})$.

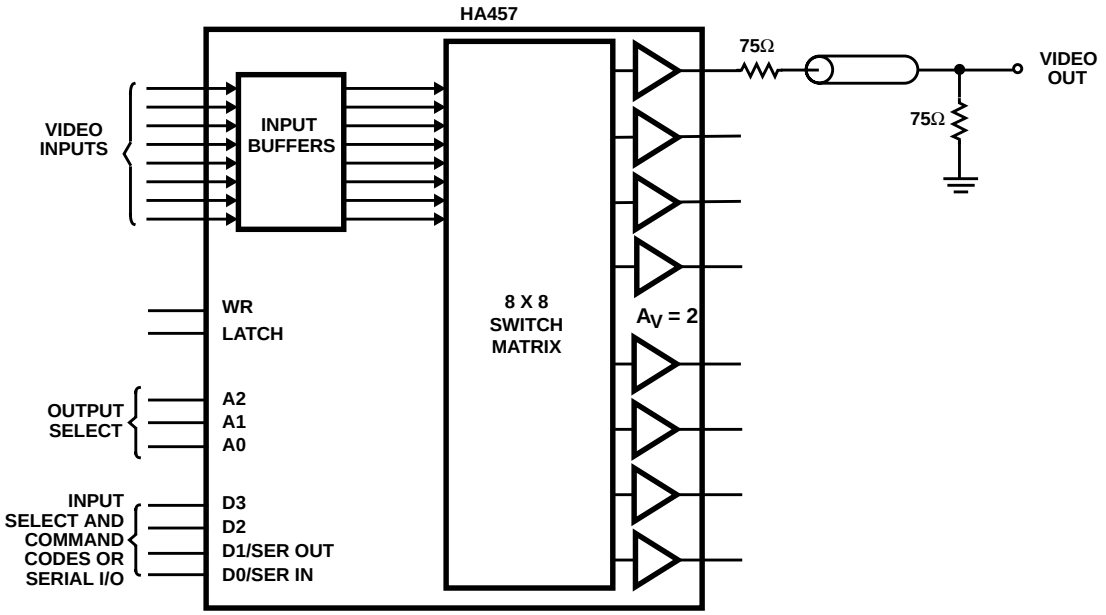


FIGURE 5. TYPICAL CABLE DRIVING APPLICATION

Application Information

HA457 Architecture

The HA457 video crosspoint switch consists of 64 switches in an 8 x 8 grid (Figure 5). Each input is fully buffered and presents a constant input capacitance whether the input connects to one output or all eight outputs. This yields consistent input termination impedances regardless of the switch configuration. The 8 matrix outputs are followed by 8 gain of 2, wideband, three-stateable buffers optimized for driving 1kΩ loads. Double terminated video cables (R_L = 150Ω) may be driven if degraded differential phase is acceptable (see “Electrical Specification” Table). The output disable function is useful for multiplexing two or more HA457s to create a larger input matrix (e.g., two multiplexed HA457s yield a 16x8 crosspoint).

The HA457 outputs can be disabled individually or collectively under software control. When disabled, an output enters a pseudo high-impedance state (R_{OUT} = 2kΩ). In multichip parallel applications, the disable function prevents inactive outputs from loading lines driven by other devices. Disabling an unused output also reduces power consumption.

The HA457 outputs connect easily to two HFA1412 quad, unity gain buffers when 75Ω loads must be driven with excellent differential phase (see Figures 7 and 21). The bandwidth improves to 120MHz, while differential gain and differential phase improve to 0.03% and 0.09 degrees, respectively.

Power-On RESET

The HA457 has an internal power-on reset (POR) circuit that **disables all outputs at power-up**, and presets the switch matrix so that all outputs connect to IN0. In parallel mode, the desired switch state may be programmed before the outputs are enabled. In serial mode, all outputs are connected to GND each time they are enabled, so switch state programming must occur after the output is enabled.

Digital Interface

The desired switch state can be loaded using a 7-bit parallel interface mode or 32-bit serial interface mode (see Tables 1 through 3). All actions associated with the WR line occur on its rising edge. The same is true for the LATCH line if EDGE/$\overline{\text{LEVEL}}$=1. Otherwise, the Slave Register updates asynchronously (while LATCH=0, if EDGE/$\overline{\text{LEVEL}}$=0). WR is logically ANDed with CE and $\overline{\text{CE}}$ to allow active high or active low chip enable.

7-Bit Parallel Mode

In the parallel programming mode (SER/$\overline{\text{PAR}}$ = 0), the 7 control bits (A2:0 and D3:0) typically specify an output channel (A2:0) and the corresponding action to be taken (D3:0). Command codes are available to enable or disable all outputs, or individual outputs, as shown in Table 1. Each output has 4-bit Master and Slave Registers associated with it, that hold the output’s currently selected input address (defined by D3:0). The input address - if applicable - is loaded into the Master Register on the rising edge of WR. If the HA457 is in level mode, and if LATCH=0 (asynchronous switching), then the input address flows through the transparent Slave Register, and the output immediately switches to the new input. For synchronous switching on the rising edge of LATCH, strap the HA457 for edge mode, program all the desired switch connections, and then drive an inverted pulse on the LATCH input. Note: Operations defined by commands 1011 - 1111 occur asynchronously on the WR rising edge, without regard for the state of LATCH or EDGE/$\overline{\text{LEVEL}}$.

32-Bit Serial Mode

In the serial programming mode, all master registers are loaded with data, making it unnecessary to specify an output address (A2:0). The input data format is D3-D0, starting with OUT0 and ending with OUT7 for 32 total bits (i.e., first bit shifted in is D3 for OUT0, and 32nd bit shifted in is D0 for OUT7). Only codes 0000 through 1010 are valid serial mode commands. Code 1010 disables an individual output, while code 1001 enables it. After data is shifted into the 32-bit Master Register, it transfers to the Slave Register on the rising edge of the LATCH line (Edge mode), or when LATCH = 0 (Level mode, see Figure 10).

Figure 6 shows a typical application of the HA457 for driving 75Ω loads. This application shows the HA457 digital-switch control interface set up in the 7-bit parallel mode. The HA457 uses 7 data lines and 3 control lines (WR, $\overline{CE}$ and LATCH).

The input/output information is presented to the chip at A2:0 and D3:0 by a parallel printer port. The data is stored in the master registers on the rising edge of WR. When the LATCH line goes high, the switch configuration loads into the slave registers, and all 8 outputs reconfigure at the same time. Each 7-bit word updates only one output at a time. If several outputs are to be updated, the data is individually loaded into the master registers. Then, a single LATCH pulse can reconfigure all channels simultaneously.

An IBM compatible PC loads the programming data into the HA457 via its parallel port (LPT1) using a simple BASIC program.

TABLE 1. PARALLEL INTERFACE COMMANDS

A2:0	D3:0	ACTION
Selects Output Being Programmed	0000 to 0111	Connect the input defined by D3:0 to the output selected by A2:0. Doesn't enable a disabled output.
	1000	Connect the output selected by A2:0 to GND. Doesn't enable a disabled output.
	1011	Asynchronously disable the single output selected by A2:0, and leave the Master Register unchanged.
	1100	Asynchronously enable the single output selected by A2:0, and leave the Master Register unchanged.
Address Inputs are Irrelevant for These Functions	1101	Asynchronously disable all outputs, and leave the Master Register unchanged.
	1110	Asynchronously enable all outputs, and leave the Master Register unchanged.
	1111	Send a Software pulse to the Slave Register to load it from the Master Register, iff, the LATCH input=1. If the LATCH input=0, then this command is a NOP. The Master Register is unchanged by this command.
	1001 or 1010	Do not use these codes in the parallel programming mode. These codes are for serial programming only.

TABLE 2. SERIAL INTERFACE COMMANDS

D3:0	ACTION
0000 to 0111	Connect the output to the input channel defined by D3:0. Doesn't enable a disabled output.
1000	Connect the output to GND. Doesn't enable a disabled output.
1001	Enable the output and connect it to GND. The default power-up state is all outputs disabled, so use this code to enable outputs after power is applied, but before programming the switch configuration.
1010	Disable the output. The output is no longer associated with any input channel; the desired input must be redefined after reenabling the output.
1011 to 1111	Do not use these codes in the serial programming mode.

TABLE 3. DEFINITION OF DATA AND ADDRESS BIT FUNCTIONS

SER/$\overline{PAR}$	D3	D2	D1	D0	A2:0	COMMENT
H	X	X	Serial Data Output	Serial Data Input	X	32-Bit Serial Mode
L	H	Parallel Data Input	Parallel Data Input	Parallel Data Input	Output Address	Parallel Mode; D2:0 define the command to be executed.
L	L	Parallel Data Input	Parallel Data Input	Parallel Data Input	Output Address	Parallel Mode; D2:0 define the Input Channel

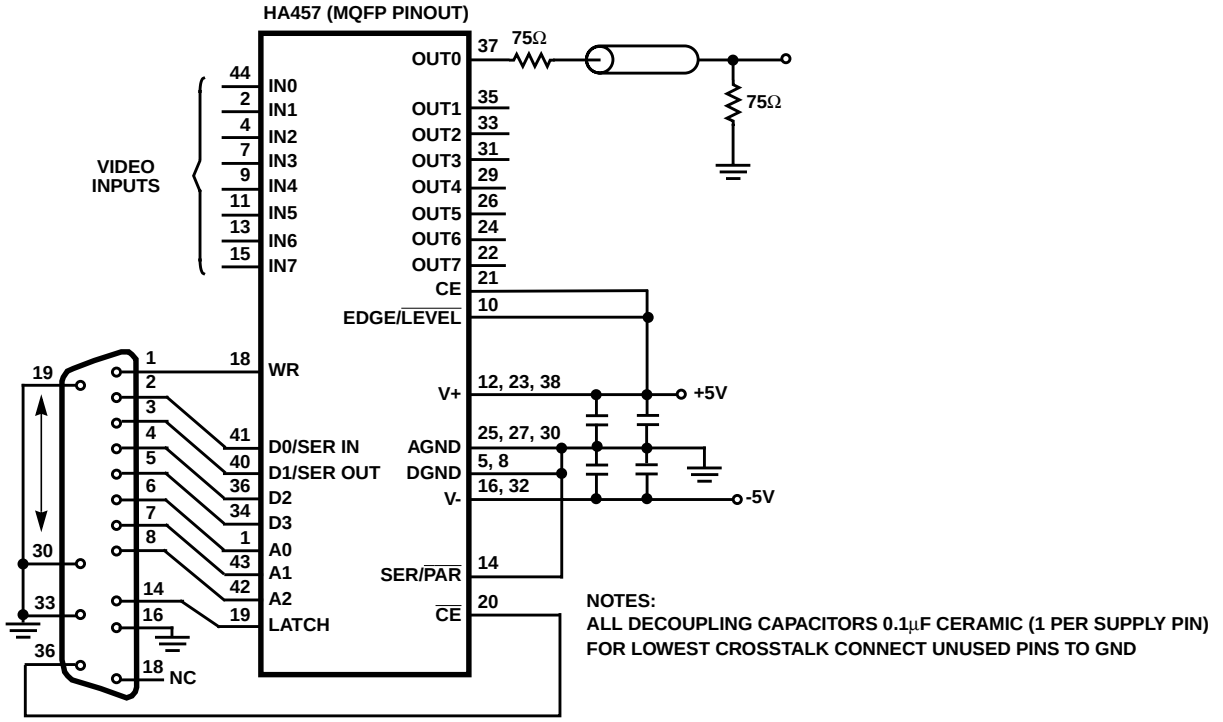


FIGURE 6. TYPICAL CABLE DRIVING, PARALLEL MODE APPLICATION CIRCUIT

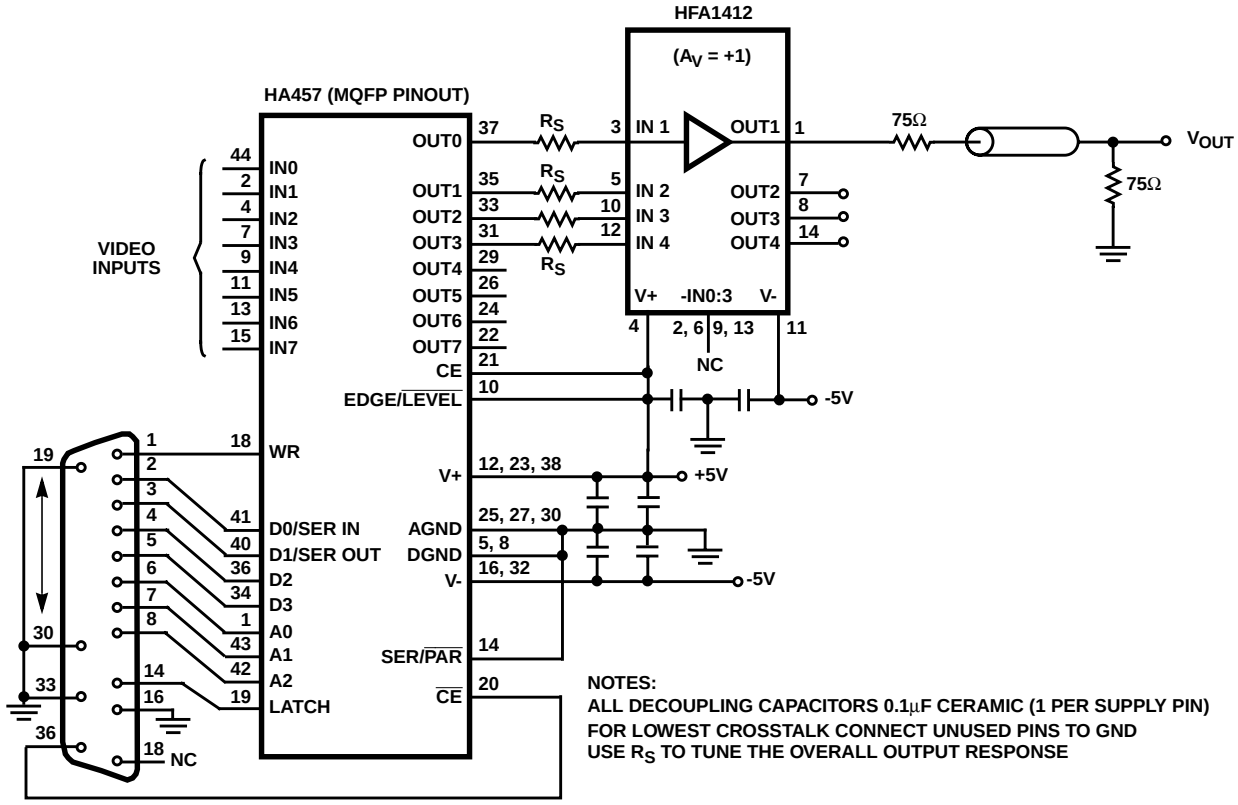


FIGURE 7. TYPICAL HIGH PERFORMANCE (IMPROVED DG, DP) APPLICATION CIRCUIT (SEE FIGURE 21)

Waveforms

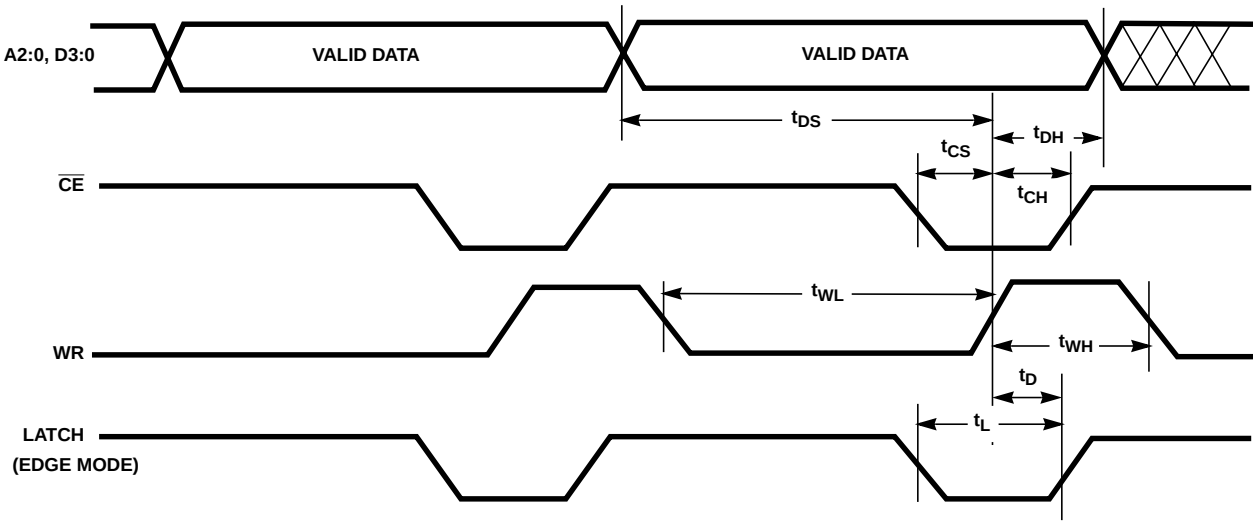


FIGURE 8. DIGITAL TIMING REQUIREMENTS

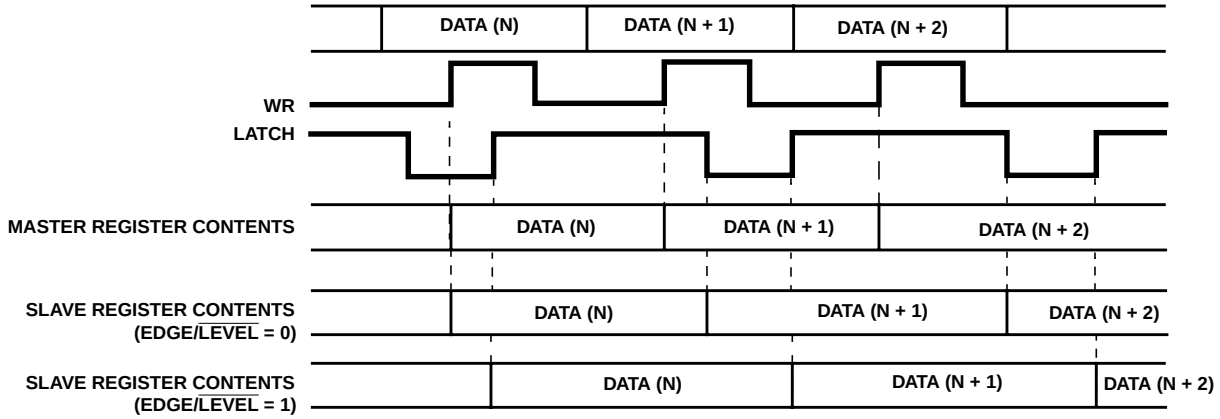


FIGURE 9. PARALLEL PROGRAMMING MODE OPERATION (SER/$\overline{PAR}$ = 0)

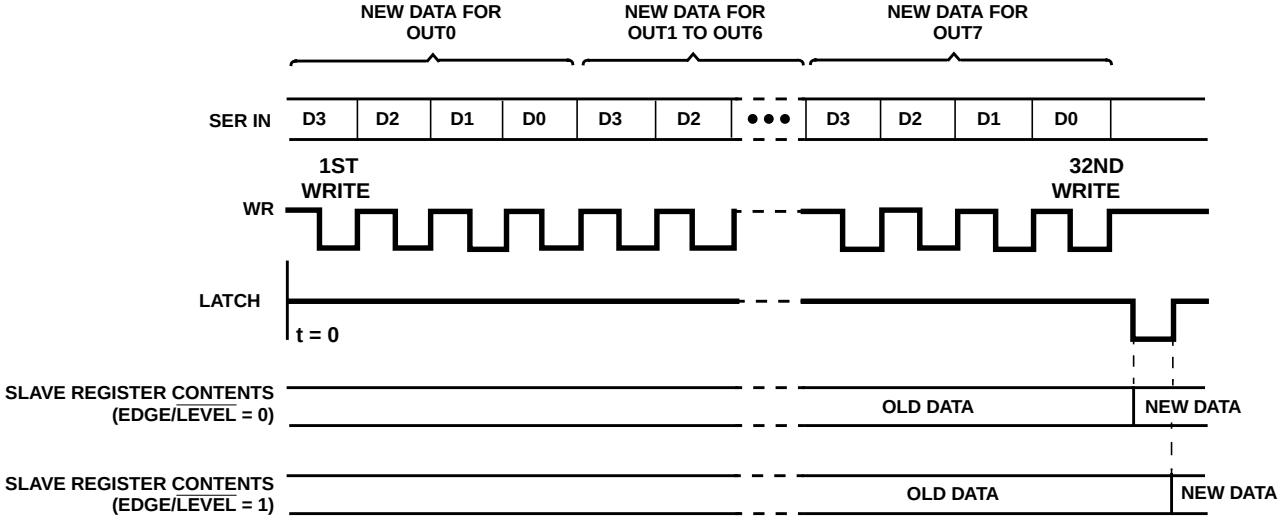


FIGURE 10. SERIAL PROGRAMMING MODE OPERATION (SER/$\overline{PAR}$ = 1)

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^oC$, $R_L = 150\Omega$, Unless Otherwise Specified

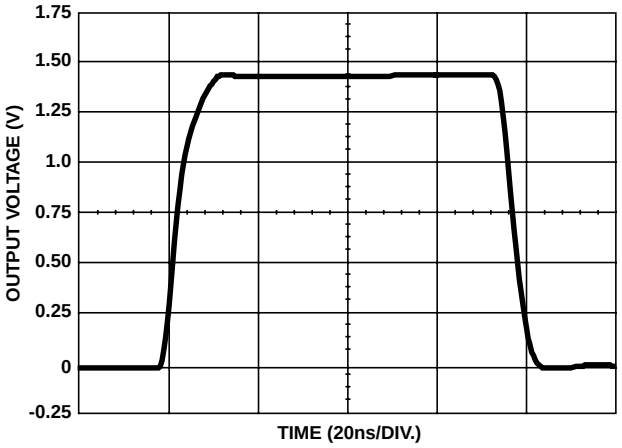


FIGURE 11. SMALL SIGNAL PULSE RESPONSE

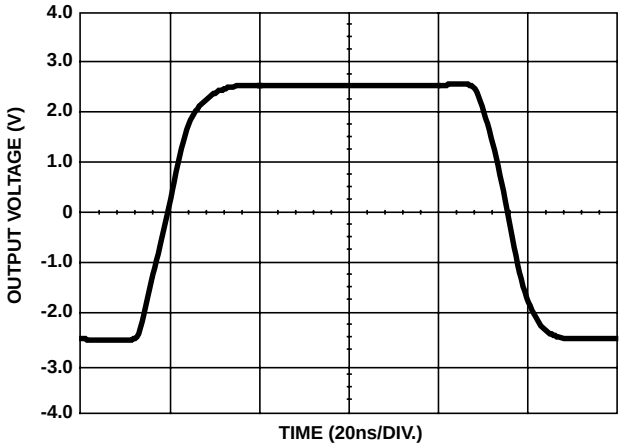


FIGURE 12. LARGE SIGNAL PULSE RESPONSE

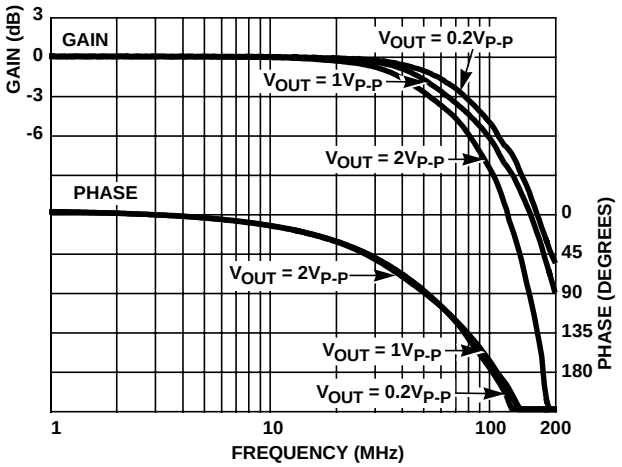


FIGURE 13. FREQUENCY RESPONSE

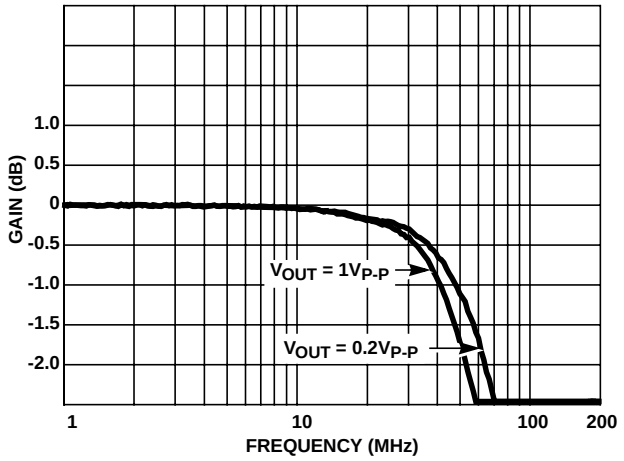


FIGURE 14. GAIN FLATNESS

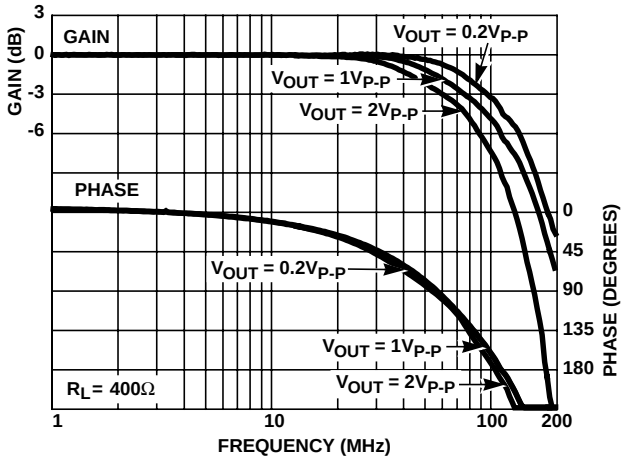


FIGURE 15. FREQUENCY RESPONSE

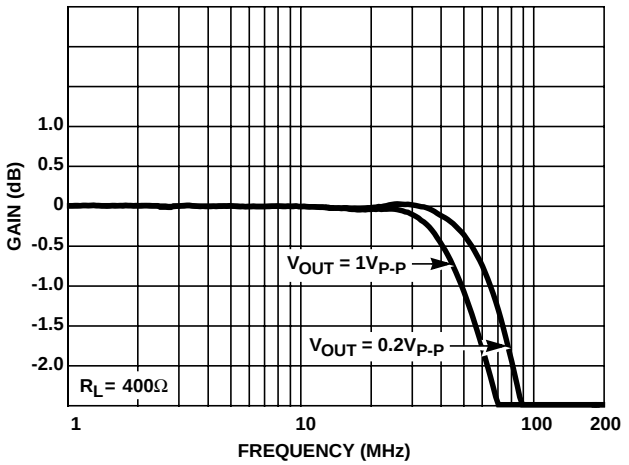


FIGURE 16. GAIN FLATNESS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = 25^0C$, $R_L = 150\Omega$, Unless Otherwise Specified **(Continued)**

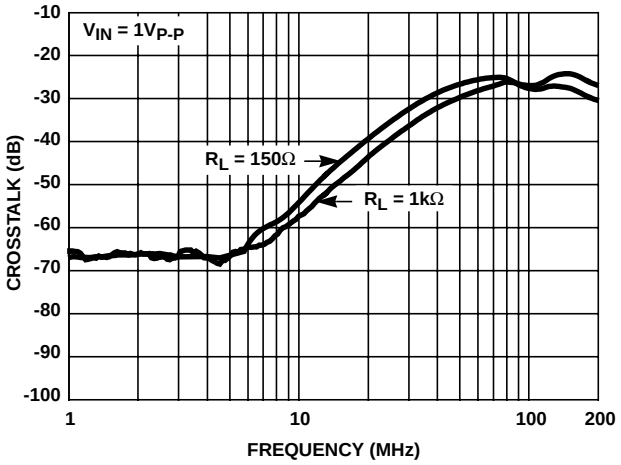


FIGURE 17. ALL HOSTILE CROSSTALK

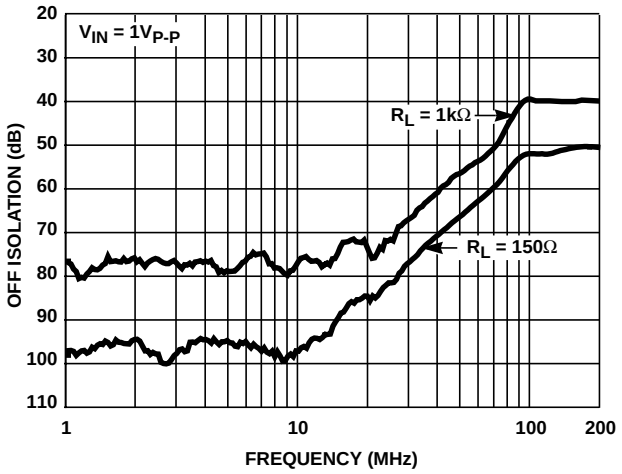


FIGURE 18. ALL HOSTILE OFF-ISOLATION

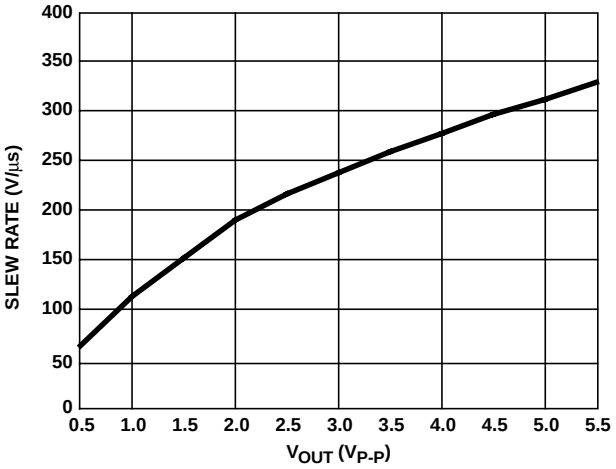


FIGURE 19. SLEW RATE vs V_{OUT}

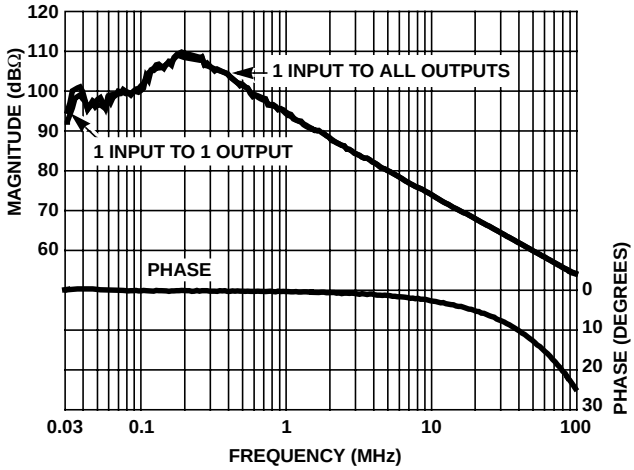


FIGURE 20. INPUT IMPEDANCE vs FREQUENCY

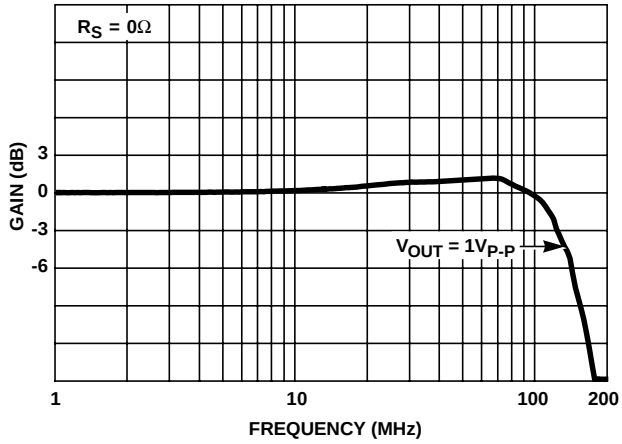
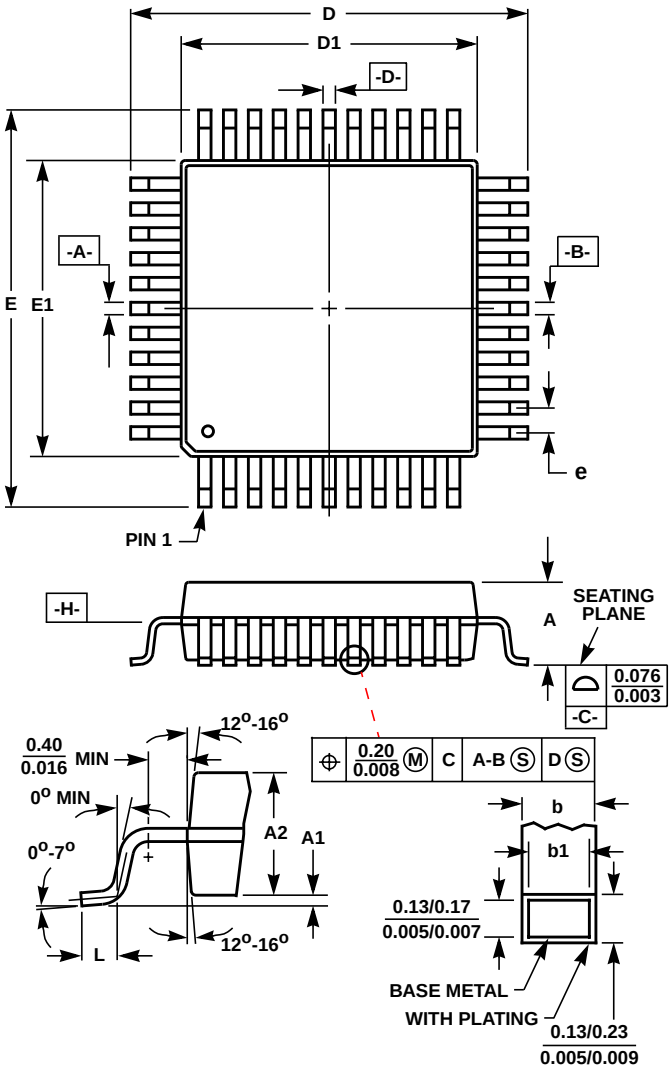


FIGURE 21. FREQUENCY RESPONSE OF HA457-HFA1412 ($A_V = 1$) COMBINATION (PER FIGURE 7)

Metric Plastic Quad Flatpack Packages (MQFP)



Q44.10x10 (JEDEC MS-022AB ISSUE B)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

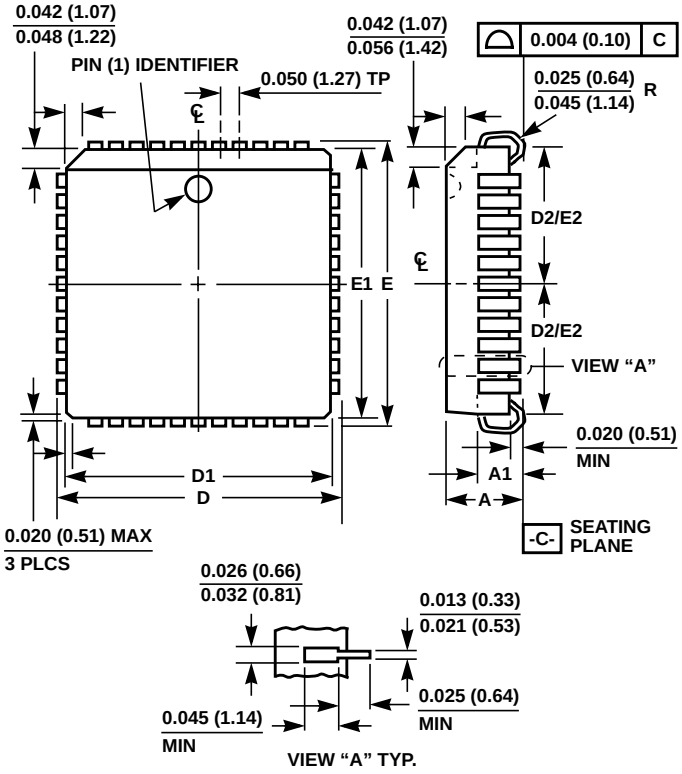
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.096	-	2.45	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.515	0.524	13.08	13.32	3
D1	0.389	0.399	9.88	10.12	4, 5
E	0.516	0.523	13.10	13.30	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 2 4/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N44.65 **(JEDEC MS-018AC ISSUE A)**
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

Rev. 2 11/97

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

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