DATA SHEET

SA9504

Dual-band, PCS(CDMA)/AMPS
LNA and downconverter mixers

Preliminary specification
Supersedes data of 1999 Aug 24

1999 Oct 28

Philips
Semiconductors

PHILIPS

Dual-band, PCS(CDMA)/AMPS LNA and downconverter mixers

SA9504

DESCRIPTION

The SA9504 is an integrated receiver front-end for 900 MHz Cellular (AMPS) and 1.9 GHz PCS (CDMA) phones. This dual-band receiver circuit has low noise amplifiers and downconverters for both bands, and provides an elegant solution for RF-to-IF conversion.

The two cascode LNAs have been designed to provide high gain with very low noise figures and high linearity. The downconverter portion is based on the Philips SA9502. There are two individual mixer blocks, each optimized for low noise figure and high linearity. The whole circuit is designed for low power consumption, high performance, and is compatible with the requirements for Cellular (AMPS) and PCS (CDMA) handsets.

The circuit has been designed in our advanced QUBiC3 BiCMOS process with 30 GHz f_T and 60 GHz f_{MAX}.

FEATURES

LNA typical performance

PARAMETER	Cellular LNA	PCS (CDMA) LNA
Gain (dB)	16.5	14.8
Noise figure (dB)	1.6	2
Input IP3 (dBm)	–2	1
Current (mA)	4.9	4.9

- LNAs for both Cellular (AMPS) and PCS (CDMA) bands
- High gain, low noise figure, high linearity performance
- Cascode output structure requiring no external matching
- Low power consumption, typical 4.9 mA
- Low voltage operation down to 2.7 volts

Downconverter typical performance

PARAMETER	Cellular FM	PCS (CDMA)
Gain (dB)	7.5	11.5
Noise Figure (dB)	10	9
Input IP3 (dBm)	5	4
Current (mA) (Tx) LO output buffer off	6.9	17

- Separate, selectable IF outputs to suit FM and CDMA bandwidths
- Buffered Cellular and PCS LO inputs
- Integrated frequency doubler for PCS mixer LO
- Differential (Tx) LO output buffer (can be switched on or off)
- Low voltage operation down to 2.7 volts
- Mixers current consumption with (Tx) LO buffer on:
  - Cellular FM: 17.4 mA
  - PCS: 27.6 mA
- Low standby current in sleep mode: <50 μA
- Small LQFP32 package

APPLICATIONS

- 800 MHz analog FM and receivers
- 1.9 GHz PCS (CDMA) digital receivers
- Supports dual-band operation
- Digital mobile communications equipment
- Portable, low power radio equipment

BLOCK DIAGRAM

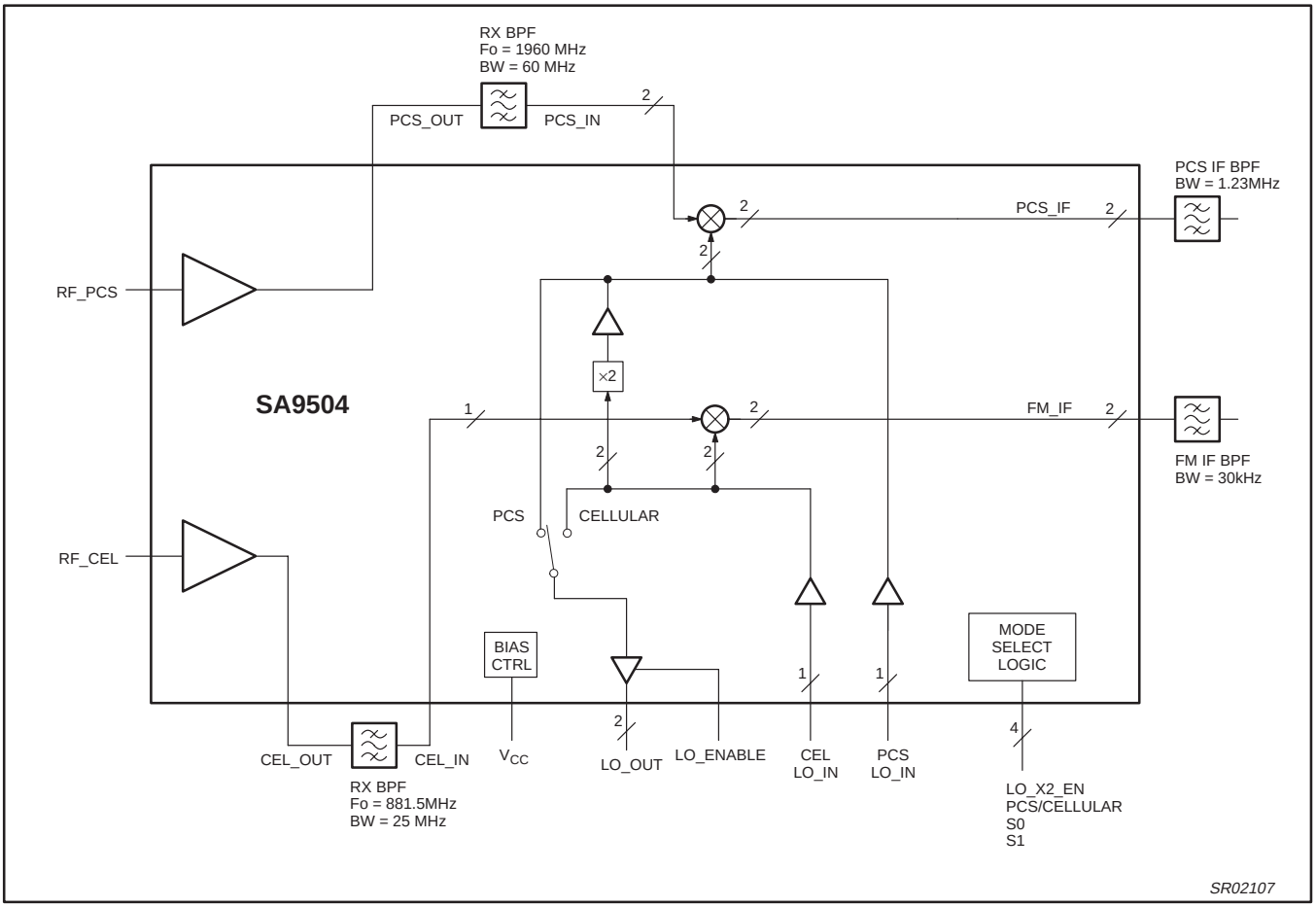


Figure 1. SA9504 Block Diagram

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATINGS	UNIT
Supply voltage (V_{CC})	–0.3 to +3.6	V
Logic input voltage	–0.3 to V_{CC}+0.3	V
Maximum power input	+20	dBm
Power dissipation (T_{amb} = 25°C)	800	mW
Storage temperature range	–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated-conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Supply voltage (V_{CC})		2.7	2.85	3.3	V
Operating ambient temperature range (T_{amb})		–40		+85	°C

FUNCTIONAL DESCRIPTION

Mode selection

The SA9504 has several modes of operation for which the selection logic is defined in Table 1. Different mode selections require different portions of the circuit to be active. Modes from unlisted combinations of logic pins are not permitted. The LNA and downconverter together can be programmed to operate in the PCS or cellular bands using the PCS/CEL logic input pin.

In order for the SA9504 to function correctly, a reset must be applied on first power-up. The whole circuit (LNAs and mixers) is powered down when control lines S0 and S1 are simultaneously held HIGH. An internal reset is applied upon releasing the circuit from power-down (on taking S0 = S1 from HIGH to LOW).

LNA

The SA9504 has two LNAs, one for cellular FM, and one for PCS (CDMA). The LNAs have been designed for high gain, low noise figure and good linearity with low power consumption. External components can be used to match the LNA inputs for the Cellular and PCS bands. The LNAs employ a cascode output structure allowing high gain and excellent reverse isolation. The LNA outputs are internally matched to drive 50Ω external loads. The input and output return loss of better than 10 dB can be achieved in all modes.

Downconverter

The SA9504 has two mixers, one for Cellular FM, and one for PCS (CDMA). Each mixer is individually optimized for its specific requirements. The Cellular FM mixer has a common single-ended RF input. The PCS mixer's RF input port is differential, and requires an external balun when used with a single-ended source. Both the PCS and the Cellular mixer RF inputs should be AC coupled.

Local oscillator drive for the mixers is provided through pins CEL LO_IN and/or PCS LO_IN. The local oscillator inputs are single-ended, AC-coupled. The CEL LO_IN signal is internally buffered to drive the following:

– (Tx) LO output buffer,

– cellular FM mixer,

– PCS LO frequency doubler.

In the PCS mode, mixer LO drive can be either direct (PCS LO_IN) or through the frequency doubler after CEL LO_IN. The mixer local oscillator signal is made available externally via the (Tx) LO output buffer for potential use elsewhere in the radio. For example, this signal typically can be used with the transmitter circuitry. The (Tx) LO output buffer can be powered down independently, using the (Tx) LO_ENABLE logic input. The (Tx) LO output buffer has open collector differential outputs which should be externally biased to power supply rail.

The PCS and Cellular FM mixers have open collector differential IF outputs. The differential IF outputs must be biased at the supply voltage through external inductors that may also be part of the matching circuit to the SAW filter.

MODE SELECT LOGIC AND DC CHARACTERISTICS

The SA9504 chip has several modes of operation for which the selection logic is defined in the following table. Different mode selections require different portions of the circuit to be active. Modes from unlisted combinations of logic pins, are not valid.

POWER-UP PROCEDURE

In order for the SA9504 to function correctly as given in Table 1, the circuit must be reset on power-up as follows:

To apply a reset, both S0 and S1 should be held HIGH simultaneously (hold time 100 ns minimum), and then released to a LOW state upon initially powering up the device.

Table 1. Mode logic definition for LNA and Downconverter mixers

	MODES	(Tx) LO BUFFER	(Tx) LO BUFFER OUTPUT	LO FREQ. DOUBLER	LOGIC INPUT PINS			
					POWER DOWN[1] S0 = S1	PCS/CEL	LO X2 ENABLE	(Tx) LO ENABLE
PCS (CDMA)								
1	PCS1	On	2 GHz	Off	0	1	0	1
2	PCS1 Idle	Off	—	Off	0	1	0	0
3	PCS2	On	2 GHz	On	0	1	1	1
4	PCS2 Idle	Off	—	On	0	1	1	0
Cellular FM								
5	FM	On	1 GHz	Off	0	0	0	1
6	FM Idle	Off	—	Off	0	0	0	0
Power Down								
7	Sleep[1]	x	x	Off	1	x	x	x

NOTES:
x = Don't care
1. The device will be in the Power Down mode (sleep) when both control lines S0 and S1 are held HIGH simultaneously.

DC CHARACTERISTICS

V_{CC} = 3.3 V; T_{amb} = +25 °C

SYMBOL	PARAMETER		CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
Power supply							
V_{CC}	Supply voltage	all modes		2.7	2.85	3.3	V
I_{CC}	Supply current	PCS1 mode			32.5	37.4	mA
		PCS1 Idle mode			21.9	25.2	mA
		PCS2 mode			36.9	42.4	mA
		PCS2 Idle mode			26.3	30.2	mA
		FM mode			22.3	25.6	mA
		FM Idle mode			11.8	13.8	mA
$I_{CC(PD)}$	Supply current in power down	Sleep			1	50	µA
Logic inputs (LO_ENABLE, PCS/CEL, S0, S1, LO_X2_EN pins)							
V_{IH}	HIGH level input voltage range		At logic 1	$0.5V_{CC}$		V_{CC}+0.3	V
V_{IL}	LOW level input voltage range		At logic 0	–0.3		$0.2V_{CC}$	V
I_{IH}	HIGH level input bias current		pins at V_{CC} – 0.4 V	–5	0	5	µA
I_{IL}	LOW level input bias current		pins at 0.4 V	–5	0	5	µA

LNA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7 V; T_{amb} = 25°C

PARAMETER	TEST CONDITIONS	LIMITS					UNIT
		MIN	–3σ	TYP	+3σ	MAX	
Cellular band LNA							
RF input frequency range		869				894	MHz
Gain			15.5	16.5	17.5		dB
Noise Figure				1.6	1.9		dB
Input IP3	2 tones of –30 dBm each, Δf=60 kHz		–7	–6			dBm
	2 tones of –30 dBm each, Δf=800 kHz		–3	–1.5			dBm
S11	With external matching			–10			dB
S22				–15			dB
S12				–40			dB
LO (input and output) to LNA input isolation All modes	LO single-ended in, single-ended out, with and without doubler. 0 dBm LO in, (Tx) LO buffer ON.			40			dB
PCS band LNA							
RF input frequency range		1810				1990	MHz
Gain			13.8	14.8	16		dB
Noise Figure				2.0	2.4		dB
Input IP3	2 tones of –30 dBm each, Δf=800 kHz		0	1.5			dBm
S11	With external matching			–9			dB
S22				–12			dB
S12				–40			dB
LO (input and Output) to LNA input isolation	LO single-ended in, single-ended out, with and without doubler. 0 dBm LO in, (Tx) LO buffer ON.			36			dB

TYPICAL LNA SPECIFICATIONS WITH TEMPERATURE VARIATION AT –40°C AND +85°C

V_{CC} = 2.7 V

SPECIFICATION	CONDITIONS	TEMPERATURE			UNIT
		–40°C	+25°C	+85°C	
Cellular band LNA					
Supply current variation		–100	0	–100	μA
Gain variation		1	0	–1	dB
Noise Figure variation		–0.3	0	0.3	dB
Input IP3 variation	Δf = 60 kHz	–0.35	0	0.3	dBm
PCS band LNA					
Supply current variation		–40	0	–40	μA
Gain variation		0.8	0	–1	dB
Noise Figure variation		–0.4	0	0.4	dB
Input IP3 variation		0.9	0	–1	dBm

DOWNCONVERTER

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7 V; T_{amb} = 25°C, P_{lo}= –3 dBm.
f_{RF} = 881 MHz, f_{LO} = 966.4 MHz, f_{IF} = 85.4 MHz, output differential load of 850Ω for FM.

PARAMETER	TEST CONDITIONS	LIMITS					UNIT
		MIN	–3σ	TYP	+3σ	MAX	
Cellular band downconverter							
RF input frequency range		869				894	MHz
LO input frequency range		950				1030	MHz
IF output frequency range		50				300	MHz
IF Output Load Impedance	Single-ended, with external balun			850			Ω
Conversion Gain			6.5	7.5	8.2		dB
Noise Figure	Single sideband Noise Figure			10	11		dB
Input IP3	P1, P2 = –24 dBm. Tone spacing = 60 kHz		5.0				dBm
RF Input Return Loss	Z_S=50Ω with external matching			11.0			dB
LO Input Return Loss	Z_S=50Ω			10.0			dB
(Tx) LO Output Return Loss	Z_S=50Ω			8.0			dB
LO Input Power Range			–9	–6	0		dBm
(Tx) LO Output Power Range	Z_L=50Ω single-ended; (Tx) LO buffer ON.		–6	–3	0		dBm
LO (Input and Output) to RF Leakage	Single-ended in, single-ended out.				–30		dBm
LO (Input and Output) to IF Leakage	Single-ended in, differential out.				–20		dBm
RF to LO (Input) Isolation	Single-ended in, single-ended out		30				dB
RF to IF Isolation	Single-ended in, differential out		10				dB
(Tx) LO Output to LO Input Isolation	Single-ended in, differential out		30				dB
Leakage conversion gain	f1 = $f_{RX} \pm 40$ MHz at LNA input. P1 = – 70 dBm. Measured through conversion gain in stop-band, without SAW filters being connected. Ports terminated with 50Ω.			–40			dBc

AC ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 2.7 V; T_{amb} = 25°C, P_{lo}= –3 dBm.
f_{RF} = 1960 MHz, f_{LO} = 1750 MHz, f_{IF} = 210 MHz, output differential load of 1 kΩ for PCS.

PARAMETER	TEST CONDITIONS	LIMITS					UNIT
		MIN	–3σ	TYP	+3σ	MAX	
PCS Downconverter							
RF input frequency range		1810				1990	MHz
LO input frequency range	without doubler	1720				2120	MHz
	with doubler	860				1050	MHz
IF output frequency range		50				300	MHz
IF Output Load Impedance	Differential			1000			Ω
Conversion Gain			10.5	11.5	12.5		dB
Noise Figure	SSB NF, low side LO (f_{LO} = 1750 MHz)			9.0	10		dB
	SSB NF, high side LO (f_{LO} = 2170 MHz)			8.0	9		dB
Input IP3	P1, P2 = –30 dBm Tone spacing = 800 kHz		3	4			dBm
RF Input Return Loss	Z_S = 50Ω, with external matching			10			dB
LO Input Return Loss	Z_S = 50Ω			10			dB
(Tx) LO Output Return Loss	Z_S = 50Ω			8			dB
LO Input Power Range			–9	–6	0		dBm
(Tx) LO Output Power Range	Z_L = 50Ω single-ended; (Tx) LO buffer ON		–10	–9	–6		dBm
LO (input and Output) to RF Leakage	Single-ended in, single-ended out, with and without doubler				–35		dBm
LO (input and Output) to IF Leakage	Single-ended in, differential out, with and without doubler				–35		dBm
RF to LO (Input) Isolation	Single-ended in, single-ended out, with and without doubler		30				dB
RF to IF Isolation	Single-ended in, differential out		20				dB
(Tx) LO Output to LO Input Isolation	Single-ended in, differential out, with doubler		30				dB
Leakage conversion gain	f1 = f_{RX} ± 80 MHz at LNA input. P1 = – 70 dBm. Measured through conversion gain in stop-band, without SAW filters being connected. Ports terminated with 50Ω.			–40			dBc

TYPICAL DOWNCONVERTER SPECIFICATIONS WITH TEMPERATURE VARIATION FROM –40°C TO +85°C

V_{CC} = 2.7 V

SPECIFICATION	TEMPERATURE			UNIT
	–40°C	+25°C	+85°C	
Cellular band downconverter				
Conversion Gain Variation	1	0	–1	dB
IP3 Variation	–4	0	+1	dB
Noise Figure Variation	–1.5	0	1.5	dB
PCS band downconverter				
Conversion Gain Variation	1	0	–1	dB
IP3 Variation	0.5	0	–1	dB
Noise Figure Variation	–1.5	0	0.8	dB

TYPICAL PERFORMANCE CHARACTERISTICS

DC current consumption

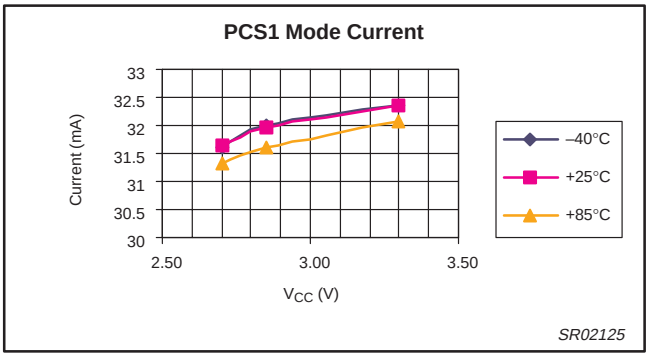


Figure 2. PCS1 Mode Current

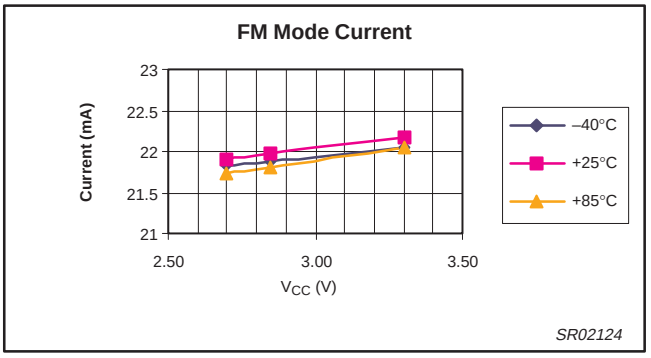


Figure 6. FM Mode Current

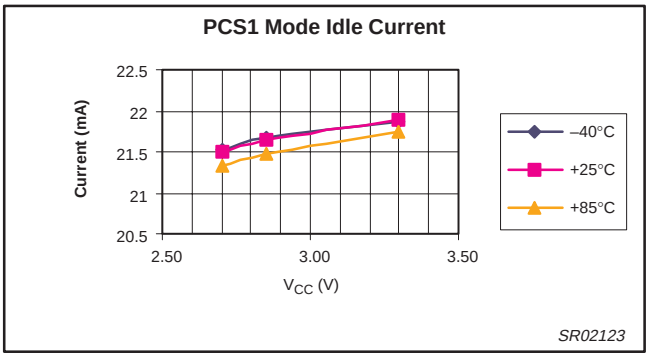


Figure 3. PCS1 Mode Idle Current

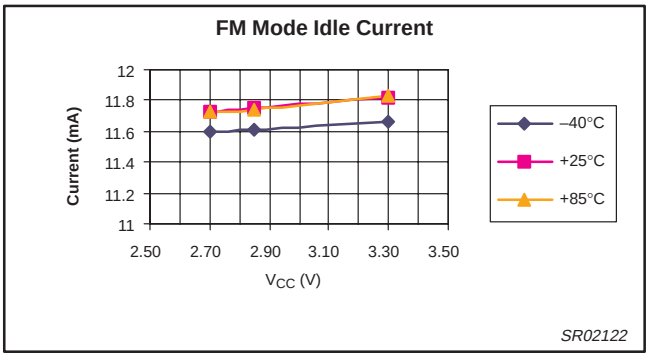


Figure 7. FM Mode Idle Current

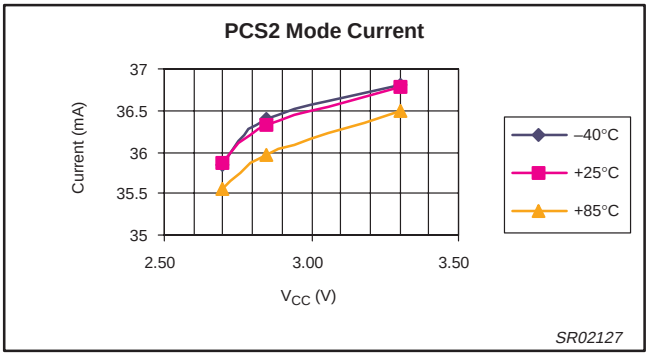


Figure 4. PCS2 Mode Current

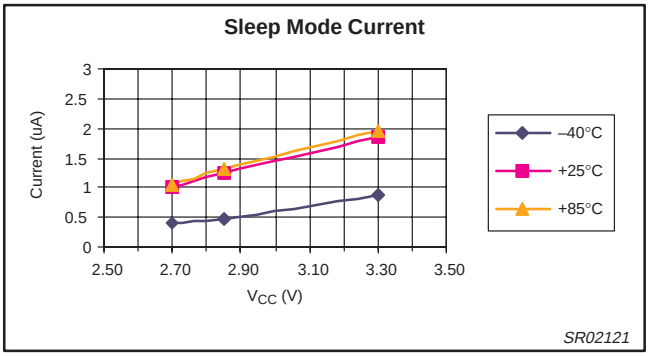


Figure 8. Sleep Mode Current

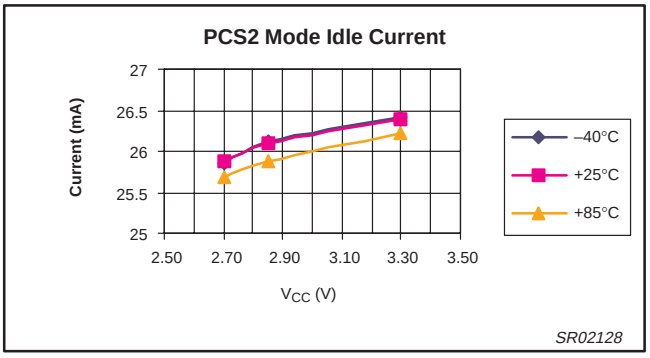


Figure 5. PCS2 Mode Idle Current

LNA characteristics

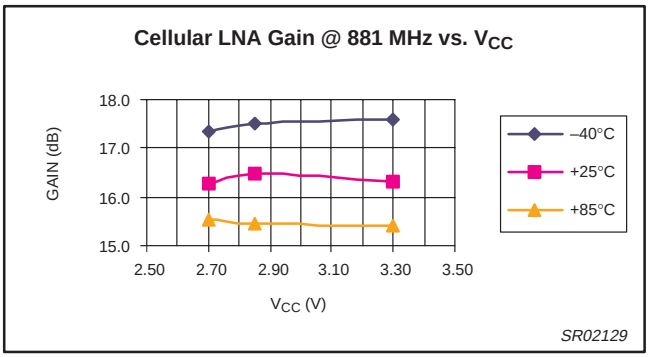


Figure 9.

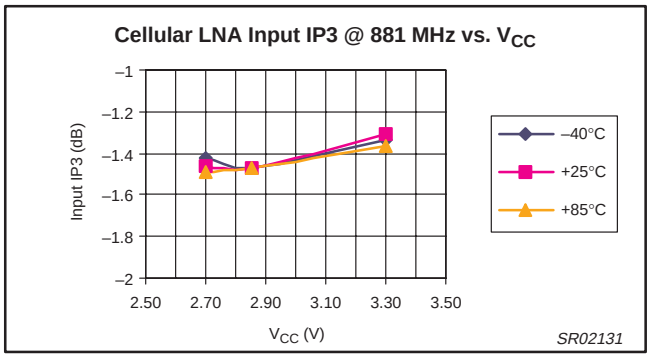


Figure 12.

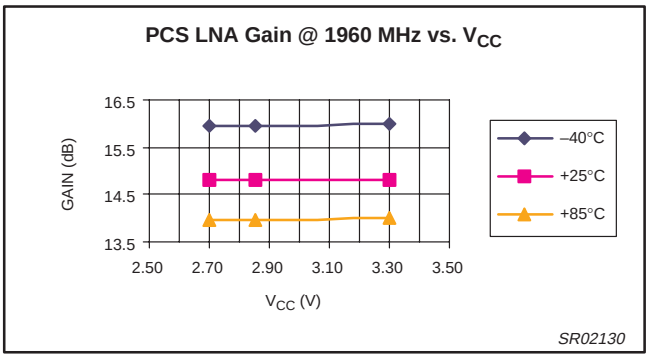


Figure 10.

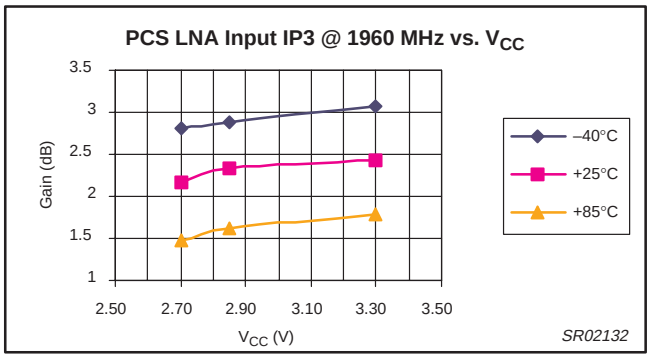


Figure 13.

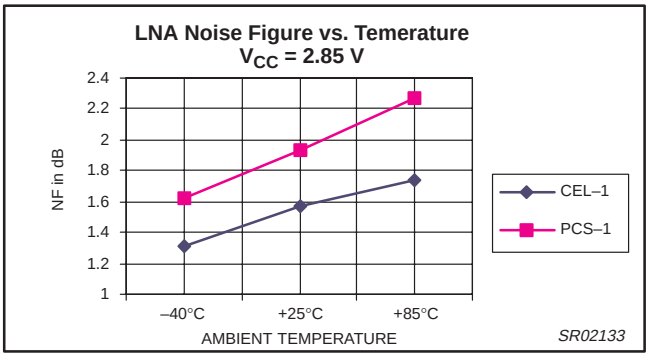


Figure 11.

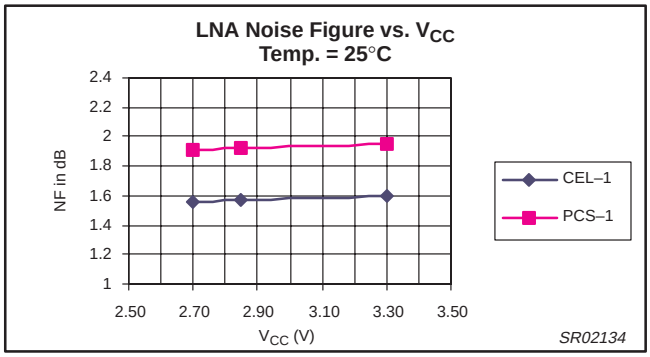


Figure 14.

Cellular Band Downconverter – Conversion Gain

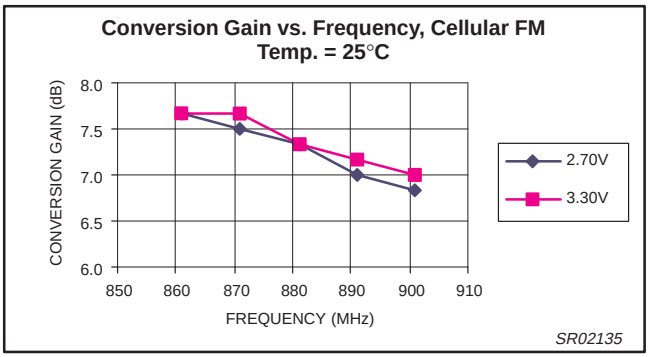
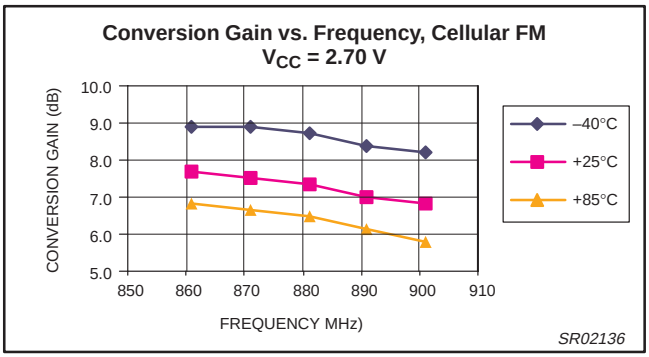


Figure 15.



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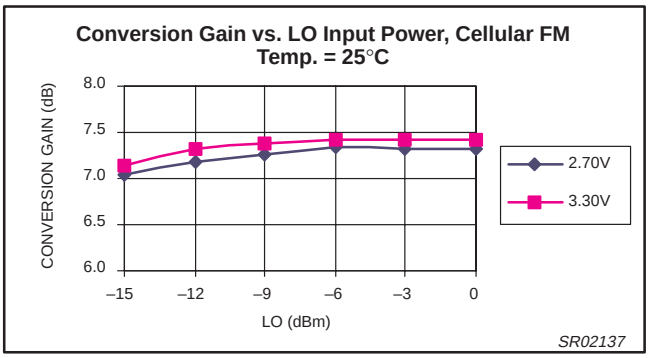
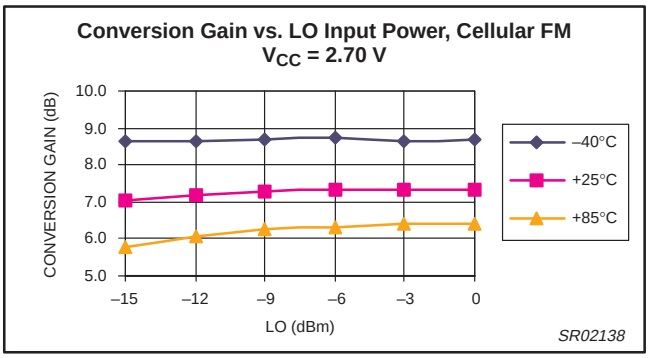


Figure 16.



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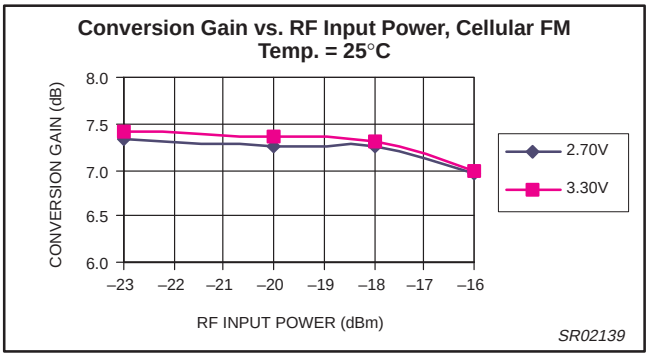


Figure 17.

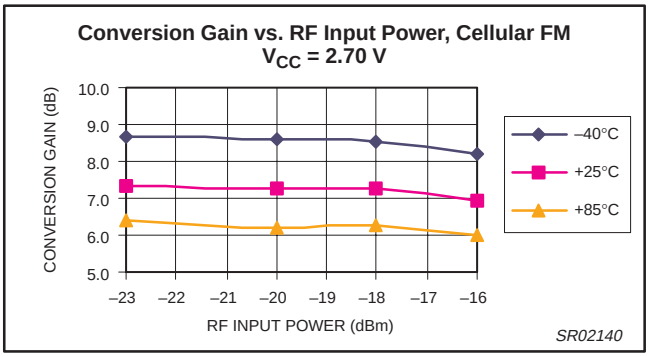


Figure 20.

PCS Downconverter (Direct LO) – Conversion Gain

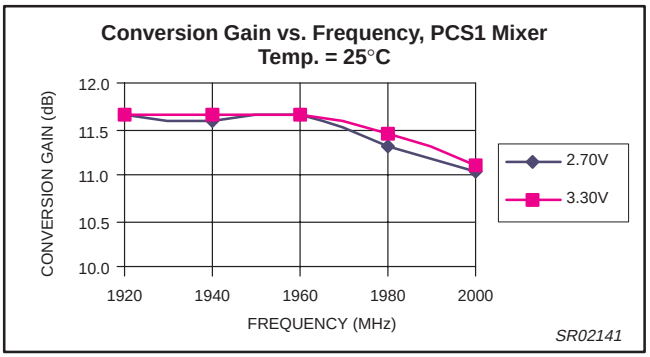


Figure 21.

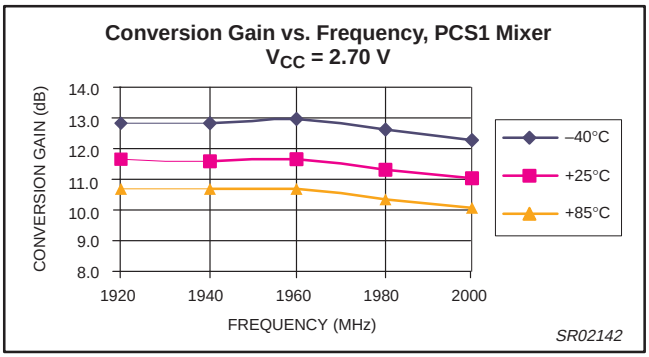


Figure 24.

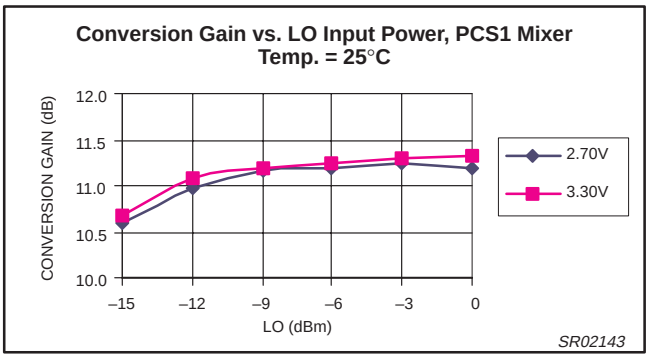


Figure 22.

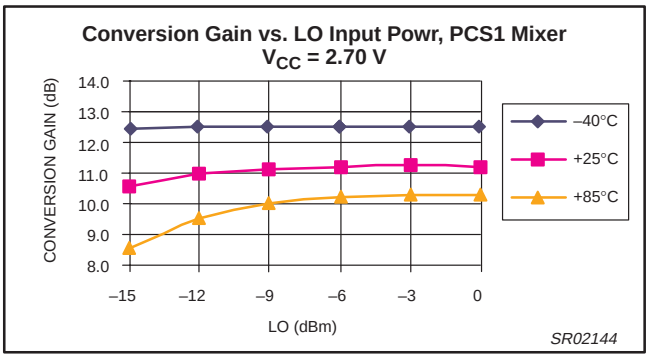


Figure 25.

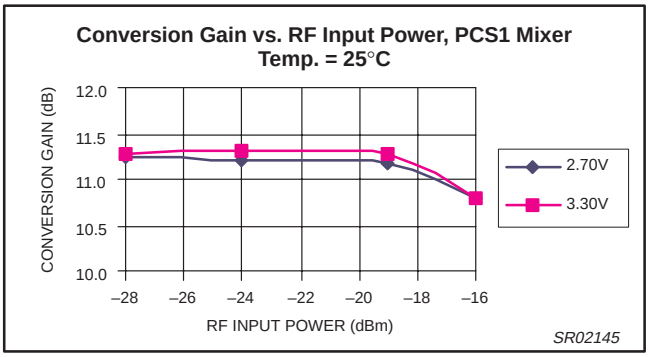


Figure 23.

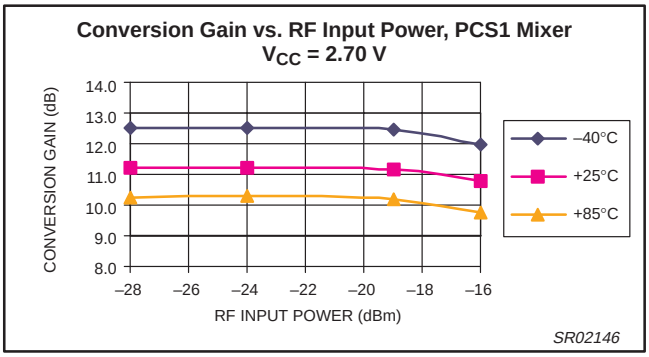


Figure 26.

PCS Downconverter (LO Doubler) – Conversion Gain

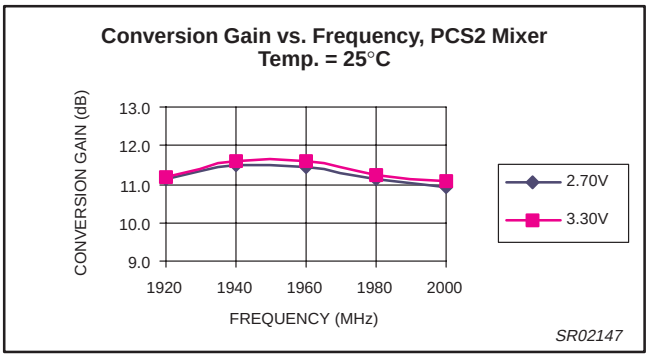
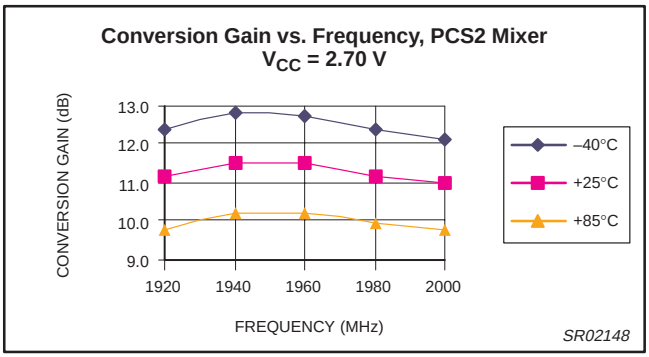


Figure 27.



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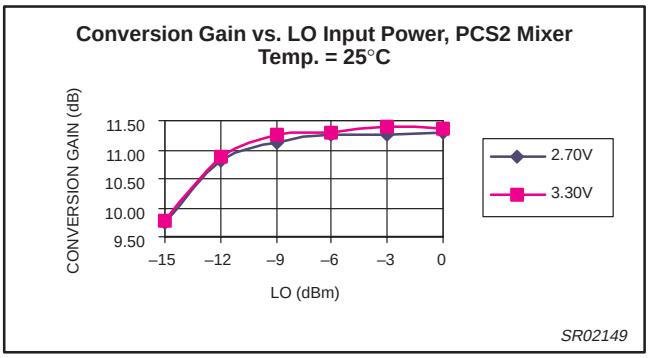
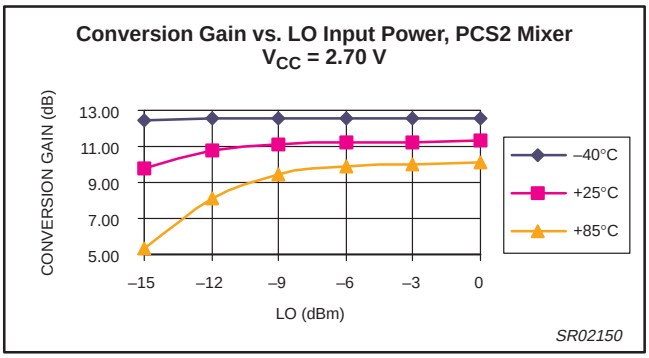


Figure 28.



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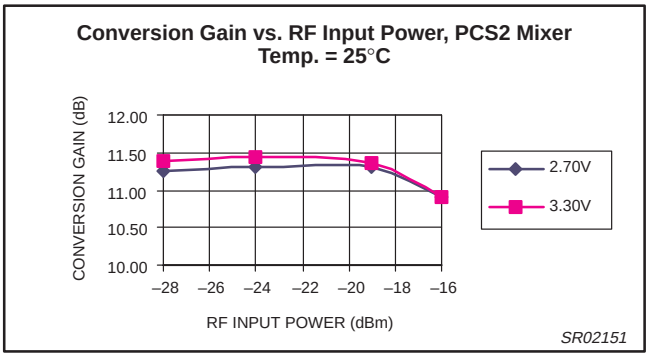


Figure 29.

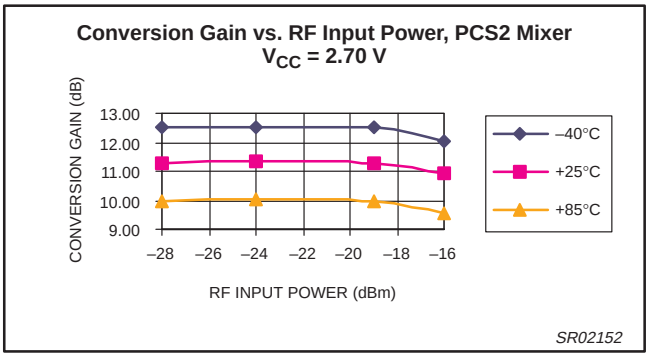


Figure 32.

Cellular Band Downconverter – Input IP3

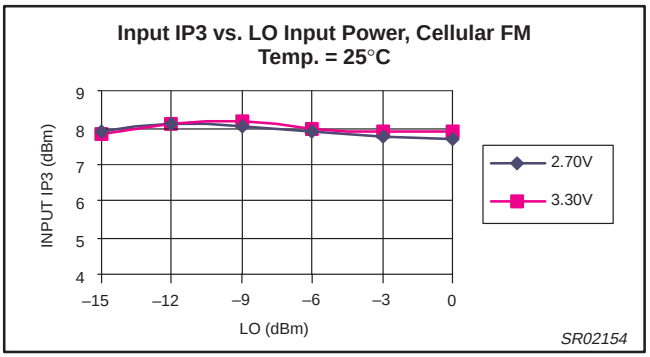


Figure 33.

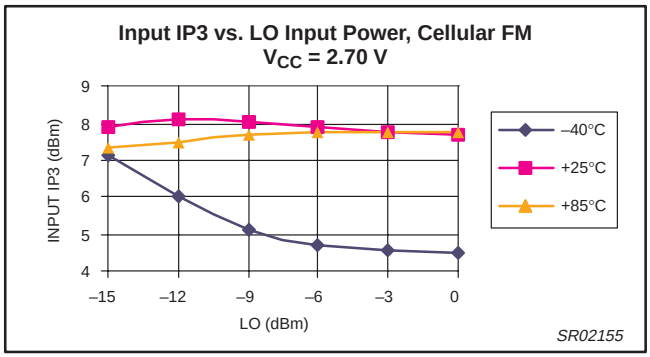
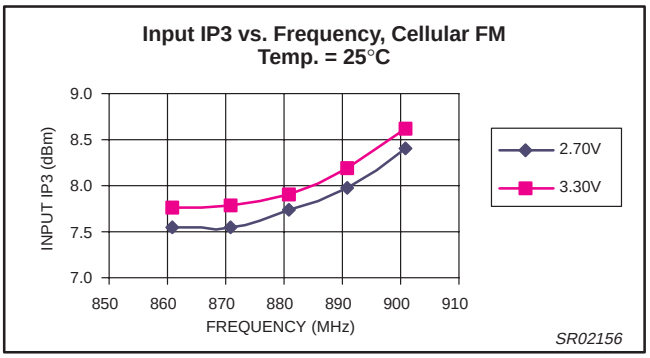


Figure 36.



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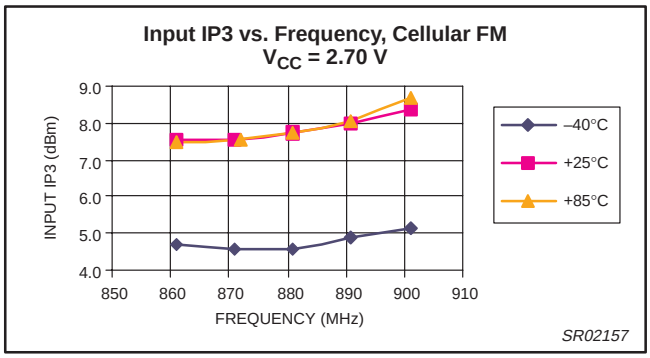

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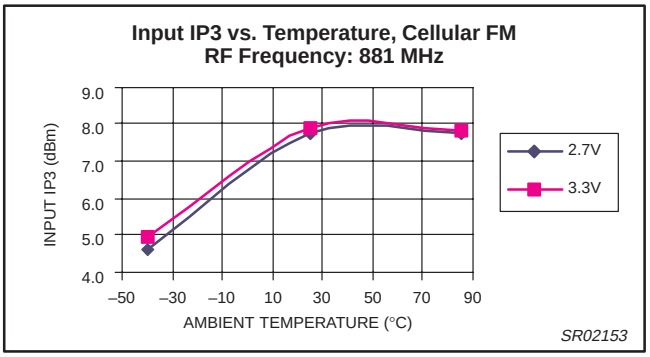


Figure 35.

PCS Downconverter (Direct LO) – Input IP3

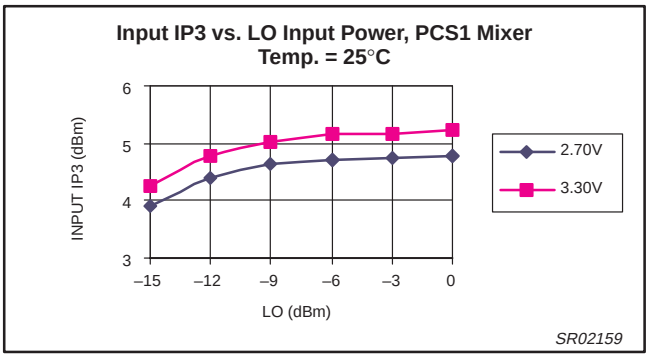


Figure 38.

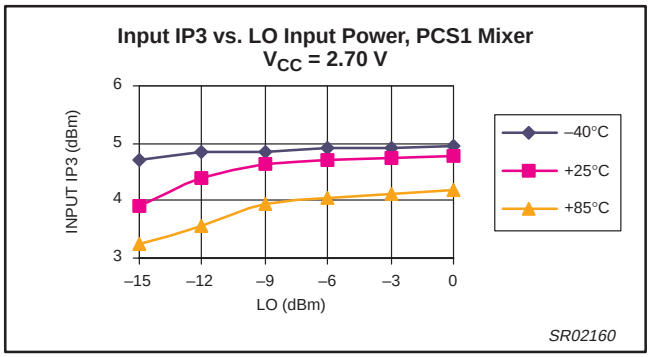


Figure 41.

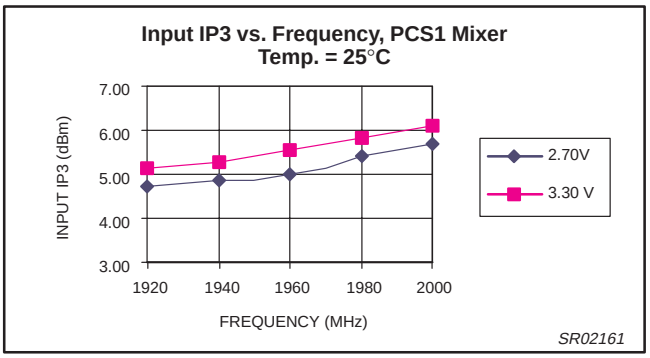


Figure 39.

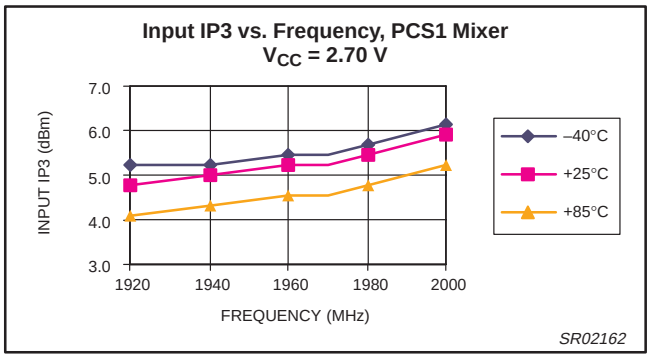


Figure 42.

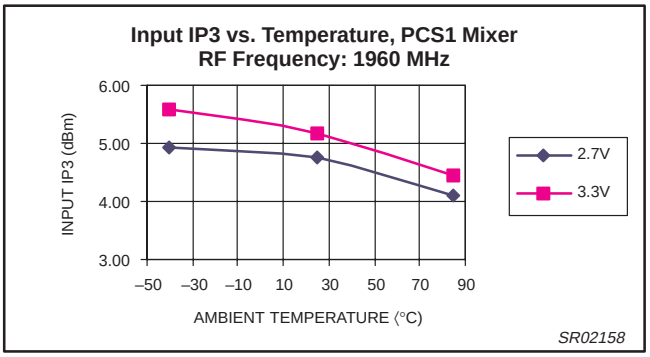


Figure 40.

PCS Downconverter (LO Doubler) – Input IP3

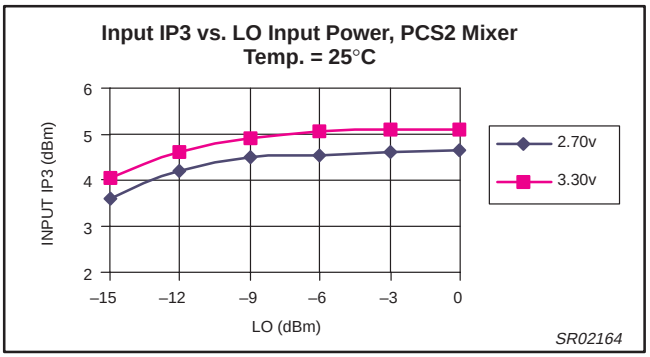


Figure 43.

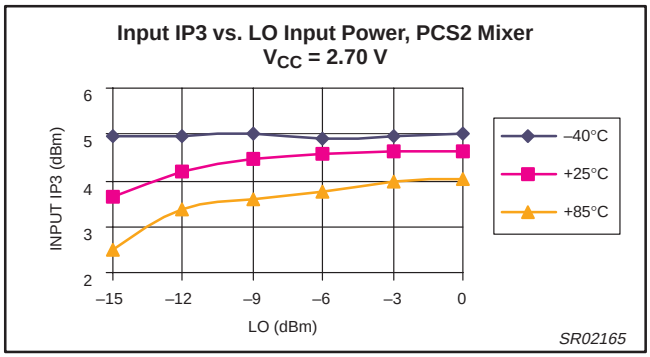


Figure 46.

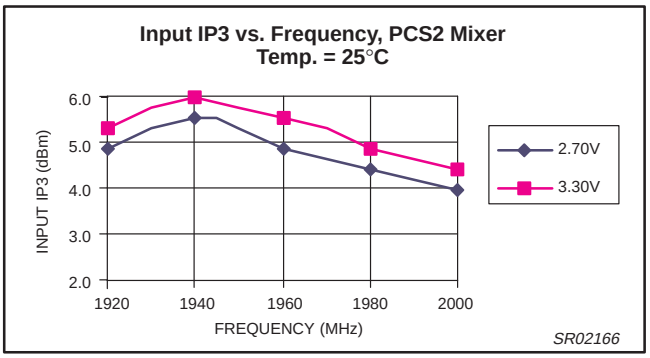


Figure 44.

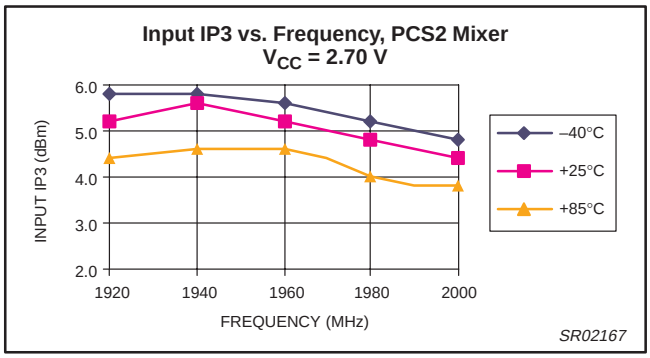


Figure 47.

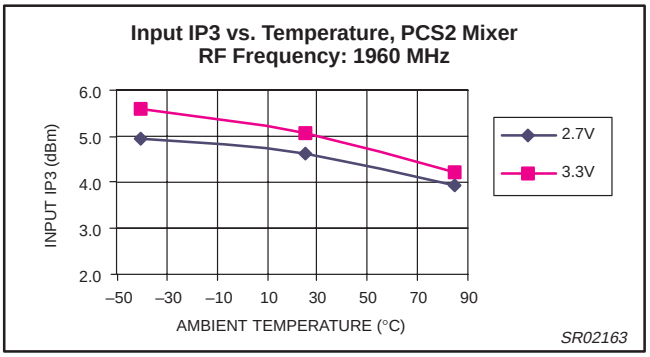


Figure 45.

Downconverter Mixers Noise Figure

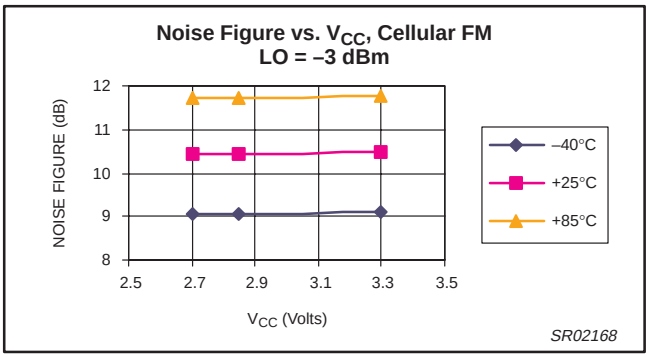


Figure 48.

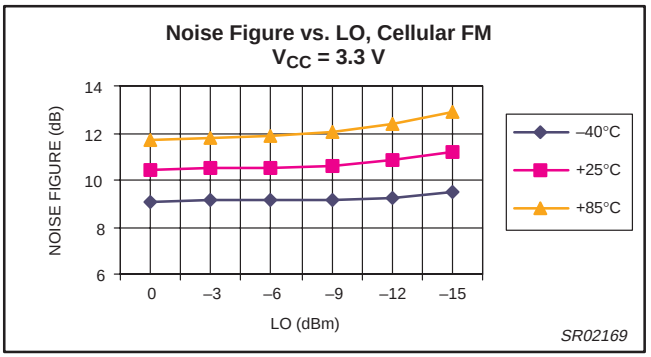


Figure 51.

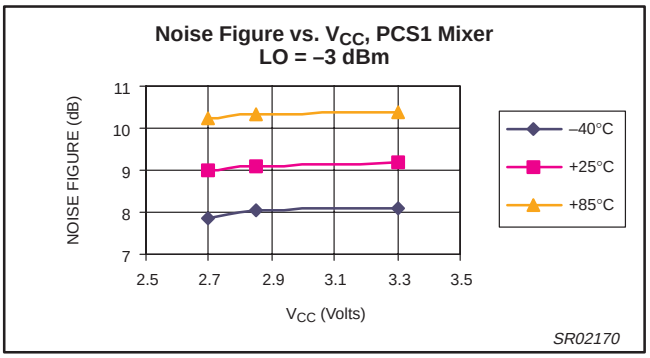


Figure 49.

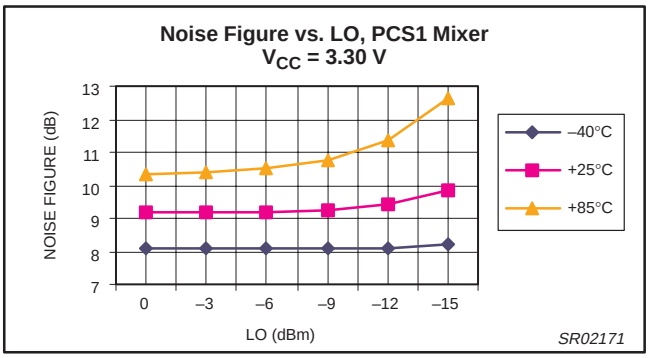


Figure 52.

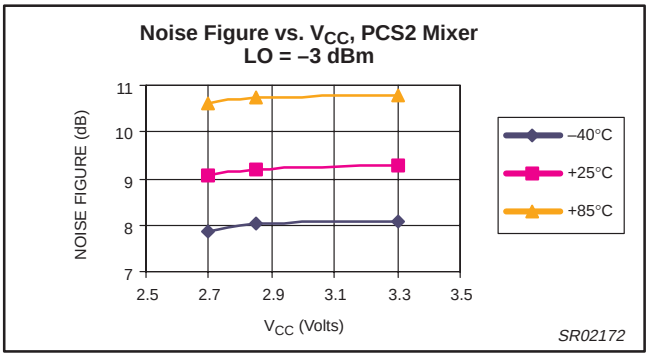


Figure 50.

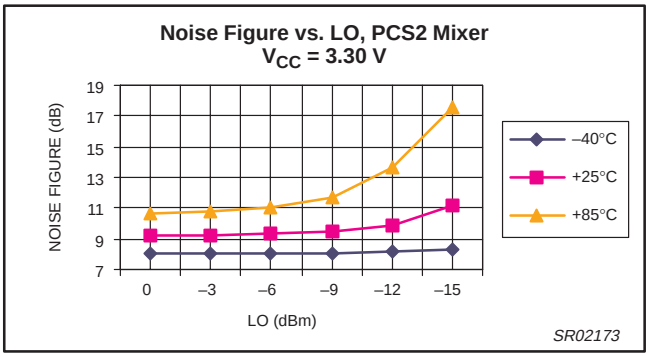


Figure 53.

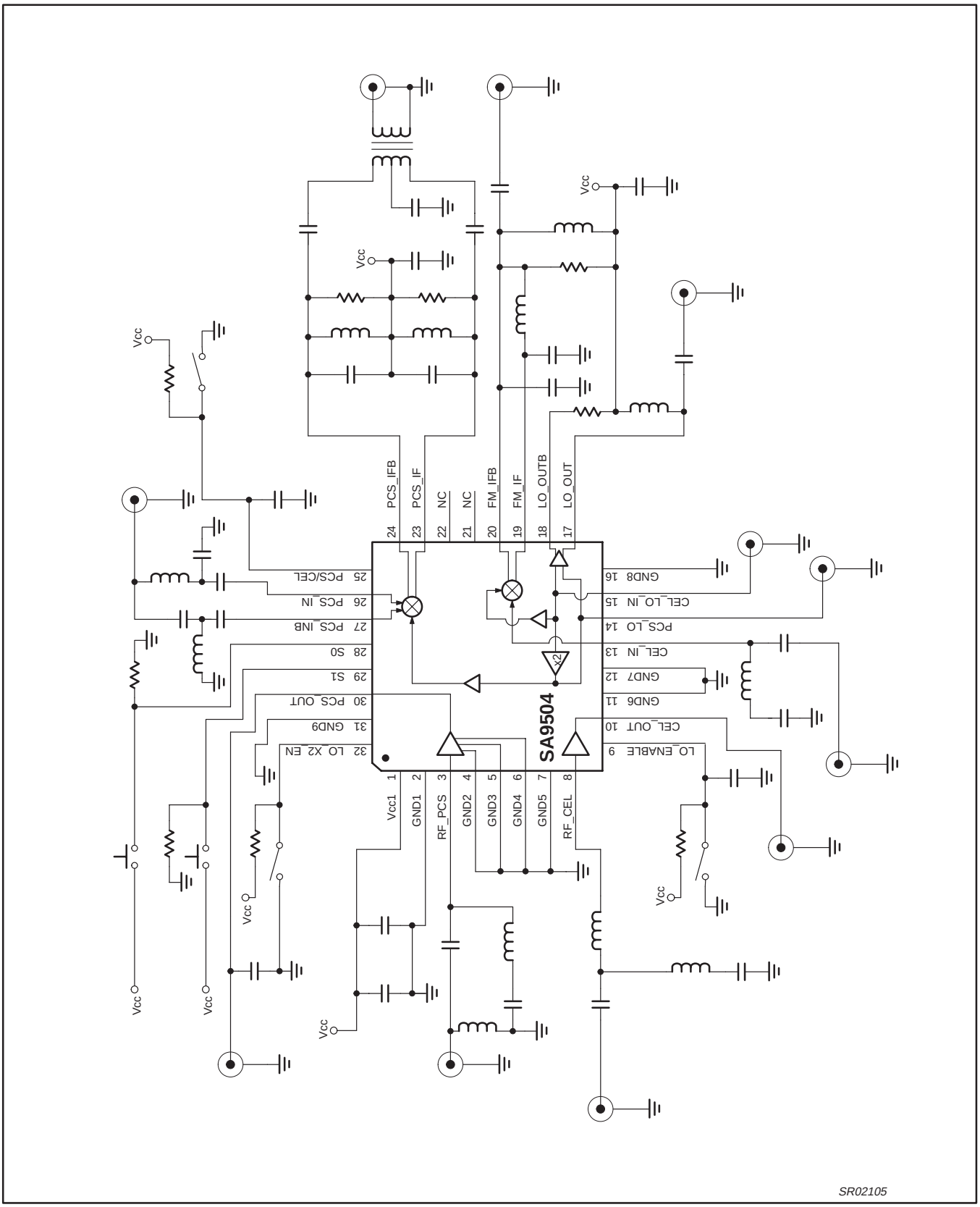


Figure 54. Demonstration Board Diagram

PINNING

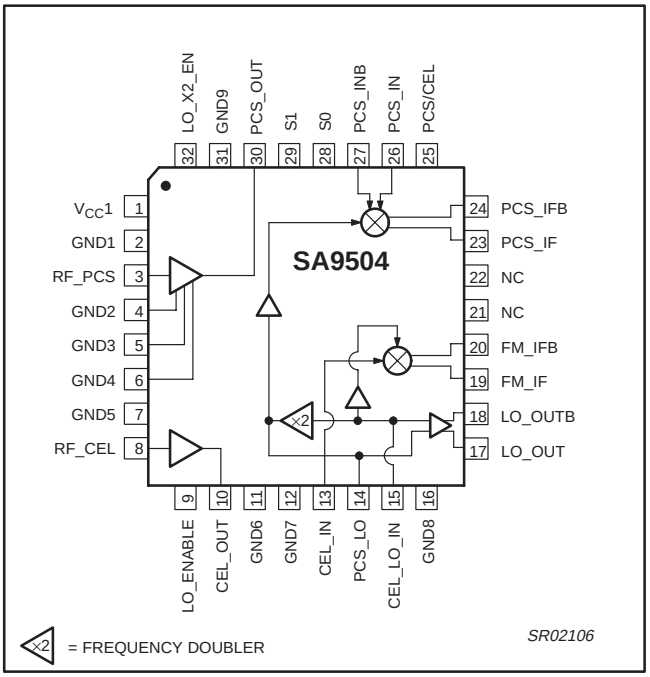
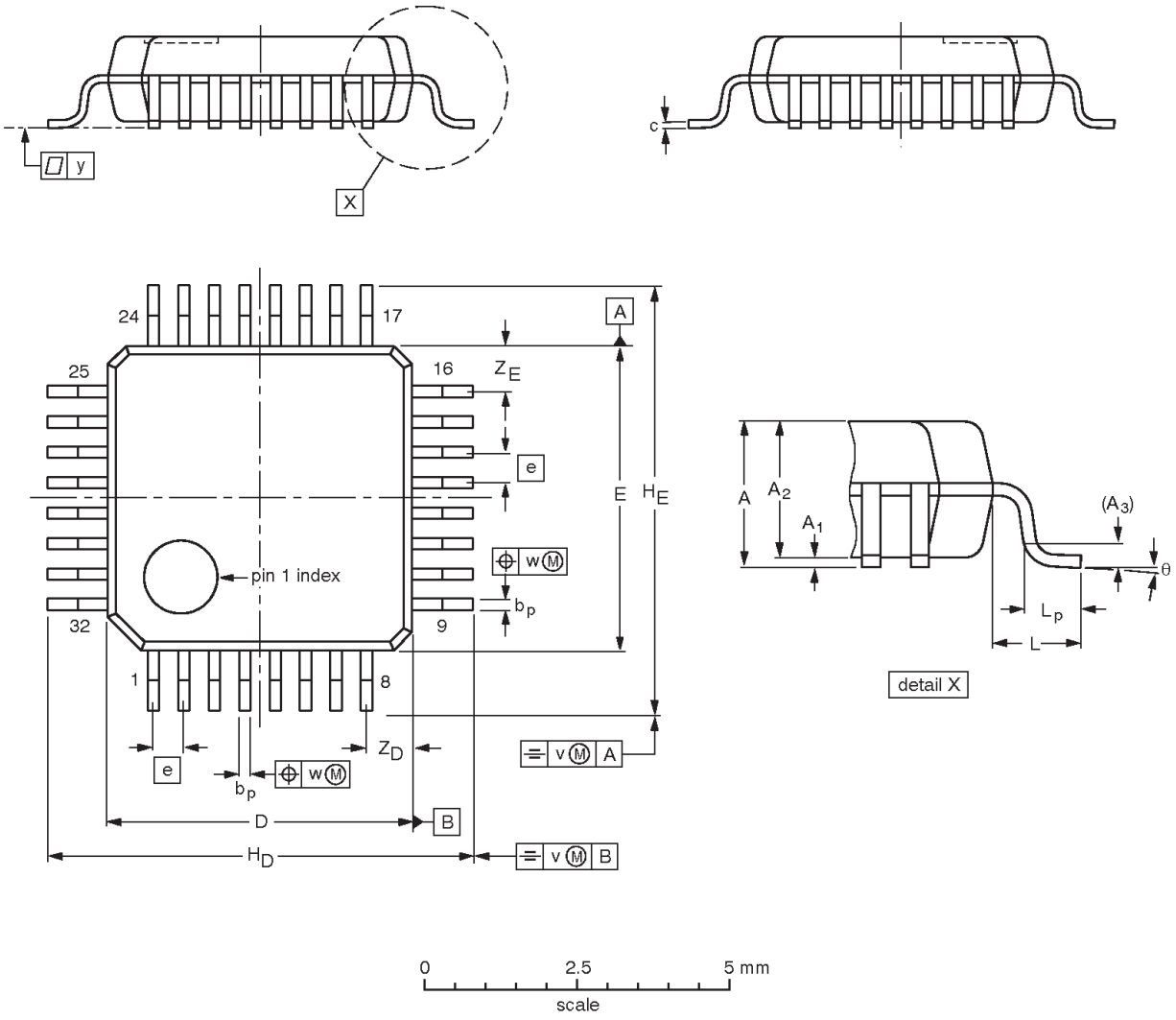


Figure 55. Pin-Out Block Diagram

Table 2. Pin function definition

PIN	NAME	DESCRIPTION
1	$V_{CC}1$	Power supply
2	GND1	Ground
3	RF_PCS	PCS LNA input
4	GND2	Ground
5	GND3	Ground
6	GND4	Ground
7	GND5	Ground
8	RF_CEL	Cellular LNA input
9	LO_ENABLE	(Tx) LO buffer enable
10	CEL_OUT	Cellular LNA output
11	GND6	Ground
12	GND7	Ground
13	CEL_IN	Cellular RF mixer input
14	PCS_LO	PCS LO input
15	CEL_LO_IN	Cellular LO input
16	GND8	Ground
17	LO_OUT	Non-inverting (Tx) LO output
18	LO_OUTB	Inverting (Tx) LO output
19	FM_IF	Non-inverting FM IF output
20	FM_IFB	Inverting FM IF output
21	NC	Do not connect
22	NC	Do not connect
23	PCS_IF	Non-inverting PCS IF output
24	PCS_IFB	Inverting PCS IF output
25	PCS/CEL	PCS and cellular band select
26	PCS_IN	Non-inverting PCS RF mixer input
27	PCS_INB	Inverting PCS RF mixer input
28	S0	Control signal S0
29	S1	Control signal S1
30	PCS_OUT	PCS LNA output
31	GND9	Ground
32	LO_X2_EN	LO frequency doubler enable in PCS mode

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

NOTES

Dual-band, CDMA/AMPS LNA and downconverter mixers

SA9504

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
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Sunnyvale, California 94088–3409
Telephone 800-234-7381

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