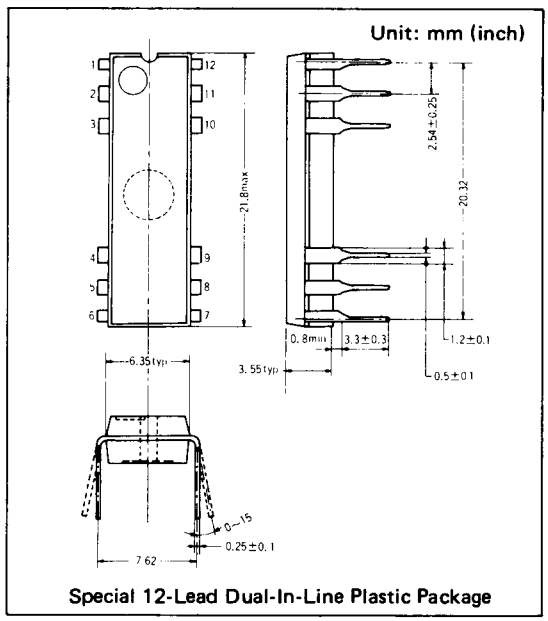
MN3011

3328-STAGE BBD with 6 TAPS

■ General description

The MN3011 is a 3328-stage BBD with 6 tap outputs suitably used for reverberation effect in audio equipments such as electronic organs. Signal of different delay time is output from each of the 6 tap outputs. Natural reverberation effect can easily be realized by mixing these output signals properly. Dealy time is freely varied by changing the clock frequency.



Special 12-Lead Dual-In-Line Plastic Package

■ Features

- 3328-stage audio signal delay device with 6 output taps.
- The stage of each output tap has no relation to multiplex, each other, therefore natural reverberation effect can be obtained by mixing output signals.
- Clock component cancellation capability.
- Dynamic rage: S/N ≧ 76dB typ.
- No insertion loss: L_i = 0dB typ.
- Low distortion: THD = 0.4% typ.
- P channel silicon gate process.
- Special 12-Lead Dual-In-Line Plastic Package.

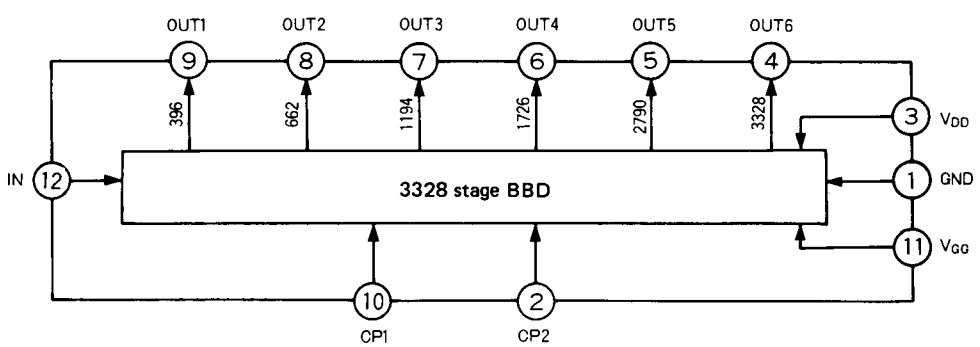
■ Applications

- Reverberation effect in audio equipment.
- Chours effect in electronic musical instruments.

■ Maximum Delay Time by Tap Output

Terminal of the Tap Output	OUT 1	OUT 2	OUT 3	OUT 4	OUT 5	OUT 6	Remarks
Stages of BBD (Stage)	396	662	1194	1726	2790	3328	
Maximum Delay Time (mS)	19.8	33.1	59.7	86.3	139.5	166.4	Clock 10KHz

■ Block Diagram



■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit	Remarks
Terminal Voltage	V_{DD}, V_{GG}	−18~+0.3	V	GND = 0 V
Input Terminal Voltage	V_I, V_{CP}	−18~+0.3	V	〃
Ouptut Voltage	V_O	−18~+0.3	V	〃
Operating Ambient Temperature	Topr	−20~+70	℃	〃
Storage Temperature	Tstg	−55~+125	℃	〃

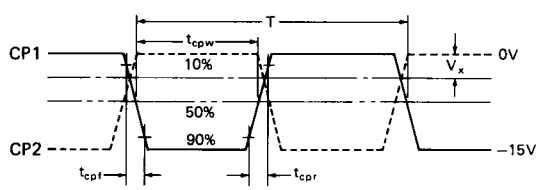
■ Operating Condition (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−14	−15	−16	V
Gate Supply Voltage	V_{GG}			$V_{DD}+1$		V
Clock Voltage "H" Level	V_{CPH}		0		−1.3	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Input Capacitance	C_{CP}				2300	pF
Clock Frequency	f_{CP}		10		100	kHz
Clock Pulse Width *1	t_{cpw}				0.5T*2	
Clock Rise Time *1	t_{cpr}				500	ns
Clock Fall Time *1	t_{cpf}				500	ns
Clock Cross Point *1	V_X		0		−3	V
Input DC Bias	V_{Bias}		−5		−10	V

■ Electrical Characteristics (Ta = 25°C, $V_{DD} = V_{CPL} = -15V$, $V_{CPH} = 0V$, $V_{GG} = -14V$, $R_L = 56k\Omega$)

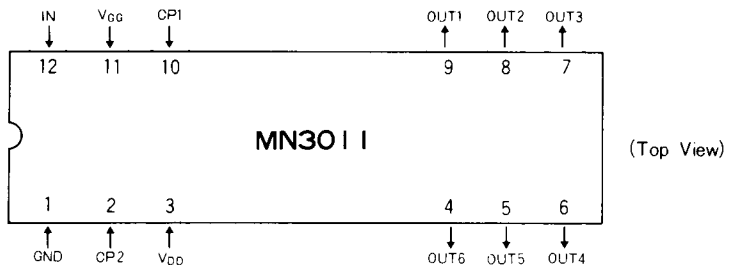
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time						
OUT 1 Terminal	t_{D1}	f_{CP}=10kHz ~100kHz	1.98		19.8	ms
OUT 2 Terminal	t_{D2}		3.31		33.1	ms
OUT 3 Terminal	t_{D3}		5.97		59.7	ms
OUT 4 Terminal	t_{D4}		8.63		86.3	ms
OUT 5 Terminal	t_{D5}		13.95		139.5	ms
OUT 6 Terminal	t_{D6}		16.64		166.4	ms
Input Signal Frequency	f_i	f_{CP} = 40kHz, −3dB	10			kHz
Input Signal Voltage	V_i	THD=2.5%	1.0			Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i = 1 kHz	−4	0	4	dB
Total Harmonic Distrotion	THD	f_{CP}=40kHz, f_i = 1 kHz V_i =0.78Vrms		0.4	2.5	%
Noise Voltage						
OUT 1, OUT 2, OUT 3 OUT 4, OUT 5, OUT 6	$V_{no\,1}$	f_{cp} = 100kHz Weighted by "A" curve			0.4	mVrms
Signal to Noise Ratio						
OUT 1, OUT 2, OUT 3 OUT 4, OUT 5, OUT 6	S/N_1	f_{cp} = 100kHz, Weighted by "A" curve Vno vs. max. output signal		76		dB

*1 Clock Pulse Waveforms



*2 $T = 1/f_{CP}$ (Clock period)

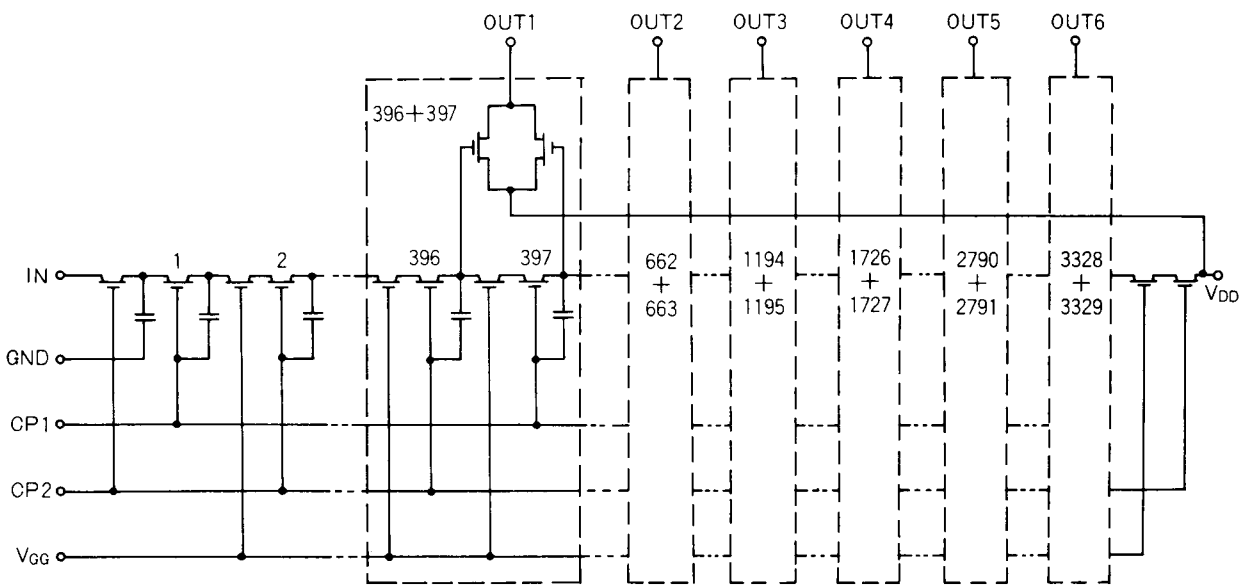
■ Terminal Assignments



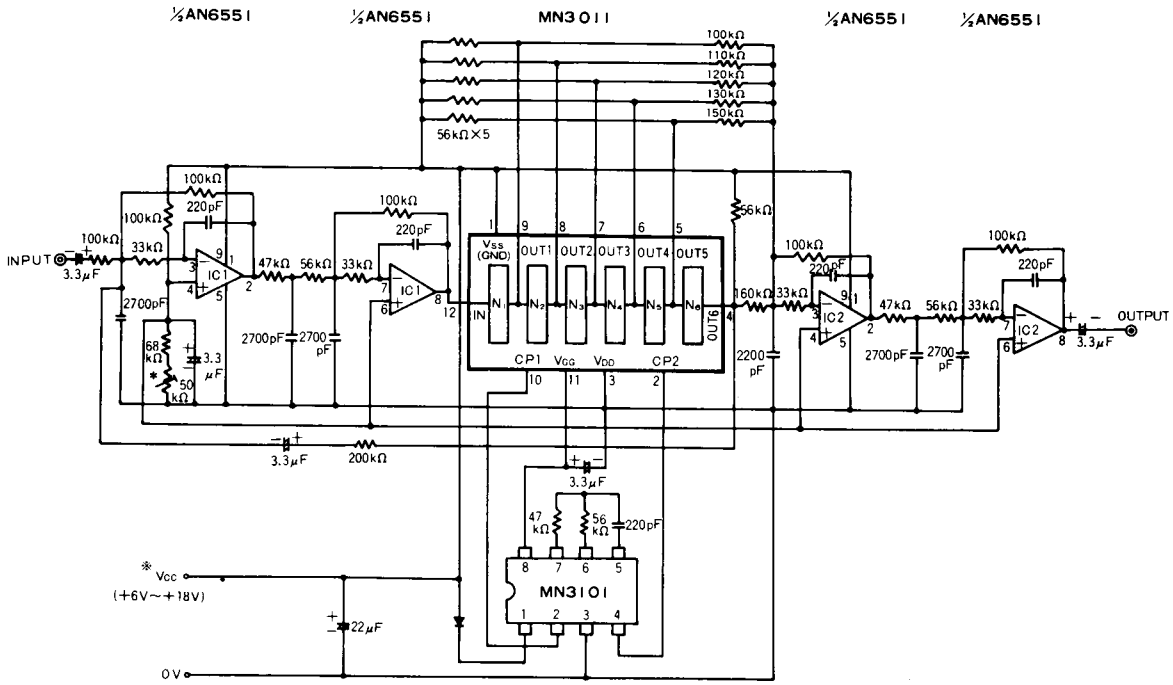
■ Terminal Description

Terminal No.	Symbol	Terminal Name	Description
1	GND	Earth terminal	Connected to the earth terminal.
2	CP2	Clock input 2	Basic clock pulse is applied to transfer the electron of BBD.
3	V_{DD}	V_{DD} applying terminal	Supply voltage of −15V is applied.
4	OUT 6	Output terminal 6	Output of 3328th and 3329th-stage are composed and output is obtained by cancelling the clock components.
5	OUT 5	Output terminal 5	Composed output of 2790th and 2791st-stage are obtained.
6	OUT 4	Output terminal 4	Composed output of 1726th and 1727th-stage are obtained.
7	OUT 3	Output terminal 3	Composed output of 1194th and 1195th-stage are obtained.
8	OUT 2	Output terminal 2	Composed output of 662nd and 663rd-stage are obtained.
9	OUT 1	Output terminal 1	Composed output of 396th and 397th-stage are obtained.
10	CP1	Clock input 1	Clock pulse of reverse phase to CP2 is applied.
11	V_{GG}	V_{GG} applying terminal	This terminal applies bias of $V_{GG} = V_{DD} + 1V$ to the MOS transistor gate that is inserted in series to transfer gate of BBD.
12	IN	Signal input terminal	Analog signal to be delayed is input. Most suitable DC bias should be applied to this terminal.

■ Circuit Diagram



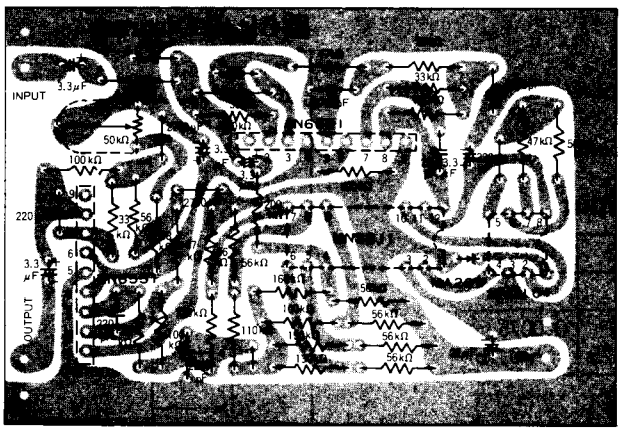
■ Application Circuit



* Adjust to minimize distortion (VR 100KΩ typ.)
* Vcc should not exceeds +18V.

Reverberation Effect Generation Circuit

■ Pattern Drawing of the Printed Circuit Board (Real size)



■ Application Circuit Electrical Characteristics (V_{CC} = +15V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	I_{CC}			11 (8)	15 (10)	mA
Power Dissipation	P_{tot}			165 (70)		mW
Signal Delay Time	t_D	OUT 6 : f_{CP}=15~20kHz	83	98	111	ms
Cut-off Frequency	f_{CO}			3		kHz
Input Signal Swing	V_i	THD=2.5%			1.1 (0.5)	Vrms
Insertion Loss	L_i	OUT 3 : f_i = 1 kHz, V_i =300mV	0	2	4	dB
Total Harmonic Distortion	THD	f_i = 1 kHz, V_i =$V_{i(max.)}$ − 6 dB		0.4 (0.5)		%
Noise Voltage	V_{no}	OUT 3 : V_i = 0 V		0.4 (0.4)		mVrms
Signal to Noise Ratio	S/N	V_S=$V_{i(max.)}$		70 (60)		dB

Contents of ( ) mean the figure at VCC = +9V