Datasheet July 29, 2005 FN2951.2

CMOS Manchester Encoder-Decoder

The HD-6409 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Non return-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409 easily interfaces to protocol controllers.

Ordering Information

PACKAGE	TEMPERATURE RANGE	1 MEGABIT/SEC	PKG. DWG. #
PDIP	-40°C to +85°C	HD3-6409-9	E20.3
SOIC	-40°C to +85°C	HD9P6409-9	M20.3
SOIC (Pb-free)	-40°C to +85°C	HD9P6409-9Z (Note)	M20.3
SOIC Tape & Reel (Pb-free)	-40°C to +85°C	HD9P6409-9Z96 (Note)	M20.3

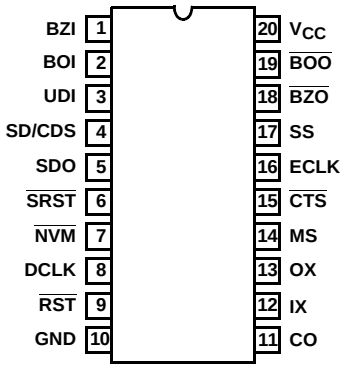
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

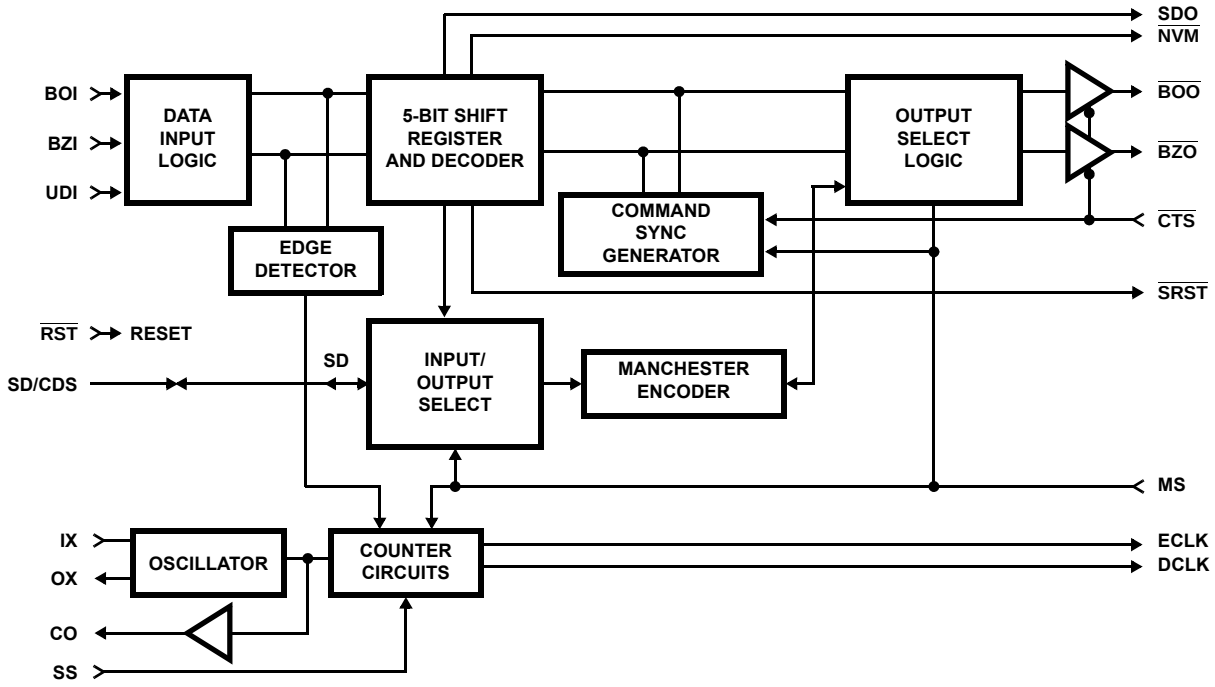
- Converter or Repeater Mode
- Independent Manchester Encoder and Decoder Operation
- Static to One Megabit/sec Data Rate Guaranteed
- Low Bit Error Rate
- Digital PLL Clock Recovery
- On Chip Oscillator
- Low Operating Power: 50mW Typical at +5V
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinouts

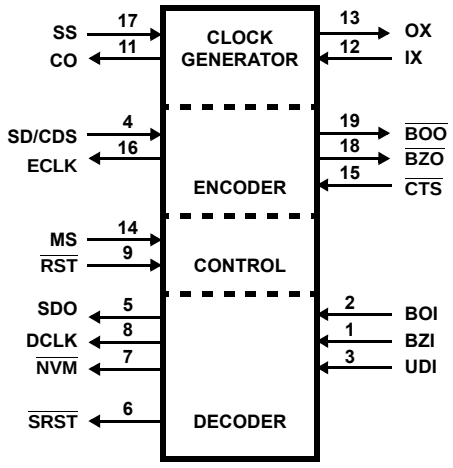
HD-6409 (PDIP, SOIC)
TOP VIEW



Block Diagram



Logic Symbol



Pin Description

PIN NUMBER	TYPE	SYMBOL	NAME	DESCRIPTION
1	I	BZI	Bipolar Zero Input	Used in conjunction with pin 2, Bipolar One Input (BOI), to input Manchester II encoded data to the decoder, BZI and BOI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BZI must be held high.
2	I	BOI	Bipolar One Input	Used in conjunction with pin 1, Bipolar Zero Input (BZI), to input Manchester II encoded data to the decoder, BOI and BZI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BOI must be held low.
3	I	UDI	Unipolar Data Input	An alternate to bipolar input (BZI, BOI), Unipolar Data Input (UDI) is used to input Manchester II encoded data to the decoder. When using pin 1 (BZI) and pin 2 (BOI) for data input, UDI must be held low.
4	I/O	SD/CDS	Serial Data/Command Data Sync	In the converter mode, SD/CDS is an input used to receive serial NRZ data. NRZ data is accepted synchronously on the falling edge of encoder clock output (ECLK). In the repeater mode, SD/CDS is an output indicating the status of last valid sync pattern received. A high indicates a command sync and a low indicates a data sync pattern.
5	O	SDO	Serial Data Out	The decoded serial NRZ data is transmitted out synchronously with the decoder clock (DCLK). SDO is forced low when $\overline{RST}$ is low.
6	O	$\overline{SRST}$	$\overline{Serial\ Reset}$	In the converter mode, $\overline{SRST}$ follows $\overline{RST}$. In the repeater mode, when $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero, and a valid synchronization sequence is received.
7	O	$\overline{NVM}$	$\overline{Nonvalid\ Manchester}$	A low on $\overline{NVM}$ indicates that the decoder has received invalid Manchester data and present data on Serial Data Out (SDO) is invalid. A high indicates that the sync pulse and data were valid and SDO is valid. $\overline{NVM}$ is set low by a low on $\overline{RST}$, and remains low after $\overline{RST}$ goes high until valid sync pulse followed by two valid Manchester bits is received.
8	O	DCLK	Decoder Clock	The decoder clock is a 1X clock recovered from BZI and BOI, or UDI to synchronously output received NRZ data (SDO).
9	I	$\overline{RST}$	$\overline{Reset}$	In the converter mode, a low on $\overline{RST}$ forces SDO, DCLK, $\overline{NVM}$, and $\overline{SRST}$ low. A high on $\overline{RST}$ enables SDO and DCLK, and forces $\overline{SRST}$ high. $\overline{NVM}$ remains low after $\overline{RST}$ goes high until a valid sync pulse followed by two Manchester bits is received, after which it goes high. In the repeater mode, $\overline{RST}$ has the same effect on SDO, DCLK and $\overline{NVM}$ as in the converter mode. When $\overline{RST}$ goes low, $\overline{SRST}$ goes low and remains low after $\overline{RST}$ goes high. $\overline{SRST}$ goes high only when $\overline{RST}$ is high, the reset bit is zero and a valid synchronization sequence is received.
10	I	GND	Ground	Ground
11	O	C_O	Clock Output	Buffered output of clock input I_X. May be used as clock signal for other peripherals.
12	I	I_X	Clock Input	I_X is the input for an external clock or, if the internal oscillator is used, I_X and O_X are used for the connection of the crystal.
13	O	O_X	Clock Drive	If the internal oscillator is used, O_X and I_X are used for the connection of the crystal.
14	I	MS	Mode Select	MS must be held low for operation in the converter mode, and high for operation in the repeater mode.
15	I	$\overline{CTS}$	Clear to Send	In the converter mode, a high disables the encoder, forcing outputs $\overline{BOO}$, $\overline{BZO}$ high and ECLK low. A high to low transition of $\overline{CTS}$ initiates transmission of a Command sync pulse. A low on $\overline{CTS}$ enables $\overline{BOO}$, $\overline{BZO}$, and ECLK. In the repeater mode, the function of $\overline{CTS}$ is identical to that of the converter mode with the exception that a transition of $\overline{CTS}$ does not initiate a synchronization sequence.
16	O	ECLK	Encoder Clock	In the converter mode, ECLK is a 1X clock output used to receive serial NRZ data to SD/CDS. In the repeater mode, ECLK is a 2X clock which is recovered from BZI and BOI data by the digital phase locked loop.
17	I	SS	Speed Select	A logic high on SS sets the data rate at 1/32 times the clock frequency while a low sets the data rate at 1/16 times the clock frequency.
18	O	$\overline{BZO}$	$\overline{Bipolar\ Zero\ Output}$	$\overline{BZO}$ and its logical complement $\overline{BOO}$ are the Manchester data outputs of the encoder. The inactive state for these outputs is in the high state.
19	O	$\overline{BOO}$	$\overline{Bipolar\ One\ Out}$	See pin 18.
20	I	V_{CC}	V_{CC}	V_{CC} is the +5V power supply pin. A 0.1µF decoupling capacitor from V_{CC} (pin-20) to GND (pin-10) is recommended.

NOTE: (I) Input (O) Output

Encoder Operation

The encoder uses free running clocks at 1X and 2X the data rate derived from the system clock I_X for internal timing. $\overline{CTS}$ is used to control the encoder outputs, ECLK, $\overline{BOO}$ and $\overline{BZO}$. A free running 1X ECLK is transmitted out of the encoder to drive the external circuits which supply the NRZ data to the MED at pin SD/CDS.

A low on $\overline{CTS}$ enables encoder outputs ECLK, $\overline{BOO}$ and $\overline{BZO}$, while a high on $\overline{CTS}$ forces $\overline{BZO}$, $\overline{BOO}$ high and holds ECLK low. When $\overline{CTS}$ goes from high to low (1), a synchronization sequence is transmitted out on $\overline{BOO}$ and $\overline{BZO}$. A synchronization sequence consists of eight Manchester “0” bits followed by a command sync pulse. (2) A command sync pulse is a 3-bit wide pulse with the first 1 1/2 bits high followed by 1 1/2 bits low. (3) Serial NRZ data is clocked into the encoder at SD/CDS on the high to low transition of ECLK during the command sync pulse. The NRZ data received is encoded into Manchester II data and transmitted out on $\overline{BOO}$ and $\overline{BZO}$ following the command sync pulse. (4) Following the synchronization sequence, input data is encoded and transmitted out continuously without parity check or word framing. The length of the data block encoded is defined by $\overline{CTS}$. Manchester data out is inverted.

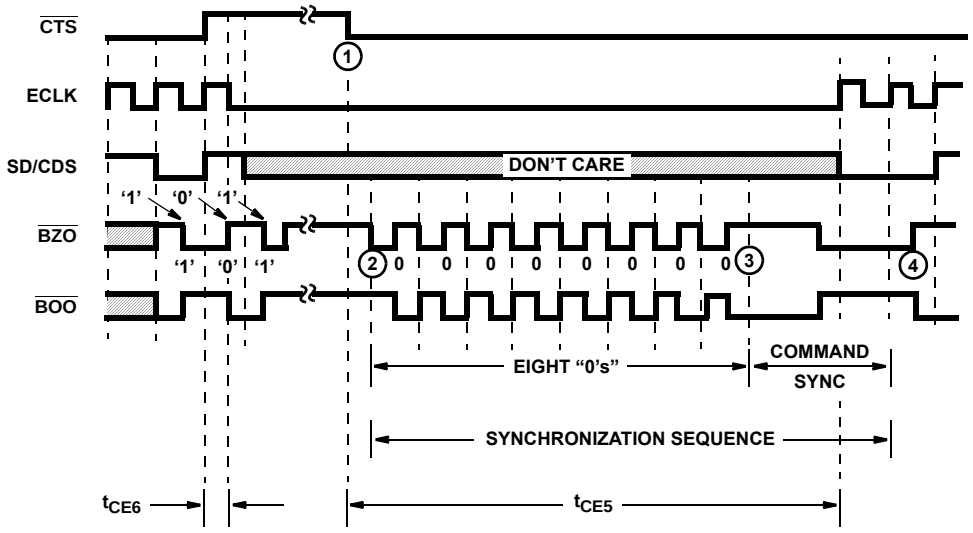


FIGURE 1. ENCODER OPERATION

Decoder Operation

The decoder requires a single clock with a frequency 16X or 32X the desired data rate. The rate is selected on the speed select with SS low producing a 16X clock and high a 32X clock. For long data links the 32X mode should be used as this permits a wider timing jitter margin. The internal operation of the decoder utilizes a free running clock synchronized with incoming data for its clocking.

The Manchester II encoded data can be presented to the decoder in either of two ways. The Bipolar One and Bipolar Zero inputs will accept data from differential inputs such as a comparator sensed transformer coupled bus. The Unipolar Data input can only accept noninverted Manchester II encoded data i.e. Bipolar $\overline{One}$ $\overline{Out}$ through an inverter to Unipolar Data Input. The decoder continuously monitors this data input for valid sync pattern. Note that while the MED encoder section can generate only a command sync pattern, the decoder can recognize either a command or data sync pattern. A data sync is a logically inverted command sync.

There is a three bit delay between UDI, BOI, or BZI input and the decoded NRZ data transmitted out of SDO.

Control of the decoder outputs is provided by the $\overline{RST}$ pin. When $\overline{RST}$ is low, SDO, DCLK and $\overline{NVM}$ are forced low. When $\overline{RST}$ is high, SDO is transmitted out synchronously with the recovered clock DCLK. The $\overline{NVM}$ output remains low after a low to high transition on $\overline{RST}$ until a valid sync pattern is received.

The decoded data at SDO is in NRZ format. DCLK is provided so that the decoded bits can be shifted into an external register on every high to low transition of this clock. Three bit periods after an invalid Manchester bit is received on UDI, or BOI, $\overline{NVM}$ goes low synchronously with the questionable data output on SDO. FURTHER, THE DECODER DOES NOT REESTABLISH PROPER DATA DECODING UNTIL ANOTHER SYNC PATTERN IS RECOGNIZED.

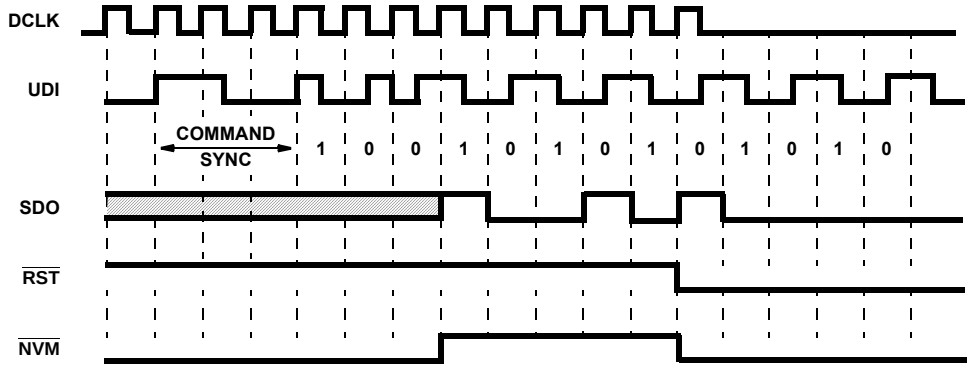


FIGURE 2. DECODER OPERATION

Repeater Operation

Manchester II data can be presented to the repeater in either of two ways. The inputs Bipolar One In and Bipolar Zero In will accept data from differential inputs such as a comparator or sensed transformer coupled bus. The input Unipolar Data In accepts only noninverted Manchester II coded data. The decoder requires a single clock with a frequency 16X or 32X the desired data rate. This clock is selected to 16X with Speed Select low and 32X with Speed Select high. For long data links the 32X mode should be used as this permits a wider timing jitter margin.

The inputs UDI, or BOI, BZI are delayed approximately 1/2 bit period and repeated as outputs $\overline{BOO}$ and $\overline{BZO}$. The 2X ECLK is transmitted out of the repeater synchronously with $\overline{BOO}$ and $\overline{BZO}$.

A low on $\overline{CTS}$ enables ECLK, $\overline{BOO}$, and $\overline{BZO}$. In contrast to the converter mode, a transition on CTS does not initiate a synchronization sequence of eight 0's and a command sync. The repeater mode does recognize a command or data sync pulse. SD/CDS is an output which reflects the state of the most recent sync pulse received, with high indicating a command sync and low indicating a data sync.

When $\overline{RST}$ is low, the outputs SDO, DCLK, and $\overline{NVM}$ are low, and $\overline{SRST}$ is set low. $\overline{SRST}$ remains low after $\overline{RST}$ goes high and is not reset until a sync pulse and two valid manchester bits are received with the reset bit low. The reset bit is the first data bit after the sync pulse. With RST high, NRZ Data is transmitted out of Serial Data Out synchronously with the 1X DCLK.

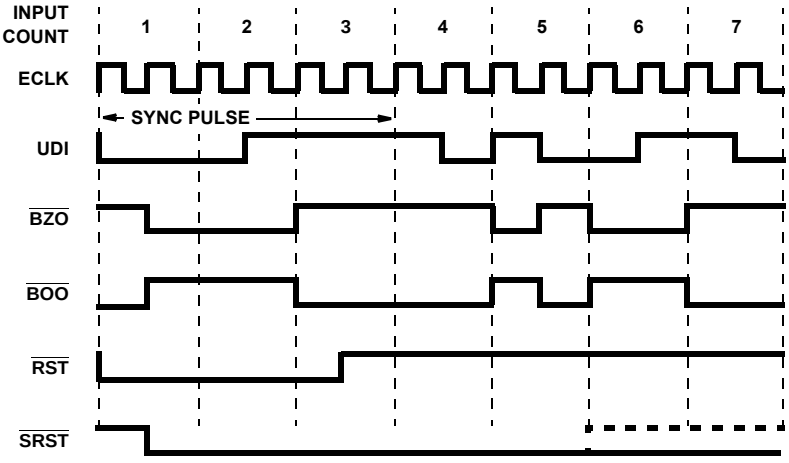


FIGURE 3. REPEATER OPERATION

Manchester Code

Nonreturn-to-Zero (NRZ) code represents the binary values logic-O and logic-1 with a static level maintained throughout the data cell. In contrast, Manchester code represents data with a level transition in the middle of the data cell. Manchester has bandwidth, error detection, and synchronization advantages over NRZ code.

The Manchester II code Bipolar One and Bipolar Zero shown below are logical complements. The direction of the transition indicates the binary value of data. A logic-0 in Bipolar One is defined as a Low to high transition in the middle of the data cell, and a logic-1 as a high to low mid bit transition, Manchester II is also known as Biphase-L code.

The bandwidth of NRZ is from DC to the clock frequency fc/2, while that of Manchester is from fc/2 to fc. Thus, Manchester can be AC or transformer coupled, which has considerable advantages over DC coupling. Also, the ratio of maximum to minimum frequency of Manchester extends one octave, while the ratio for NRZ is the range of 5-10 octaves. It is much easier to design a narrow band than a wideband amp.

Secondly, the mid bit transition in each data cell provides the code with an effective error detection scheme. If noise produces a logic inversion in the data cell such that there is no transition, an error indiction is given, and synchronization must be re-established. This places relatively stringent requirements on the incoming data.

The synchronization advantages of using the HD-6409 and Manchester code are several fold. One is that Manchester is a self clocking code. The clock in serial data communication defines the position of each data cell. Non self clocking codes, as NRZ, often require an extra clock wire or clock track (in magnetic recording). Further, there can be a phase variation between the clock and data track. Crosstalk between the two may be a problem. In Manchester, the serial data stream contains both the clock and the data, with the position of the mid bit transition representing the clock, and the direction of the transition representing data. There is no phase variation between the clock and the data.

A second synchronization advantage is a result of the number of transitions in the data. The decoder resynchronizes on each transition, or at least once every data cell. In contrast, receivers using NRZ, which does not necessarily have transitions, must resynchronize on frame bit transitions, which occur far less often, usually on a character basis. This more frequent resynchronization eliminates the cumulative effect of errors over successive data cells. A final synchronization advantage concerns the HD-6409's sync pulse used to initiate synchronization. This three bit wide pattern is sufficiently distinct from Manchester data that a false start by the receiver is unlikely.

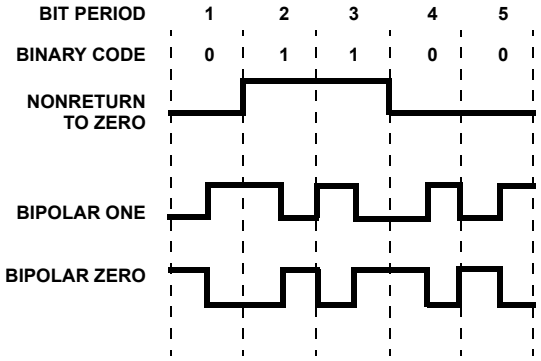


FIGURE 4. MANCHESTER CODE

Crystal Oscillator Mode

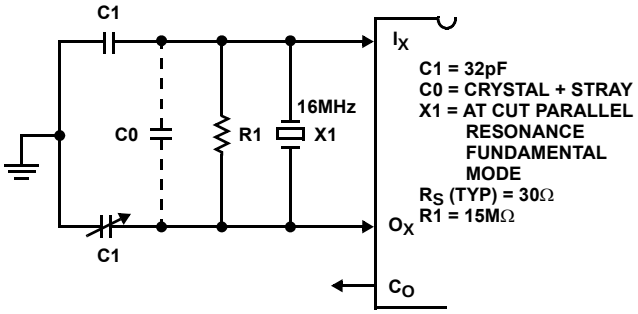


FIGURE 5. CRYSTAL OSCILLATOR MODE

LC Oscillator Mode

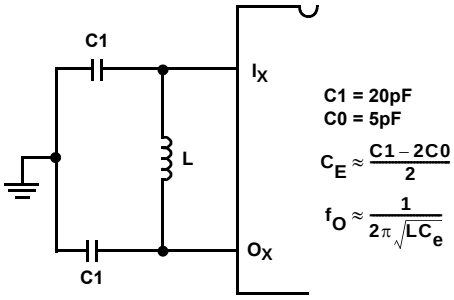


FIGURE 6. LC OSCILLATOR MODE

Using the 6409 as a Manchester Encoded UART

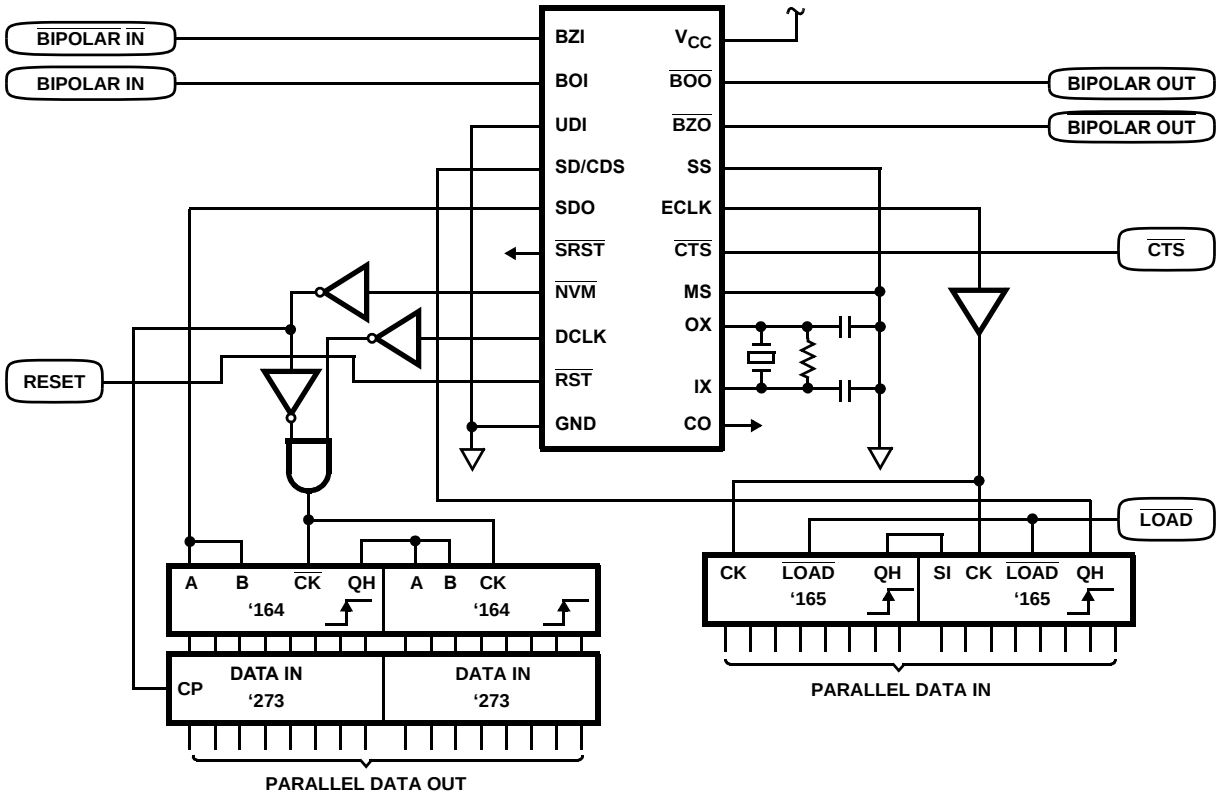


FIGURE 7. MANCHESTER ENCODER UART

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
PDIP Package	75°C/W	N/A
SOIC Package	100°C/W	N/A

Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(Lead Tips Only for Surface Mount Packages)

Die Characteristics

Gate Count . . . . . 250 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range . . . . . -40°C to +85°C
Operating Voltage Range . . . . . +4.5V to +5.5V
Input Rise and Fall Times . . . . . 50ns Max
Sync. Transition Span (t2) . . . . . 1.5 DBP Typical, (Notes 1, 2)
Short Data Transition Span (t4) . . . . . 0.5DBP Typical, (Notes 1, 2)
Long Data Transition Span (t5) . . . . . 1.0DBP Typical, (Notes 1, 2)
Zero Crossing Tolerance (tCD5) . . . . . (Note 3)

NOTES:

1. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.
2. The input conditions specified are nominal values, the actual input waveforms transition spans may vary by ± 2 I_X clock cycles (16X mode) or ± 6 I_X clock cycles (32X mode).
3. The maximum zero crossing tolerance is ± 2 I_X clock cycles (16X mode) or ± 6 I_X clock cycles (32 mode) from the nominal.

DC Electrical Specifications V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C (HD-6409-9)

SYMBOL	PARAMETER	MIN	MAX	UNITS	(NOTE 1) TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}	-	V	V_{CC} = 4.5V
V_{IL}	Logical "0" Input Voltage	-	20% V_{CC}	V	V_{CC} = 4.5V
V_{IHR}	Logic "1" Input Voltage ($\overline{Reset}$)	V_{CC} -0.5	-	V	V_{CC} = 5.5V
V_{ILR}	Logic "0" Input Voltage ($\overline{Reset}$)	-	GND +0.5	V	V_{CC} = 4.5V
V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5	-	V	V_{CC} = 5.5V
V_{ILC}	Logical "0" Input Voltage (Clock)	-	GND +0.5	V	V_{CC} = 4.5V
I_I	Input Leakage Current (Except I_X)	-1.0	+1.0	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
I_I	Input Leakage Current (I_X)	-20	+20	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
I_O	I/O Leakage Current	-10	+10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5V
V_{OH}	Output HIGH Voltage (All Except O_X)	V_{CC} -0.4	-	V	I_{OH} = -2.0mA, V_{CC} = 4.5V (Note 2)
V_{OL}	Output LOW Voltage (All Except O_X)	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.5V (Note 2)
I_{CCSB}	Standby Power Supply Current	-	100	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open
I_{CCOP}	Operating Power Supply Current	-	18.0	mA	f = 16.0MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V, C_L = 50pF
F_T	Functional Test	-	-	-	(Note 1)

NOTES:

1. Tested as follows: f = 16MHz, V_{IH} = 70% V_{CC}, V_{IL} = 20% V_{CC}, $V_{OH} \geq V_{CC}/2$, and $V_{OL} \leq V_{CC}/2$, V_{CC} = 4.5V and 5.5V.
2. Interchanging of force and sense conditions is permitted

Capacitance T_A = +25°C, Frequency = 1MHz

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	10	pF	All measurements are referenced to device GND
C_{OUT}	Output Capacitance	12	pF	

AC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = -40°C to +85°C (HD-6409-9)

SYMBOL	PARAMETER	MIN	MAX	UNITS	(NOTE 1) TEST CONDITIONS
f_C	Clock Frequency	-	16	MHz	-
t_C	Clock Period	$1/f_C$	-	sec	-
t_1	Bipolar Pulse Width	t_C+10	-	ns	-
t_3	One-Zero Overlap	-	t_C-10	ns	-
t_{CH}	Clock High Time	20	-	ns	f = 16.0MHz
t_{CL}	Clock Low Time	20	-	ns	f = 16.0MHz
t_{CE1}	Serial Data Setup Time	120	-	ns	-
t_{CE2}	Serial Data Hold Time	0	-	ns	-
t_{CD2}	DCLK to SDO, $\overline{NVM}$	-	40	ns	-
t_{R2}	ECLK to $\overline{BZO}$	-	40	ns	-
t_r	Output Rise Time (All except Clock)	-	50	ns	From 1.0V to 3.5V, C_L = 50pF, Note 2
t_f	Output Fall Time (All except Clock)	-	50	ns	From 3.5V to 1.0V, C_L = 50pF, Note 2
t_r	Clock Output Rise Time	-	11	ns	From 1.0V to 3.5V, C_L = 20pF, Note 2
t_f	Clock Output Fall Time	-	11	ns	From 3.5V to 1.0V, C_L = 20pF, Note 2
t_{CE3}	ECLK to $\overline{BZO}$, $\overline{BOO}$	0.5	1.0	DBP	Notes 2, 3
t_{CE4}	$\overline{CTS}$ Low to $\overline{BZO}$, $\overline{BOO}$ Enabled	0.5	1.5	DBP	Notes 2, 3
t_{CE5}	$\overline{CTS}$ Low to ECLK Enabled	10.5	11.5	DBP	Notes 2, 3
t_{CE6}	$\overline{CTS}$ High to ECLK Disabled	-	1.0	DBP	Notes 2, 3
t_{CE7}	$\overline{CTS}$ High to $\overline{BZO}$, $\overline{BOO}$ Disabled	1.5	2.5	DBP	Notes 2, 3
t_{CD1}	UDI to SDO, $\overline{NVM}$	2.5	3.0	DBP	Notes 2, 3
t_{CD3}	$\overline{RST}$ Low to CDLK, SDO, $\overline{NVM}$ Low	0.5	1.5	DBP	Notes 2, 3
t_{CD4}	$\overline{RST}$ High to DCLK, Enabled	0.5	1.5	DBP	Notes 2, 3
t_{R1}	UDI to $\overline{BZO}$, $\overline{BOO}$	0.5	1.0	DBP	Notes 2, 3
t_{R3}	UDI to SDO, $\overline{NVM}$	2.5	3.0	DBP	Notes 2, 3

NOTES:

1. AC testing as follows: f = 4.0MHz, V_{IH} = 70% V_{CC}, V_{IL} = 20% V_{CC}, Speed Select = 16X, $V_{OH} \geq V_{CC}/2$, $V_{OL} \leq V_{CC}/2$, V_{CC} = 4.5V and 5.5V. Input rise and fall times driven at 1ns/V, Output load = 50pF.
2. Guaranteed via characteristics at initial device design and after major process and/or design changes, not tested.
3. DBP-Data Bit Period, Clock Rate = 16X, one DBP = 16 Clock Cycles; Clock Rate = 32X, one DBP = 32 Clock Cycles.

Timing Waveforms

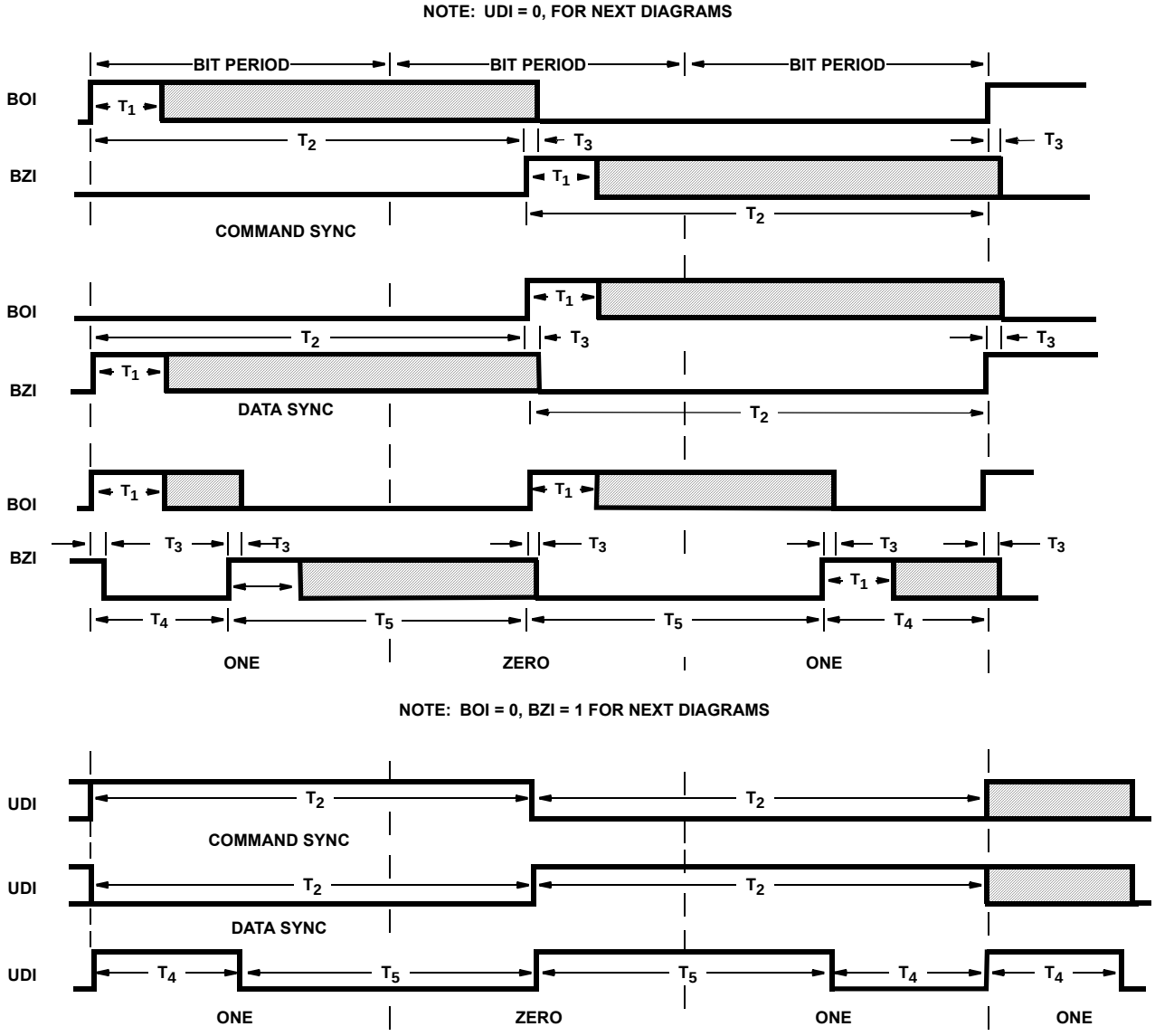


FIGURE 8.

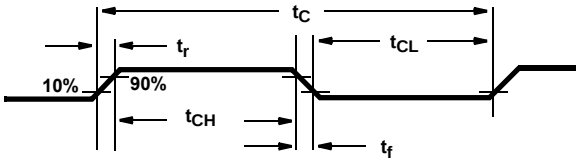


FIGURE 9. CLOCK TIMING

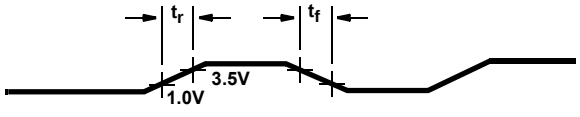


FIGURE 10. OUTPUT WAVEFORM

Timing Waveforms (Continued)

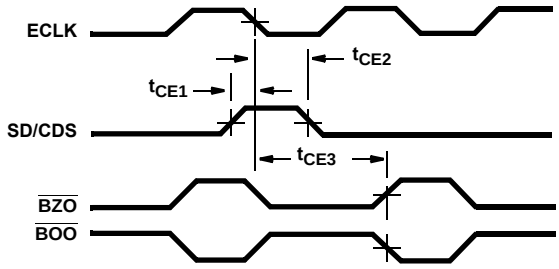


FIGURE 11. ENCODER TIMING

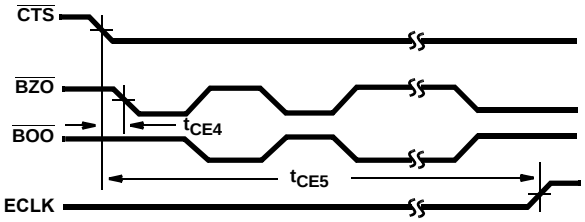


FIGURE 12. ENCODER TIMING

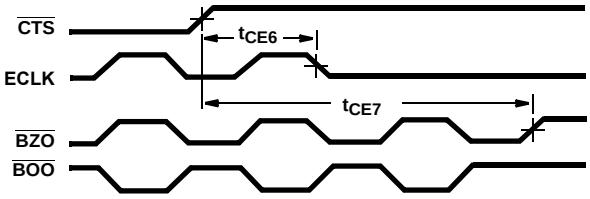
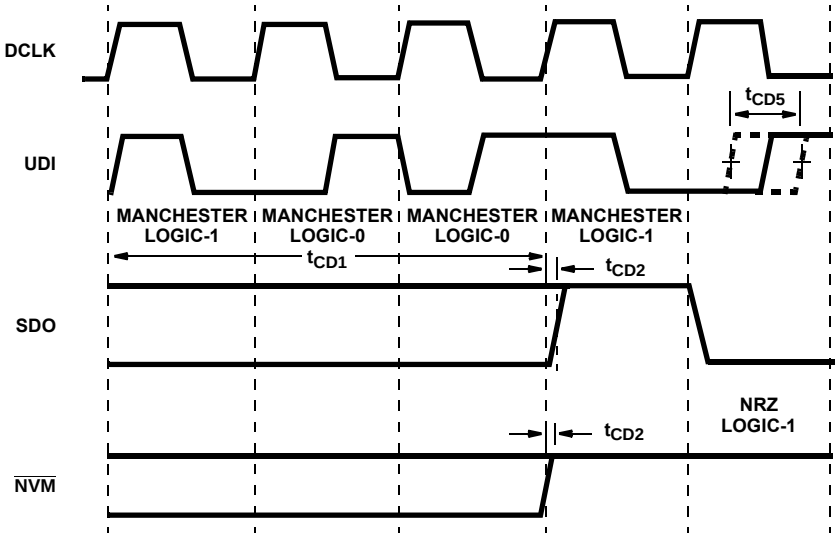


FIGURE 13. ENCODER TIMING



NOTE: Manchester Data-In is not synchronous with Decoder Clock. Decoder Clock is synchronous with decoded NRZ out of SDO.

FIGURE 14. DECODER TIMING

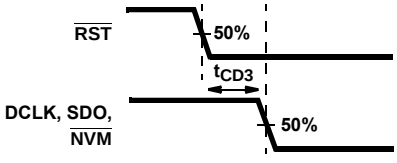


FIGURE 15. DECODER TIMING

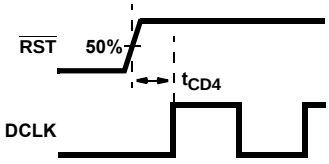


FIGURE 16. DECODER TIMING

Timing Waveforms (Continued)

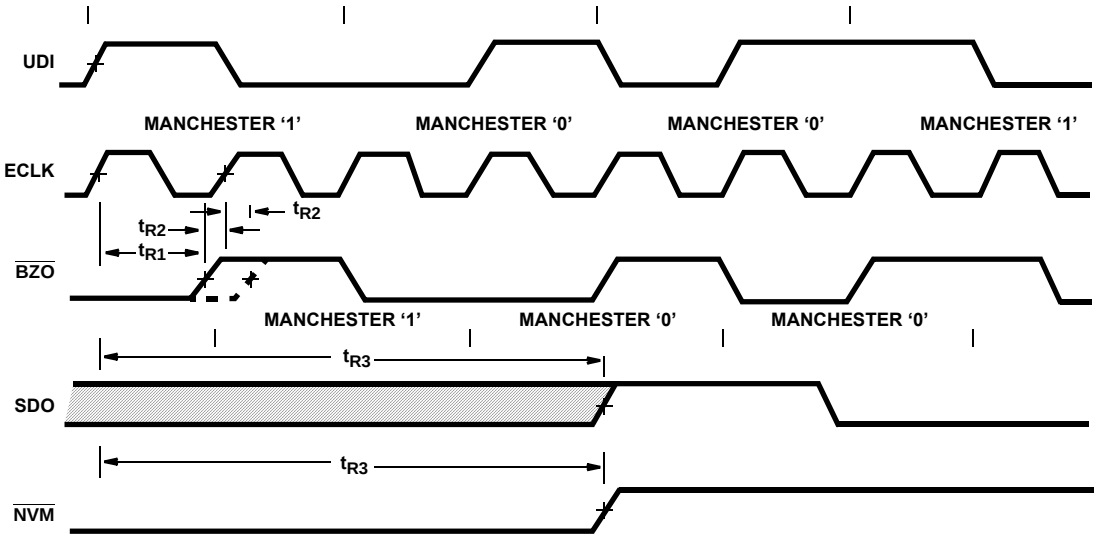
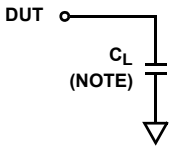


FIGURE 17. REPEATER TIMING

Test Load Circuit



NOTE: INCLUDES STRAY AND JIG CAPACITANCE

FIGURE 18. TEST LOAD CIRCUIT