MX23C4000

4M-BIT MASK ROM (8 BIT OUTPUT)

FEATURES

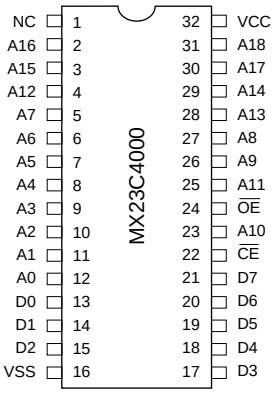
- Bit organization
  - 512K x 8 (byte mode)
- Fast access time
  - Random access: 90ns (max.)
- Current
  - Operating: 35mA
  - Standby: 100uA
- Supply voltage
  - 5V ± 10%
- Package
  - 32 pin PDIP (600 mil)
  - 32 pin PLCC
  - 32 pin SOP (450 mil)
  - 32 pin TSOP (8mm x 20mm)

ORDER INFORMATION

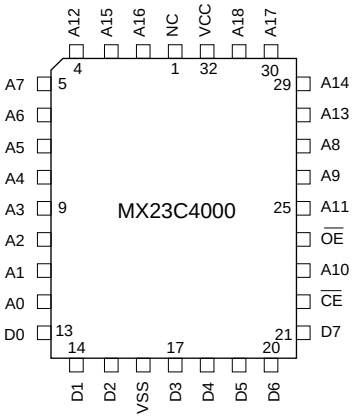
Part No.	Access Time	Package
MX23C4000PC-90	90ns	32 pin PDIP
MX23C4000PC-10	100ns	32 pin PDIP
MX23C4000PC-12	120ns	32 pin PDIP
MX23C4000PC-15	150ns	32 pin PDIP
MX23C4000QC-10	100ns	32 pin PLCC
MX23C4000QC-12	120ns	32 pin PLCC
MX23C4000QC-15	150ns	32 pin PLCC
MX23C4000MC-90	90ns	32 pin SOP
MX23C4000MC-10	100ns	32 pin SOP
MX23C4000MC-12	120ns	32 pin SOP
MX23C4000MC-15	150ns	32 pin SOP
MX23C4000TC-10	100ns	32 pin TSOP
MX23C4000TC-12	120ns	32 pin TSOP
MX23C4000TC-15	150ns	32 pin TSOP

PIN CONFIGURATION

32 PDIP / 32 SOP



32 PLCC



PIN DESCRIPTION

Symbol	Pin Function
A0~A18	Address Inputs
D0~D7	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

32 TSOP

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Power Supply Voltage	VCC	-0.5V to 7.0V
Input Voltage	VI	-0.5V to VCC + 0.5V
Output Voltage	VO	-0.5V to VCC + 0.5V
Ambient Operating Temperature	Topr	-10° C to 70° C
Storage Temperature	Tstg	-65° C to 125° C

Note: minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -2.0V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = -10° C ~ 70° C, VCC = 5.0V ±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	0.8VCC	-	IOH = -100uA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.5V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	10uA	0V, VCC
Output Leakage Current	ILO	-	10uA	0V, VCC
Operating Current	ICC1	-	35mA	tRC = 100ns, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$ = VIH
Standby Current (CMOS)	ISTB2	-	100uA	$\overline{CE}$ > VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25° C, f = 1MHz
Output Capacitance	COUT	-	10pF	Ta = 25° C, f = 1MHz

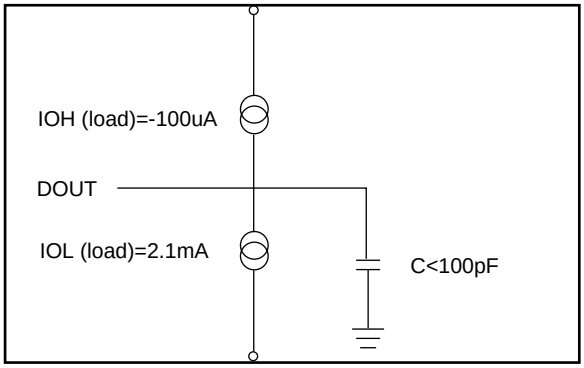
AC CHARACTERISTICS (Ta = -10° C ~ 70° C, VCC = 5.0V ± 10%)

Item	Symbol	23C4000-90		23C4000-10		23C4000-12		23C4000-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	90ns	-	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	90ns	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	90ns	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	45ns	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns	-	20ns

Note : Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

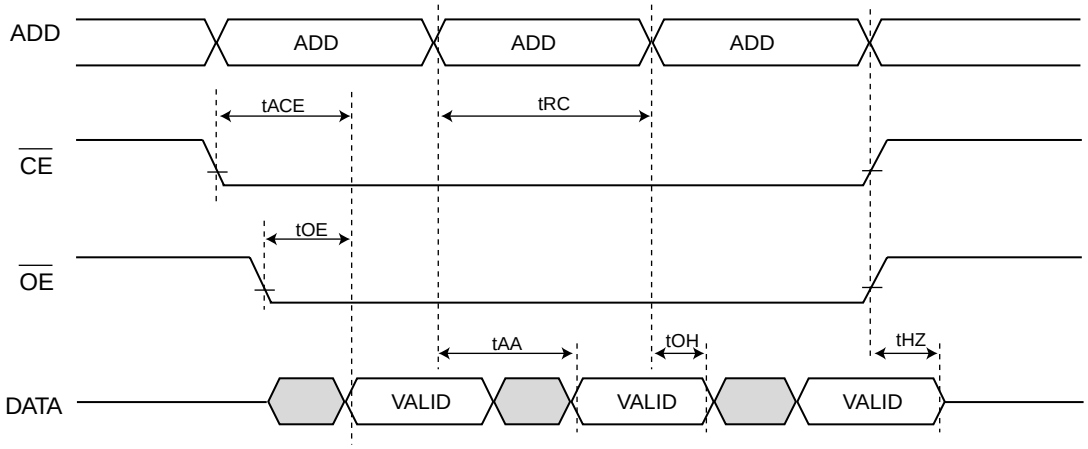
- Input Pulse Levels : 0.4V~2.4V
- Input Rise and Fall Times : 10ns
- Input Timing Level : 1.5V
- Output Timing Level : 0.8V and 2.0V
- Output Load : See Figure



Note:No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

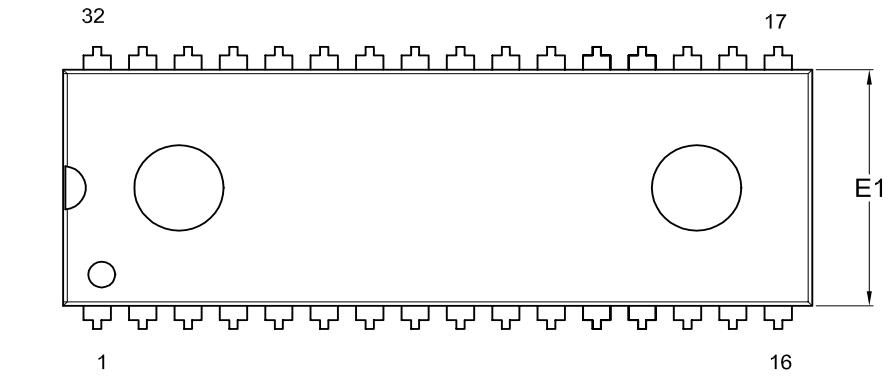
RANDOM READ

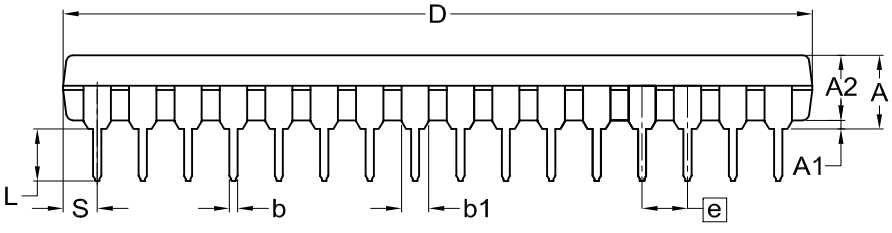


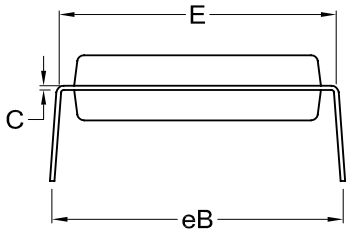
Note:$\overline{CE}$, $\overline{OE}$ are enable

PACKAGE INFORMATION

Title: **Package Outline for PDIP 32L(600MIL)**





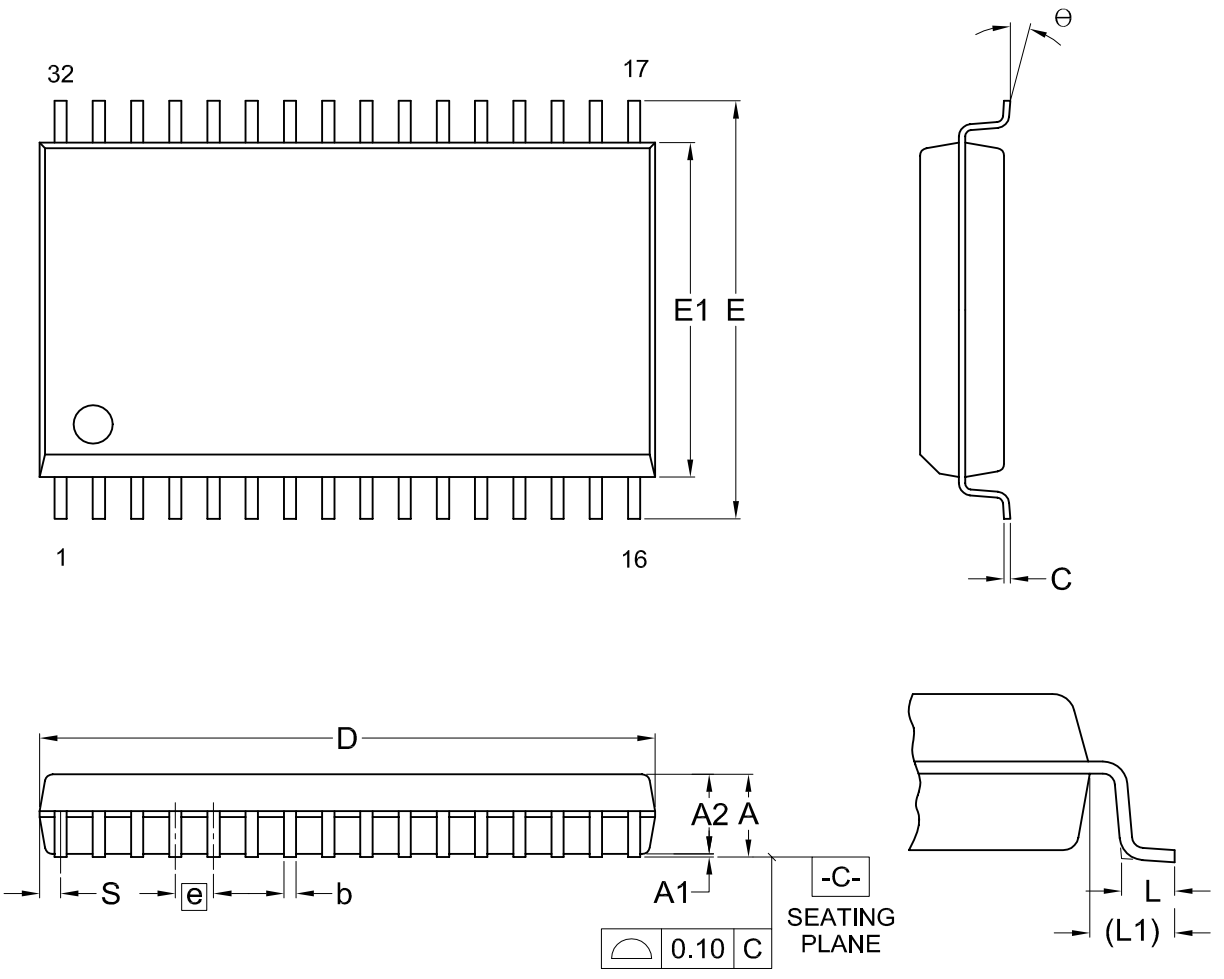


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	—	0.38	3.73	0.38	1.14	0.20	41.78	15.11	13.84		15.75	2.92	1.65
	Nom.	—	---	3.94	0.46	1.27	0.25	41.91	15.24	13.97	2.54	16.51	3.30	1.90
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	42.04	15.37	14.10		17.27	3.68	2.16
Inch	Min.	---	0.015	0.147	0.015	0.045	0.008	1.645	0.595	0.545		0.620	0.115	0.065
	Nom.	---	---	0.155	0.018	0.050	0.010	1.650	0.600	0.550	0.100	0.650	0.130	0.075
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	1.655	0.605	0.555		0.680	0.145	0.085

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.2	7				11-24-'03

Title: **Package Outline for SOP 32L (450MIL)**

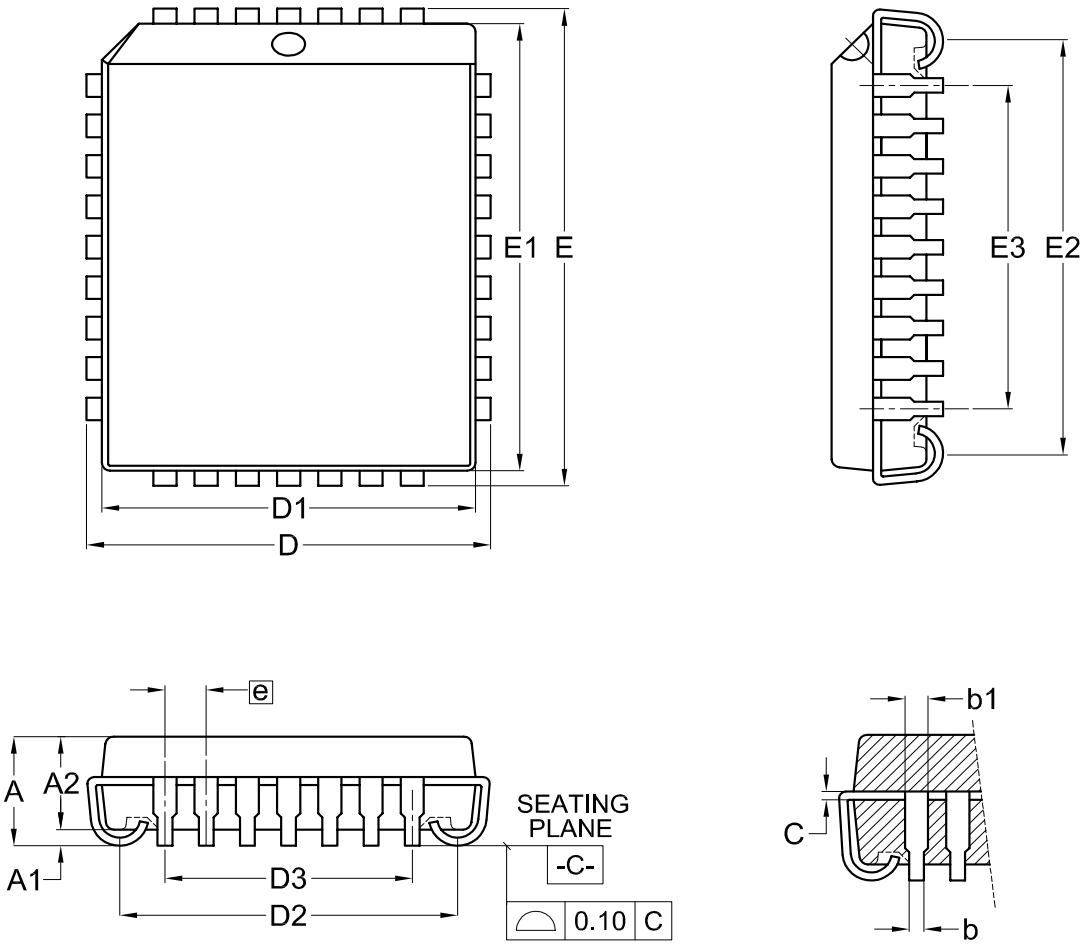


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	—	0.10	2.59	0.36	0.15	20.32	13.92	11.18		0.56	1.20	0.58	0
	Nom.	---	0.15	2.69	0.41	0.20	20.45	14.12	11.30	1.27	0.76	1.40	0.70	5
	Max.	3.00	0.20	2.80	0.51	0.25	20.57	14.32	11.43		0.96	1.60	0.83	8
Inch	Min.	---	0.004	0.102	0.014	0.006	0.800	0.548	0.440		0.022	0.047	0.023	0
	Nom.	–-	0.006	0.106	0.016	0.008	0.805	0.556	0.445	0.050	0.030	0.055	0.028	5
	Max.	0.118	0.008	0.110	0.020	0.010	0.810	0.564	0.450		0.038	0.063	0.033	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1404	5	MO-099			11-26-'03

Title: **Package Outline for 32L PLCC**

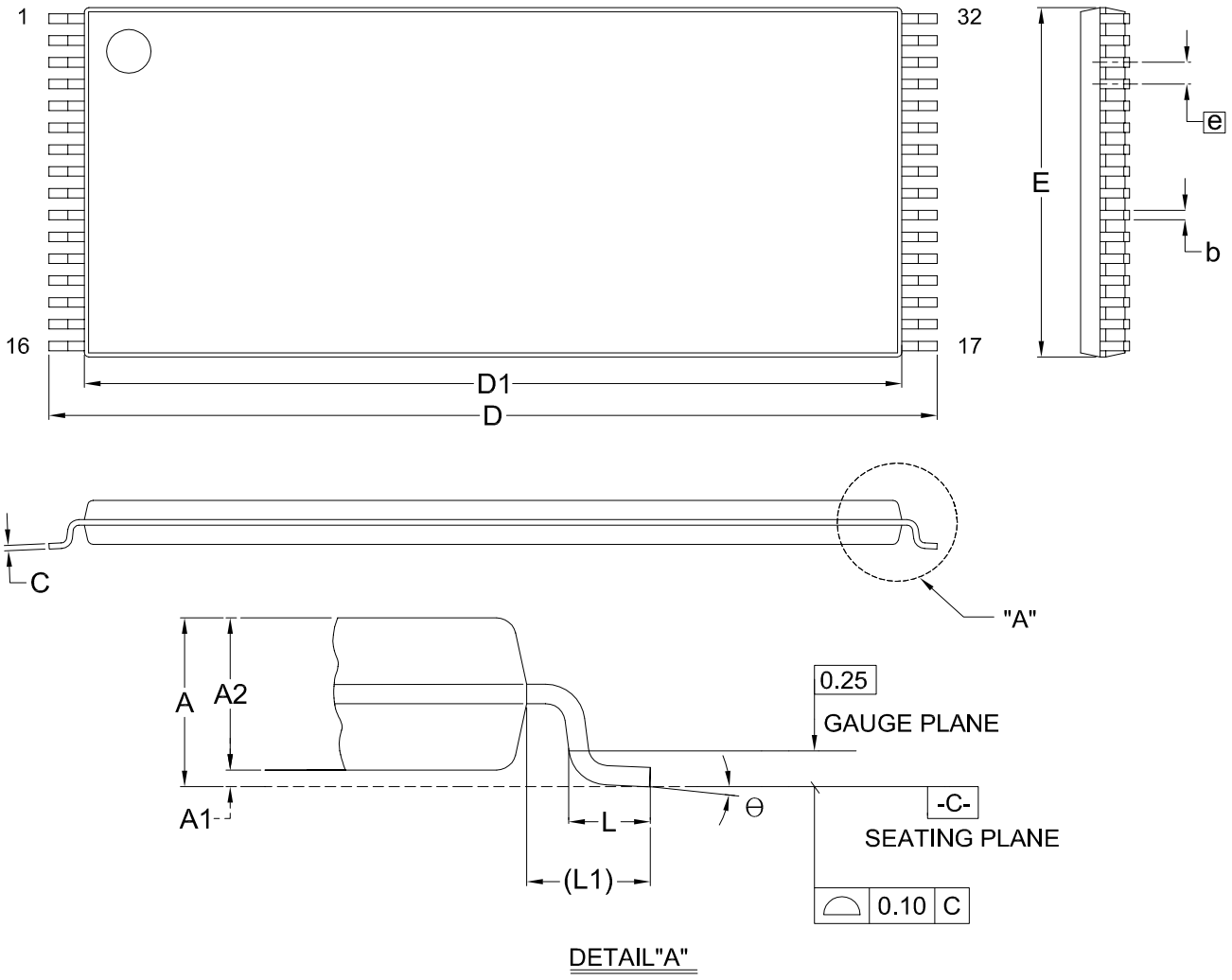


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	---	0.38	2.69	0.38	0.61	0.20	12.32	11.36	10.11		14.86	13.98	12.65		
	Nom.	---	0.58	2.79	0.46	0.71	0.25	12.45	11.43	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.81	2.89	0.54	0.81	0.30	12.58	11.50	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.447	0.398		0.585	0.550	0.498		
	Nom.	---	0.023	0.110	0.018	0.028	0.010	0.490	0.450	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.032	0.114	0.021	0.032	0.012	0.495	0.453	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	7	MS-016			12-10-'03

Title: **Package Outline for TSOP(I) 32L (8X20mm)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	9	MO-142			11-26-'03

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
3.7	AC Characteristics: tOH 10ns --> 0ns	P3	JAN/29/1999
3.8	Add 4000PC-90 32 pin PDIP	P1	JUN/02/1999
3.9	Modify DC Characteristics:ILI/ILO:5uA-->10uA;	P2	OCT/17/2000
	ISTB2:100mA-->100uA	P2	
4.0	Modify Package Information	P4~7	JUL/16/2001
4.1	Modify Package Information	P4~7	NOV/21/2001
4.2	Added "ABSOLUTE MAXIMUM RATINGS" note	P2	JUN/19/2003

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