512MB – 64Mx64 DDR2 SDRAM UNBUFFERED, SO-DIMM

FEATURES

- Unbuffered 200-pin, Small-Outline DIMM (SO-DIMM)
- Fast data transfer rates: PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 667*, 533 and 400 MT/s DDR2 SDRAM components
- V_{CC} = 1.8V ±0.1V
- V_{CCSPD} = 1.7V to 3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, and 5*
- Adjustable data-output drive strength
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Auto & self refresh (64ms: 8,192 cycle refresh)
- Gold edge contacts
- RoHS Compliant
- JEDEC Package option
  - 200 Pin (SO-DIMM)
  - PCB – 30.00mm (1.181") TYP.

DESCRIPTION

The WV3HG64M64EEU is a 64Mx64 Double Data Rate 2 SDRAM memory module based on 512Mb DDR2 SDRAM components. The module consists of eight 64Mx8, in FBGA package mounted on a 200 pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-5300*	PC2-4200	PC2-3200
Clock Speed	333MHz	266MHz	200MHz
CL-t_{RCD}-t_{RP}	5-5-5	4-4-4	3-3-3

Note:
- Consult factory for availability

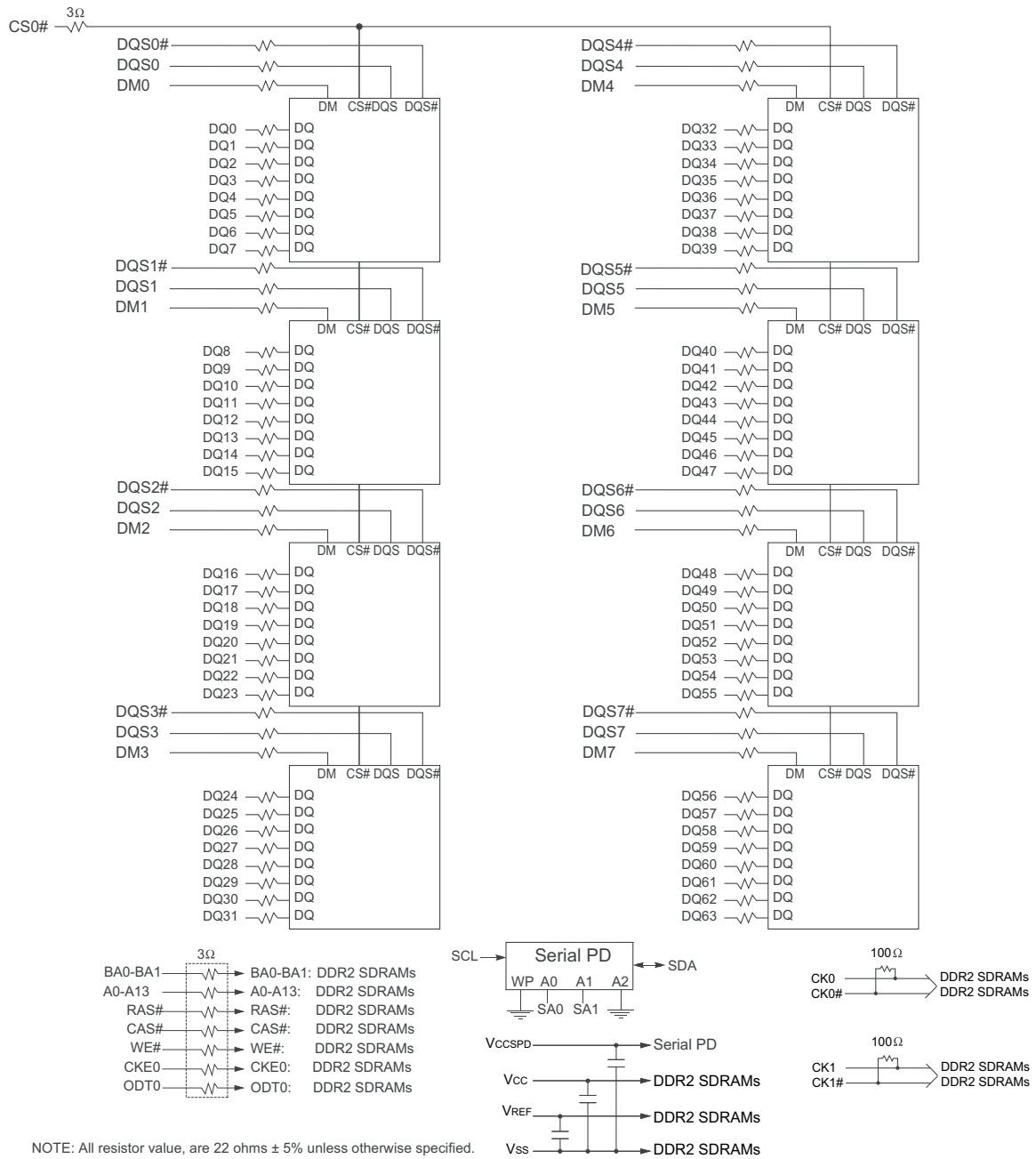
PIN CONFIGURATION

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VREF	51	DQS2	101	A1	151	DQ42
2	Vss	52	DM2	102	A0	152	DQ46
3	Vss	53	Vss	103	VCC	153	DQ43
4	DQ4	54	Vss	104	VCC	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	Vss
6	DQ5	56	DQ22	106	BA1	156	Vss
7	DQ1	57	DQ19	107	BA0	157	DQ48
8	Vss	58	DQ23	108	RAS#	158	DQ52
9	Vss	59	Vss	109	WE#	159	DQ49
10	DM0	60	Vss	110	CS0#	160	DQ53
11	DQS0#	61	DQ24	111	VCC	161	Vss
12	Vss	62	DQ28	112	VCC	162	Vss
13	DQS0	63	DQ25	113	CAS#	163	NC
14	DQ6	64	DQ29	114	ODT0	164	CK1
15	Vss	65	Vss	115	NC	165	Vss
16	DQ7	66	Vss	116	A13	166	CK1#
17	DQ2	67	DM3	117	VCC	167	DQS6#
18	Vss	68	DQS3#	118	VCC	168	Vss
19	DQ3	69	NC	119	NC	169	DQS6
20	DQ12	70	DQS3	120	NC	170	DM6
21	Vss	71	Vss	121	Vss	171	Vss
22	DQ13	72	Vss	122	Vss	172	Vss
23	DQ8	73	DQ26	123	DQ32	173	DQ50
24	Vss	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51
26	DM1	76	DQ31	126	DQ37	176	DQ55
27	Vss	77	Vss	127	Vss	177	Vss
28	Vss	78	Vss	128	Vss	178	Vss
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56
30	CK0	80	NC	130	DM4	180	DQ60
31	DQS1	81	VCC	131	DQS4	181	DQ57
32	CK0#	82	VCC	132	Vss	182	DQ61
33	Vss	83	NC	133	Vss	183	Vss
34	Vss	84	NC	134	DQ38	184	Vss
35	DQ10	85	NC	135	DQ34	185	DM7
36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	VCC	137	DQ35	187	Vss
38	DQ15	88	VCC	138	Vss	188	DQS7
39	Vss	89	A12	139	Vss	189	DQ58
40	Vss	90	A11	140	DQ44	190	Vss
41	Vss	91	A9	141	DQ40	191	DQ59
42	Vss	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	Vss
44	DQ20	94	A6	144	Vss	194	DQ63
45	DQ17	95	VCC	145	Vss	195	SDA
46	DQ21	96	VCC	146	DQS5#	196	Vss
47	Vss	97	A5	147	DM5	197	SCL
48	Vss	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	Vss	199	VCCSPD
50	NC	100	A2	150	Vss	200	SA1

PIN NAMES

SYMBOL	DESCRIPTION
A0-A13	Address input
ODT0	On-Die Termination
CK0, CK0#	Differential Clock Inputs
CK1, CK1#	Differential Clock inputs
CKE0	Clock Enable input
CS0#	Chip select
RAS#, CAS#, WE#	Command Inputs
BA0, BA1	Bank Address Inputs
DM0-DM7	Input Data Mask
DQ0-DQ63	Data Input/Output
DQS0-DQS7 DQS0#-DQS7#	Data Strobe
SCL	Serial Clock for Presence Detect
SA0-SA1	Presence Detect Address Inputs
SDA	Serial Presence Detect Data
V_{CC}	Power Supply
V_{REF}	Reference voltage
V_{SS}	Ground
V_{CCSPD}	Serial EEPROM Power Supply
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor value, are 22 ohms ± 5% unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Units
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	˚C
I_L	Input leakage current; Any input 0V<V_{IN}<V_{CC}; VREF iput 0V<V_{IN}<0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#	-80	80	uA
		CS#, CKE	-40	40	uA
		CK, CK#	-20	20	uA
		DM	-5	5	uA
I_{OZ}	Output leakage current; 0V<V_{IN}<V_{CC}; DQs and ODT are disable	DQ, DQS, DQS#	-5	5	uA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid VREF level		-16	16	uA

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Rating			Units	Notes
		Min.	Type	Max.		
Supply Voltage	V_{CC}	1.7	1.8	1.9	V	
I/O Reference Voltage	V_{REF}	0.49 x V_{CC}	0.50 x V_{CC}	0.51 x V_{CC}	V	1
I/O Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	2

Notes:

1. V_{REF} is expected to equal V_{CC}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on V_{REF} may not excedd +/-2 persent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
2. V_{TT} in sot applied directly to the device. V_{TT} is a system supply for signal terminaion resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A13, BA0~BA1, RAS#, CAS#, WE#)	C_{IN1}	12	20	pF
Input Capacitance CKE0, ODT	C_{IN2}	12	20	pF
Input Capacitance CS0#	C_{IN3}	12	20	pF
Input Capacitance (CK0, CK0#, CK1, CK1#)	C_{IN4}	8	12	pF
Input Capacitance (DM0 ~ DM7), (DQS0 ~ DQS7)	C_{IN5} (667)	6.5	7.5	pF
	C_{IN5} (533)	6.5	8	pF
Input Capacitance (DQ0 ~ DQ63)	C_{OUT1} (667)	6.5	7.5	pF
	C_{OUT1} (533)	6.5	8	pF

Notes:

- AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature	TOPER	0° to 85°	°C	1, 2

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measuremnet conditions, please refer to JEDED JESD51.2
2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.125	V_{CC} + 0.300	V
Input Low (Logic 0) Voltage	V_{IL}(DC)	-0.300	V_{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V_{IH}(DC)	V_{REF} + 0.250	-	V
Input Low (Logic 1) Voltage DDR2-667	V_{IH}(DC)	V_{REF} + 0.200	-	V
Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V_{IL}(DC)	-	V_{REF} - 0.250	V
Input Low (Logic 0) Voltage DDR2-667	V_{IL}(DC)	-	V_{REF} - 0.200	V

I_{CC} SPECIFICATION

Symbol	Proposed Conditions		665	534	403	Units
I_{CC0}*	Operating one bank active-precharge; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}$ min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		680	640	640	mA
I_{CC1}*	Operating one bank active-read-precharge; I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}$ (I_{CC}), $t_{RAS} = t_{RAS}$ min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address businputs are SWITCHING; Data pattern is same as I_{CC}4W		800	760	720	mA
I_{CC2P}**	Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		64	64	64	mA
I_{CC2Q}**	Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputsare STABLE; Data bus inputs are FLOATING		280	240	240	mA
I_{CC2N}**	Precharge standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING		320	280	280	mA
I_{CC3P}**	Active power-down current; All banks open; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	240	280	240	mA
		Slow PDN Exit MRS(12) = 1	96	96	96	mA
I_{CC3N}**	Active standby current; All banks open; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC}$, $t_{RAS} = t_{RAS}$ min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		440	400	400	mA
I_{CC4W}*	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}$max(I_{CC}), $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1120	960	880	mA
I_{CC4R}*	Operating burst read current; All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}$max(I_{CC}), $t_{RP} = t_{RP}(I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W		1160	1000	880	mA
I_{CC5}**	Burst auto refresh current; $t_{CK} = t_{CK}(I_{CC})$; Refresh command at every $t_{RFC}(I_{CC})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1200	1120	1120	mA
I_{CC6}**	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs vre FLOATING; Data bus inputs are FLOATING	Normal	64	64	64	mA
I_{CC7}*	Operating bank interleave read current; All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{DD}), AL = t_{RC}D(I_{CC})-1*t_{CK}(I_{CC}); $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RRD} = t_{RRD}(I_{CC})$, t_{RCD} = 1*t_{CK}(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.		1760	1760	1760	mA

I_{CC} specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Note:

*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

**: Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS				665		534		403		
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
		CL = 5	$t_{CK\ (5)}$	3,000	8,000					ps
		CL = 4	$t_{CK\ (4)}$	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	$t_{CK\ (3)}$	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	Half clock period		t_{HP}	MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		ps
	Clock jitter		t_{JIT}	250		250		250		ps
Data	DQ output access time from CK/CK#		t_{AC}	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t_{HZ}		t_{AC} MAX		t_{AC} MAX		t_{AC} MAX	ps
	Data-out low-impedance window from CK/CK#		t_{LZ}	t_{AC} MIN	t_{AC} MAX	t_{AC} MIN	t_{AC} MAX	t_{AC} MIN	t_{AC} MAX	ps
	DQ and DM input setup time relative to DQS		t_{DS}	100		100		150		ps
	DQ and DM input hold time relative to DQS		t_{DH}	225		225		275		ps
	DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		0.35		t_{CK}
	Data hold skew factor		t_{QHS}		340		400		450	ps
	DQ…DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ps
	Data valid output window (DVW)		t_{DVW}	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
Data Strobe	DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35		t_{CK}
	DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35		t_{CK}
	DQS output access time from CK/CK#		t_{DQSCK}	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising … setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}
	DQS falling edge from CK rising … hold time		t_{DSH}	0.2		0.2		0.2		t_{CK}
	DQS…DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		240		300		350	ps
	DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
	DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	DQS write preamble setup time		t_{WPRES}	0		0		0		p s
	DQS write preamble		t_{WPRE}	0.35		0.35		0.35		t_{CK}
	DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	Write command to first DQS latching transition		t_{DQSS}	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t_{CK}
	Address and control input pulse width for each input		t_{IPW}	0.6		0.6		0.6		t_{CK}
	Address and control input setup time		t_{IS}	200		250		350		ps
	Address and control input hold time		t_{IH}	275		375		475		ps
	Address and control input hold time		t_{CCD}	2		2		2		t_{CK}

Note:
AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.
Continued on next page

AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			665		534		403		
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t_{RC}	55		60		65		ns
	ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t_{RCD}	15		15		15		ns
	Four Bank Activate period	t_{FAW}	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	t_{RTP}	7.5		7.5		7.5		ns
	Write recovery time	t_{WR}	15		15		15		ns
	Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns
	Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		10		ns
	PRECHARGE command period	t_{RP}	15		15		15		ns
	PRECHARGE ALL command period	t_{RPA}	$t_{RP}+t_{CK}$		$t_{RP}+t_{CK}$		$t_{RP}+t_{CK}$		ns
	LOAD MODE command cycle time	t_{MRD}	2		2		2		t_{CK}
	CKE low to CK,CK# uncertainty	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		ns
Self Refresh	REFRESH to Active of Refresh to Refresh command interfal	t_{RFC}	105	70,000	105	70,000	105	70,000	ns
	Average periodic refresh interval	t_{REF}I		7.8		7.8		7.8	µs
	Exit self refresh to non-READ command	t_{XSNR}	t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		ns
	Exit self refresh to READ command	t_{XSRD}	200		200		200		t_{CK}
	Exit self refresh timing reference	t_{ISXR}	t_{IS}		t_{IS}		t_{IS}		ps
ODT	ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	t_{CK}
	ODT turn-on	t_{AON}	t_{AC} (MIN)	t_{AC} (MAX) + 1000	t_{AC} (MIN)	t_{AC} (MAX) + 1000	t_{AC} (MIN)	t_{AC} (MAX) + 1000	ps
	ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
	ODT turn-off	t_{AOF}	t_{AC} (MIN)	t_{AC} (MAX) + 600	t_{AC} (MIN)	t_{AC} (MAX) + 600	t_{AC} (MIN)	t_{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t_{AONPD}	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t_{ANPD}	3		3		3		t_{CK}
	ODT power-down exit latency	t_{AXPD}	8		8		8		t_{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2		2		2		t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	7 - AL		6 - AL		6 - AL		t_{CK}
	A Exit precharge power-down to any non-READ command.	t_{XP}	2		2		2		t_{CK}
	CKE minimum high/low time	t_{CKE}	3		3		3		t_{CK}

Note:
AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

ORDERING INFORMATION FOR D4

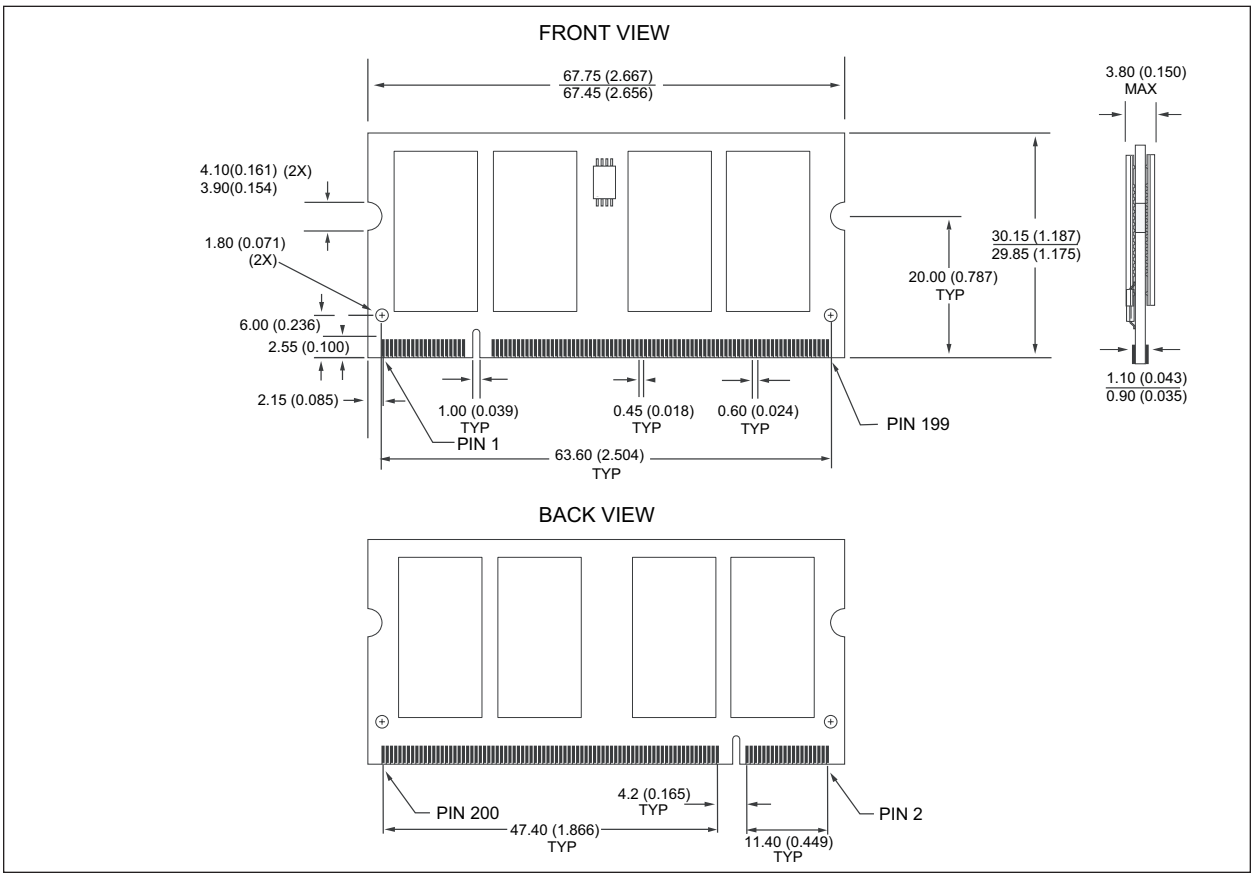
Part Number	Clock/Data Rate Frequency	CAS Latency	t_{RCD}	t_{RP}	Height**
WV3HG64M64EEU665D4xxG*	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG64M64EEU534D4xxG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG64M64EEU403D4xxG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

* Consult Factory for availability

NOTES:

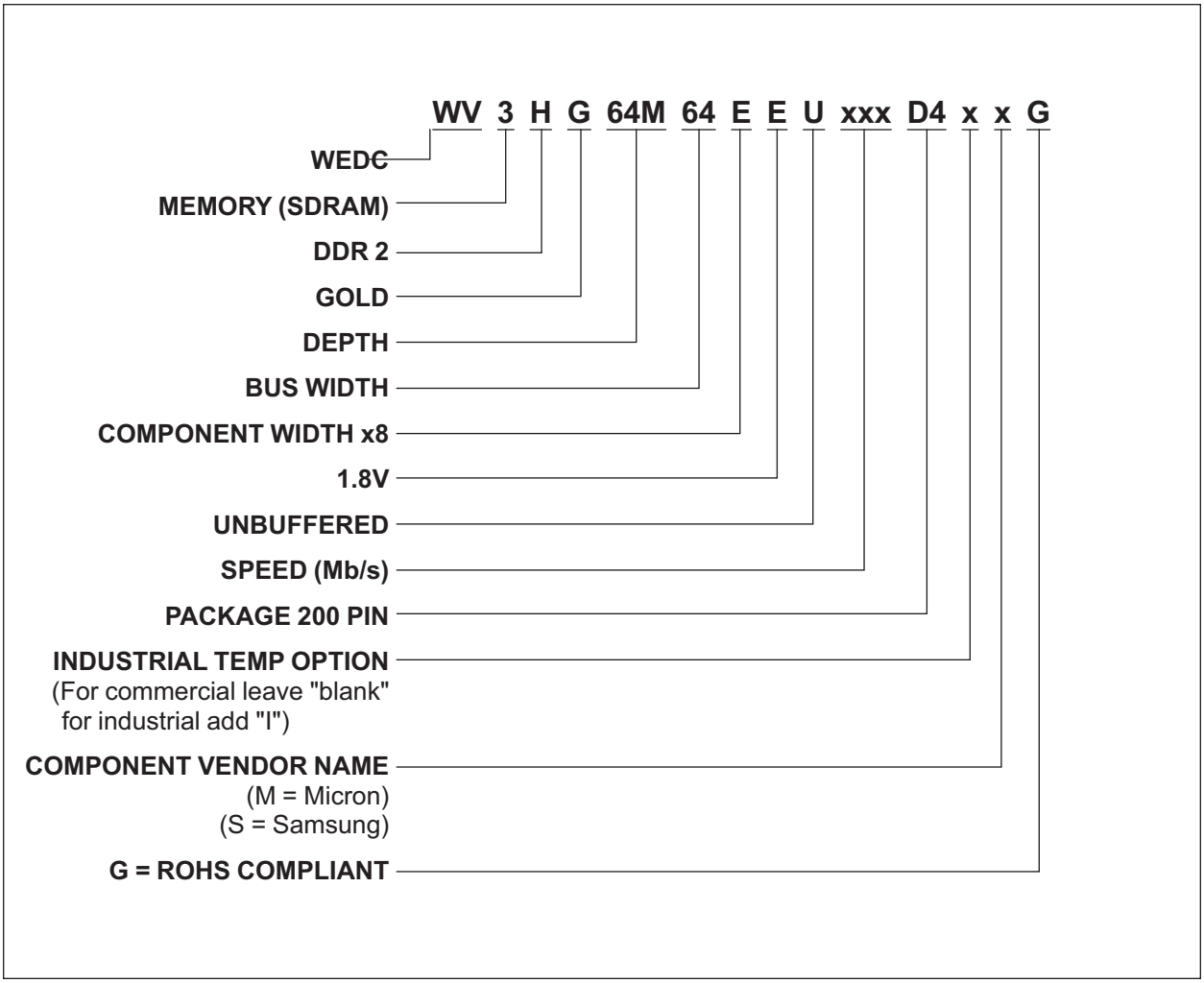
- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D4



** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

512MB – 64Mx64 DDR2 SDRAM UNBUFFERED

DRAM DIE OPTIONS:

- SAMSUNG: C-Die, will move to E-Die Q2'06
- MICRON: U37Y: B-Die

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	January 2006	Advanced
Rev 1	1.0 Updated Vcc spec	Feburary 2006	Advanced
Rev 2	2.1 Updated AC specs 2.2 Updated ordering information 2.3 Added industrial temp option on part numbering guide 2.4 Added die rev info	May 2006	Advanced