

NUD4301

Advance Information Dual Channel LED Driver/Current Source

This device is designed to replace switching regulators for driving LEDs in low voltage DC applications (up to 6 V). Its unique integrated circuit design provides the ability to drive external FETs to achieve higher voltage and current capabilities for different application needs (see Figure 8). An external resistor allows the circuit designer to set the LED current for different applications needs. The device is packaged in a small surface mount leadless package (DFN8), which results in a significant reduction of both system cost and board space.

Features

- Low Dropout Voltage < 300 mV
- Programmable Output Current from 1 mA to 30 mA
- Dual Output with Independent Current Limit Set
- DC Current in LED
- Analog/Digital PWM Capability
- This is a Pb-Free Device

Typical Applications

- Portables: PDAs, Cell phones
- LCD Backlighting Applications

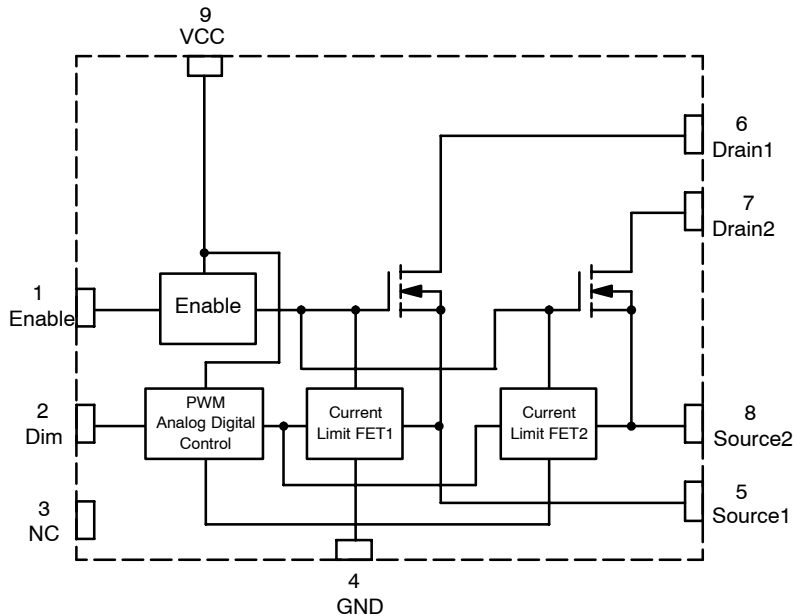
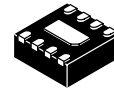


Figure 1. Block Diagram



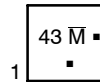
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DFN8
CASE 506AQ

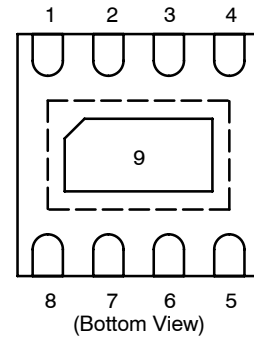
MARKING DIAGRAM



- 43 = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION



ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|-------------------|------------------|
| NUD4301MNT1G | DFN8 (Pb-Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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FUNCTIONAL PIN DESCRIPTIONS

| Pin | Function | Description |
|-----|----------|--|
| 1 | Enable | The device is enabled with a positive voltage signal at this pin. The enable controls both channels. |
| 2 | Dim | This pin is used for analog or PWM dimming control. An analog signal of 0 – 3.3 volts is required, or a PWM signal with an amplitude greater than 3.3 volts. The dim controls both channels. |
| 3 | NC | No connection. |
| 4 | GND | Ground Reference to the device. |
| 5 | Source1 | Source terminal of the FET 1 |
| 6 | Drain1 | Drain terminal of the FET 1, which is also the switching node of the load 1. |
| 7 | Drain2 | Drain terminal of the FET 2, which is also the switching node of the load 2. |
| 8 | Source2 | Source terminal of the FET 2 |
| 9 | VCC | Input voltage to the LED driver. This voltage is compatible with any battery based systems of up to 6 V. |

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|-------------|------------------------|-------------|
| Input Voltage, Operating Steady State (V_{CC} to GND) Transient (1 ms) | V_{CC} | -0.3 to 6 -0.3 to 7 | V |
| Drain Voltage, Operating Steady State (Drain-to-Source) Transient (1 ms) | V_{DS} | -0.3 to 6 -0.3 to 7 | V |
| Enable Voltage, Operating Steady State | V_{EN} | -0.3 to 6 | V |
| Dim Voltage, Operating Steady State | V_{dim} | -0.3 to 3.6 | V |
| Drain Current, Peak | I_{Dpk} | 100 | mA |
| Drain Current, Continuous | $I_{D(av)}$ | 30 | mA |
| Thermal Resistance, Junction-to-Air (Note 1) | Q_{JA} | 365 | °C/W |
| Power Dissipation @ $T_A = 25^{\circ}C$ (Note 1) Derating above 25°C | P_{max} | 340 2.7 | mW mW/°C |
| Operating Temperature Range | T_J | -40 to 150 | °C |
| Non-Operating Temperature Range | T_J | -55 to 175 | °C |
| Maximum Lead Temperature for Soldering Purposes (1.8" from case for 10 s) | T_L | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Mounted onto minimum pad board.

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ELECTRICAL CHARACTERISTICS (Unless otherwise noted: $V_{CC} = 3.6\text{ V}$, $R_{\text{sense}} = 4.7\ \Omega$, 1%, $T_A = 25^\circ\text{C}$ for typical values, For min/max values T_J is the applicable junction temperature)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|--|---------------------|-----|-----|-----|---------------|
| Power FET (Each Channel) | | | | | |
| ON Resistance ($V_{CC} = 3.6\text{ V}$, $I_D = 10\text{ mA}$, $R_{\text{sense}} = 4.7\ \Omega$, $V_{\text{dim}} = 3.3\text{ V}$) | R_{DSon} | – | 5.0 | 5.5 | Ω |
| Zero Enable Voltage Drain Current ($V_{\text{DS}} = 6\text{ V}$, $V_{\text{Enable}} = 0\text{ V}$) | I_{DSS} | – | 10 | 100 | nA |
| Drain-to-Source Sustaining Voltage ($I_D = 100\ \mu\text{A}$) | V_{BRDSS} | 7.0 | – | – | V |
| Output Capacitance ($V_{\text{DS}} = 6\text{ V}$, $V_{\text{Enable}} = 0\text{ V}$, $f = 1\text{ kHz}$) | | – | 100 | – | pF |
| Voltage Drop (Note 2) ($V_{CC} = 3.6\text{ V}$, $V_{\text{LED}} = 3.3\text{ V}$, $I_D = 20\text{ mA}$, $R_{\text{sense}} = 4.7\ \Omega$, $V_{\text{dim}} = 3.3\text{ V}$) | V_{drop} | – | – | 300 | mV |
| Current Regulation Circuit (Each Channel) | | | | | |
| Output Current Regulation ($V_{CC} = 3.6\text{ V}$, $V_{\text{LED}} = 3.3\text{ V}$, $R_{\text{sense}} = 4.7\ \Omega$, $V_{\text{dim}} = 3.3\text{ V}$) | I_{out} | 19 | 20 | 21 | mA |
| Enable | | | | | |
| Logic Level High (Unit Operational) | V_{ENhigh} | 1.7 | – | – | V |
| Logic Level Low (Unit Shutdown) | V_{ENlow} | – | – | 0.7 | V |
| Dim | | | | | |
| Off Voltage (Zero Output Current), $I_D = 20\ \mu\text{A}$, $R_{\text{sense}} = 4.7\ \Omega$ | V_{zero} | – | – | 50 | mV |
| On Voltage (Max Output Current), $I_D = I_{\text{out}}$, $R_{\text{sense}} = 4.7\ \Omega$ | V_{max} | 3.1 | 3.3 | 3.6 | V |
| Max PWM Frequency | f_{max} | – | 10 | – | kHz |
| Bias Supply (Complete Device) | | | | | |
| Bias Current ($V_{CC} = 3.6\text{ V}$, Device Non-Operational, $V_{\text{Enable}} = 0\text{ V}$) | I_{BIAS1} | – | 10 | 100 | nA |
| Bias Current ($V_{CC} = 3.6\text{ V}$, Device Operational, $V_{\text{Enable}} = V_{CC}$) | I_{BIAS2} | – | 100 | 200 | μA |

2. $V_{\text{drop}} = V_{\text{DS}} + V_{\text{Rsense}}$

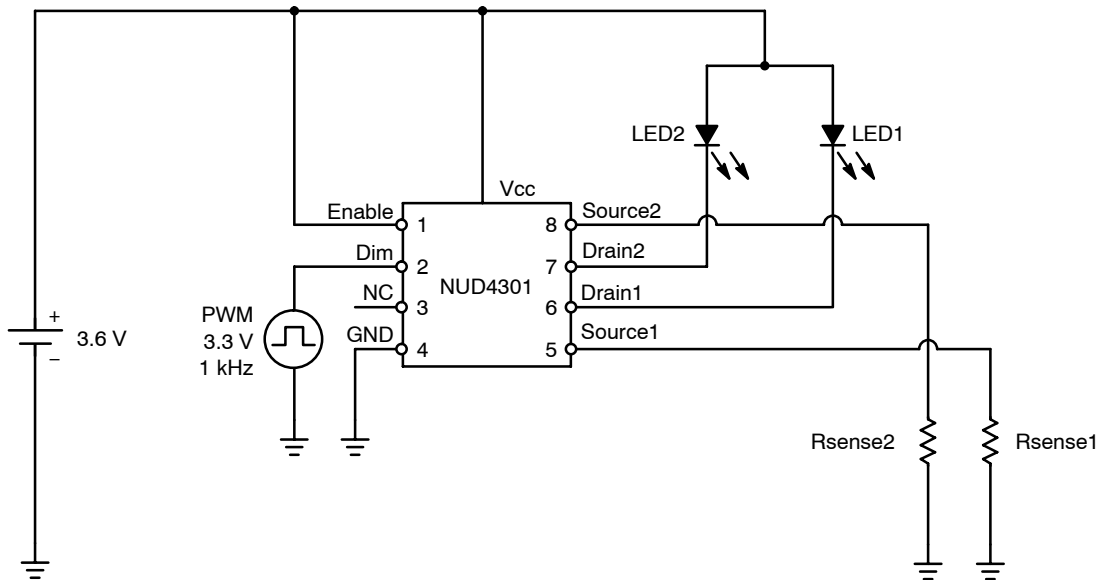


Figure 2. Typical Low Voltage Application Circuit

TYPICAL PERFORMANCE CURVES

($T_A = 25^\circ\text{C}$, unless otherwise noted)

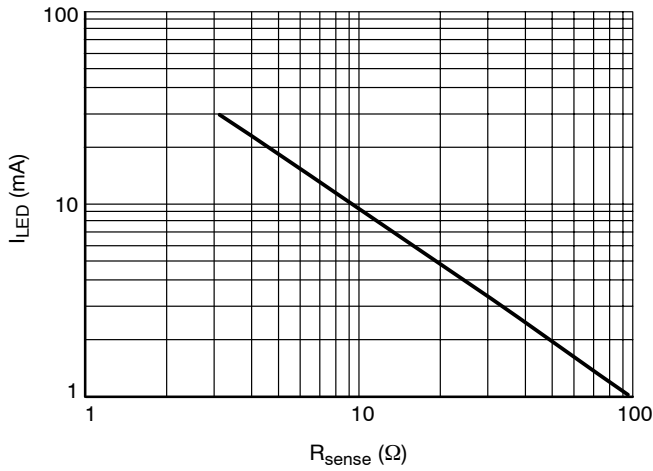


Figure 3. Current Limit Adjustment

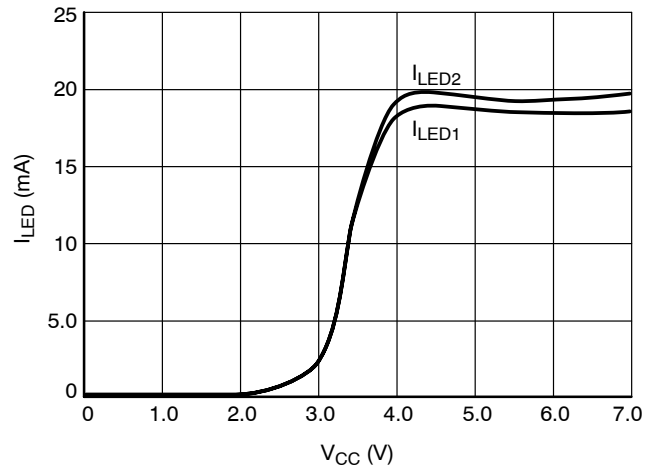


Figure 4. Typical Line Regulation Performance
($V_{LED} = 3.4\text{ V}$, $R_{sense} = 4.7\ \Omega$)

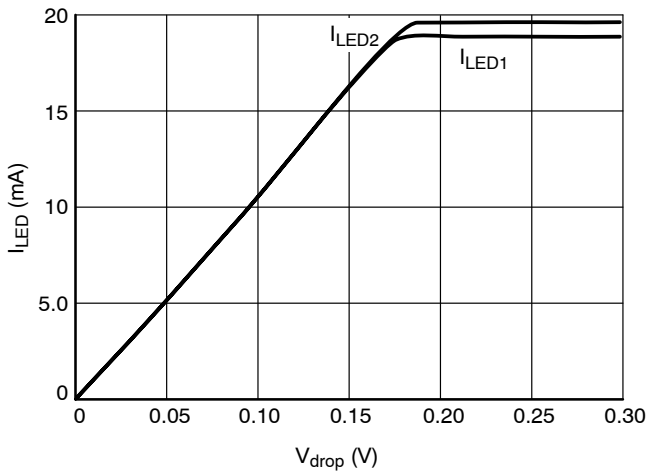


Figure 5. Typical Current Regulation vs. V_{drop}
($V_{drop} = V_{DS} + V_{Rsense}$)

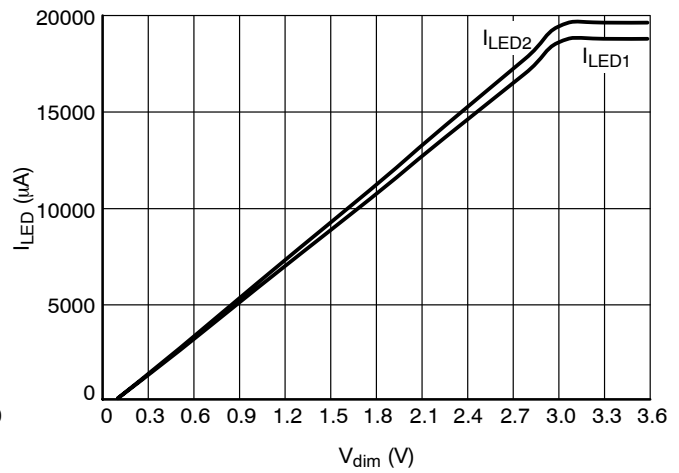


Figure 6. Typical Current Regulation vs. V_{dim}
($V_{LED} = 3.4\text{ V}$, $R_{sense} = 4.7\ \Omega$)

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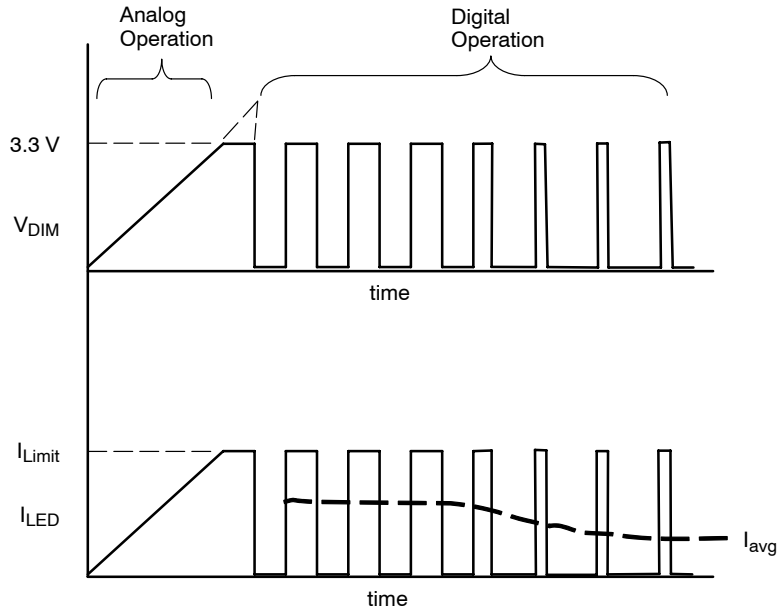


Figure 7. Dimming Operation Curves
(Graph obtained from SPICE simulations)

Theory of Operation

This device contains two LED current sources. Each channel is comprised of a lateral N-channel FET controlled by a current limit circuit that senses the voltage drop across the R_{sense} resistor and compares it with an internal voltage reference to provide the current regulation. For dimming applications, the current limit circuit operates in combination with the PWM signal applied to the dim pin of the device for control purposes.

Current Limit and PWM Circuits

With a DC voltage of 3.3 V applied to the Dim pin of the device, the internal reference voltage of the current limit circuit is set to 94 mV. The R_{sense} resistor is then selected through a very simple formula: $R_{sense} = 94 \text{ mV} / I_{LED}$. This allows the user to set different LED currents (between 1 mA and 30 mA).

For dimming control, a PWM signal may be applied to the dim pin of the device. This PWM signal can be used to perform digital dimming.

For digital dimming, the amplitude of the PWM signal must be 3.3 V or higher. The LED current will be proportional to the duty cycle of the PWM signal.

For analog dimming, the input signal to the Dim pin must be between 0 V and 3.3 V. The resulting output current will be given by the following formula:

$$I_{LED} = \frac{(V_{dim}/35)}{R_{sense}}$$

If a PWM signal is beyond the input frequency range for the Dim pin, a RC filter may be used to convert it to an analog signal.

The RC filter generates an analog voltage signal, which is proportional to the duty cycle of the PWM signal applied. This analog signal is then used as the new reference voltage for the current limit circuit, which compares it with the voltage signal generated across R_{sense} to provide the current regulation.

Enable

The enable circuit turns the device on when a positive signal is applied to the enable pin. The circuit is designed to allow low current consumption (0.1 μA typical) when the device is disabled.

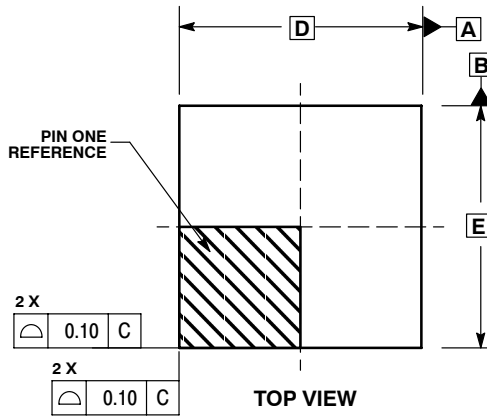
LCD Backlighting Applications

The voltage and current capability of the NUD4301 device can be increased by using external FETs so that the circuit can be used in high voltage backlighting applications such as TV. Figure 8 shows the schematic diagram of this concept.

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PACKAGE DIMENSIONS

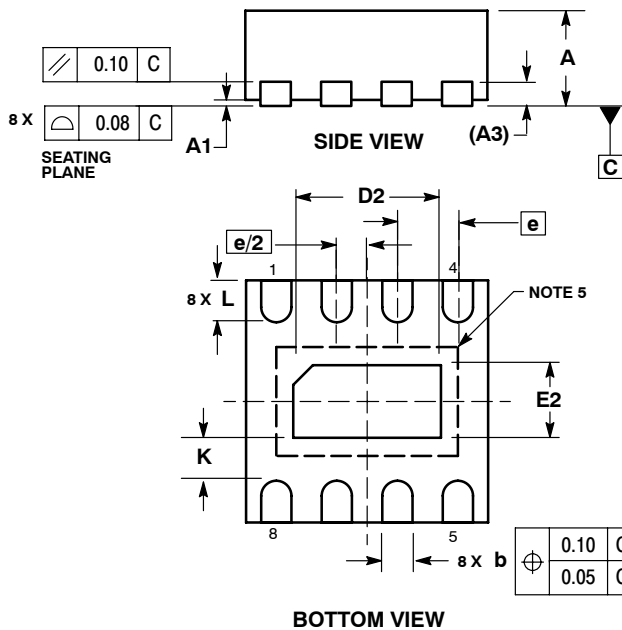
DFN8
CASE 506AQ-01
ISSUE A



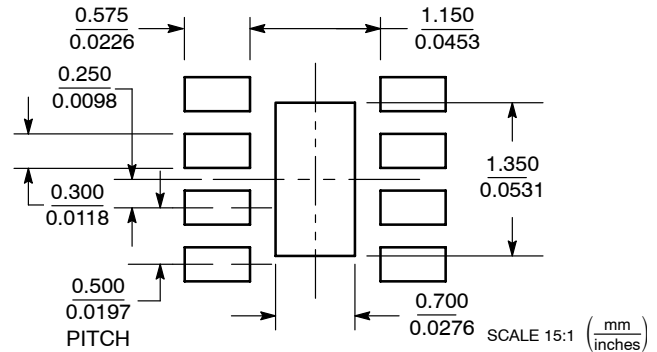
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. INTERNAL PAD SIZE: 1.5 X 0.9 MM.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.20 | 0.30 |
| D | 2.00 | BSC |
| D2 | 1.10 | 1.30 |
| E | 2.00 | BSC |
| E2 | 0.50 | 0.70 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.25 | 0.45 |



SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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