



3.3V DUAL DIFFERENTIAL LVPECL-to-LVTTL TRANSLATOR

Precision Edge®
SY89223L

FEATURES

- $f_{MAX} > 160\text{MHz}$
- $3.3\text{V} \pm 10\%$ power supply
- $< 2.5\text{ns}$ propagation delay
- $< 300\text{ps}$ within-device skew
- Differential LVPECL inputs
- 24mA LVTTL outputs
- Industrial temperature range: -40°C to $+85^{\circ}\text{C}$
- Available in an ultra-small 8-pin (2mm x 2mm) MLF™ package



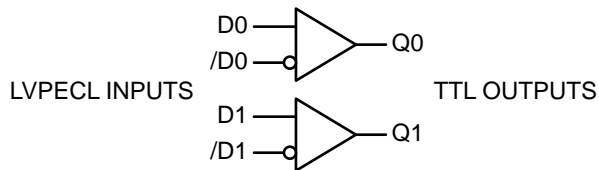
Precision Edge®

DESCRIPTION

The SY89223L is a 3.3V, precision dual differential LVPECL-to-LVTTL translator. The ultra-small 8-pin MLF package and the low skew, dual gate design of this translator makes it ideal for applications which require the translation of a clock and a data signal.

The SY89223L translator accepts 10k or 100k differential LVPECL inputs.

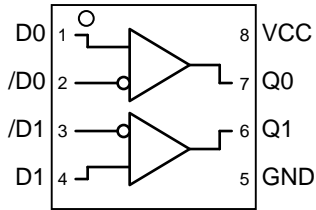
BLOCK DIAGRAM



FUNCTIONAL CROSS REFERENCE

Micrel Part Number	Functional Cross
SY89223L	10/100ELT23

PACKAGE/ORDERING INFORMATION



**8-Pin MLF™
Ultra-Small Outline**

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89223LMITR ⁽²⁾	MLF-8	Industrial	223	Sn-P
SY89223LMGTR ⁽²⁾	MLF-8	Industrial	223 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1, 2, 3, 4	D0, /D0 D1, /D1	10k/100k PECL Input	Differential LVPECL Input: Channels 0 and 1 inputs are applied to these LVPECL compatible inputs. See "Input Interface Applications" section for single-ended inputs.
7, 6	Q0, Q1	LVTTL Output	Single-ended Output: LVTTL outputs.
8	VCC	VCC Power	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.
5	GND, Exposed Pad	Ground	Ground and exposed pad must be tied to ground plane.

Absolute Maximum Ratings^(Note 1)

Power Supply Voltage (V_{CC})	-0.5V to 4.0V
PECL Input Voltage (V_{IN})	+0V to $V_{CC} + 0.5V$
Voltage Applied to Output at HIGH State (V_{OUT})	-0.5V to V_{CC}
Current Applied to Output at LOW State (I_{OUT})	Twice the Rated I_{OL} mA
Lead Temperature (soldering, 20 sec.)	260°C
Storage Temperature (T_S)	-65°C to +150°C

Operating Ratings^(Note 2)

Power Supply Voltage (V_{CC})	+3.0V to +3.6V
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance, ^(Note 3)	
MLF™ (θ_{JA})	
Still-Air	93°C/W
500lfpm	87°C/W
MLF™ (ψ_{JB})	56°C/W

LV TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V \pm 10\%$; GND = 0V, $T_A = -40^\circ C$ to $+85^\circ C$; unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.0mA$	2.0			V
V_{OL}	Output LOW Voltage	$I_{OL} = 24mA$			0.5	V
I_{CC}	Power Supply Current				30	mA
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$	-80		-240	mA

LV PECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V \pm 10\%$; GND = 0V, $T_A = -40^\circ C$ to $+85^\circ C$; unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		$V_{CC} - 1.165$	—	$V_{CC} - 0.880$	V
V_{IL}	Input LOW Voltage		$V_{CC} - 1.810$	—	$V_{CC} - 1.475$	V
V_{IHCMR}	Input HIGH Common Mode Range	Note 4	1.2	—	V_{CC}	V
V_{PP}	Minimum Input Swing		200	—	—	mV
I_{IH}	Input HIGH Current		—	—	150	μA
I_{IL}	Input LOW Current		0.5	—	—	μA

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

Note 4. $V_{IHCMR}(\min)$ varies 1:1 with V_{EE} , Max varies 1:1 with V_{CC} .

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V \pm 10\%$; $GND = 0V$, $T_A = -40^\circ C$ to $+85^\circ C$; $C_L = 20pF$ unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Input Frequency	Note 5	160			MHz
t_{pd}	Propagation Delay		1.5		2.5	ns
t_{SKEW++}	Within-Device Skew	Notes 6, 8			0.3	ns
t_{SKEW--}	Within-Device Skew	Notes 7, 8			0.3	ns
t_{SKPP}	Part-to-Part Skew	Notes 8, 9			0.5	ns
t_r, t_f	Output Rise/Fall Times (1.0V to 2.0V)		0.5		1.0	ns

- Note 5.** Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
- Note 6.** Within-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.
- Note 7.** Within-Device Skew considering LOW-to-LOW transitions at common V_{CC} level.
- Note 8.** All skew parameters are guaranteed but not tested.
- Note 9.** Device-to-Device Skew considering HIGH-to-HIGH transitions at common V_{CC} level.

INPUT INTERFACE APPLICATIONS

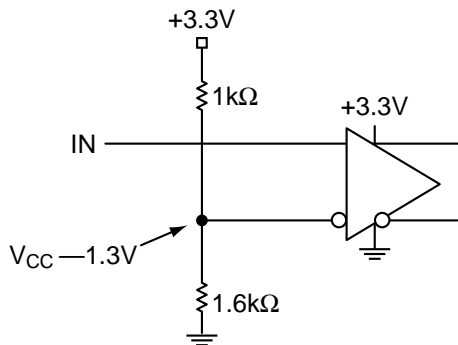


Figure 1a. Single-Ended Input (Terminating Unused Input)

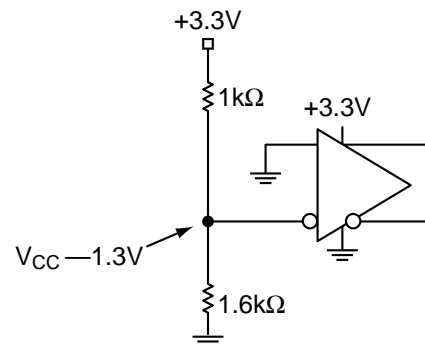
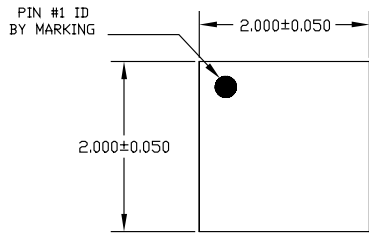


Figure 1b. Terminating Inputs of Unused Gate

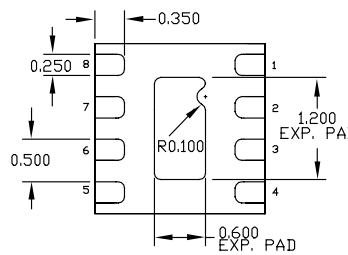
RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89206/216V	3.3V/5V 1GHz Differential PECL/ECL Receiver/Buffer	www.micrel.com/product-info/products/sy89206-216v.shtml
SY89306/316V	3.3V/5V 2.5GHz PECL/ECL Differential Receiver/Buffer	www.micrel.com/product-info/products/sy89306-316v.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

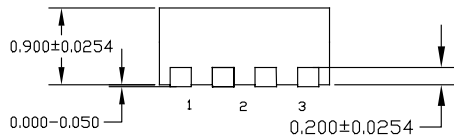
8 LEAD ULTRA-SMALL EPAD-MicroLeadFrame™ (MLF-8)



TOP VIEW

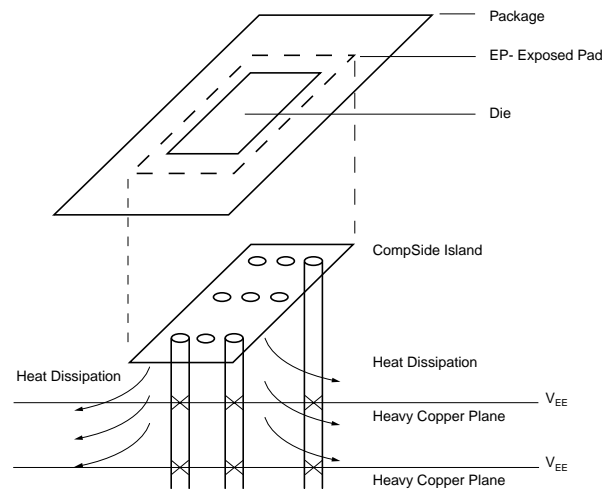


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 8-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)**

Package Notes:

- Note 1.** Package meets level two qualification.
- Note 2.** All parts are dry-packaged before shipment.
- Note 3.** Exposed pads must be soldered to a ground plane, of the same potential as the device GND pin, for proper thermal management.

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