STRUCTURE Silicon Monolithic Integrated Circuit
TYPE 1ch Series Regulator Driver IC
PRODUCT SERIES **BD3507HFV**
FEATURES
- Built-in high-accuracy buffer circuit
- Adoption of ceramic capacitors
- Built in Super low ON resistance (300mΩ typ) Nch PowerMOSFET

○ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limit	Unit
Supply Voltage 1	Vcc	6.0 *1 *2	V
Supply Voltage 2	V_{IN}	6.0 *1 *2	V
Enable Input Voltage	V_{EN}	6.0 *1 *2	V
Power dissipation 1	Pd1	512.5 *3	mW
Power dissipation 2	Pd2	850.0 *4	mW
Operating temperature range	Topr	−10～+100	°C
Storage temperature range	Tstg	−55～+150	°C
Junction Temperature	Tjmax	+150	°C

*1 Not to exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Reduced by 4.1mW for each increase in Ta of 1°C over 25°C
*4 Ta≧25°C (When mounted on board 70mm x 70mm x 1.6mm Glass-epoxy PCB which has 2 layers (100m^2) of copper on the back side) 6.8mW/°C increase.

○ RECOMMENDED OPERATING CONDITIONS (Ta=25°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage 1	V_{CC}	4.5	5.5	V
Supply Voltage 2	V_{IN}	1.2	Vcc−1	V
VREF Setup Voltage	V_{REF}	0.65	2.7	V
Enable Input Voltage	V_{EN}	-0.3	5.5	V
Output Current	I_O	0	550	mA

★ This product is not designed for protection against radioactive rays.

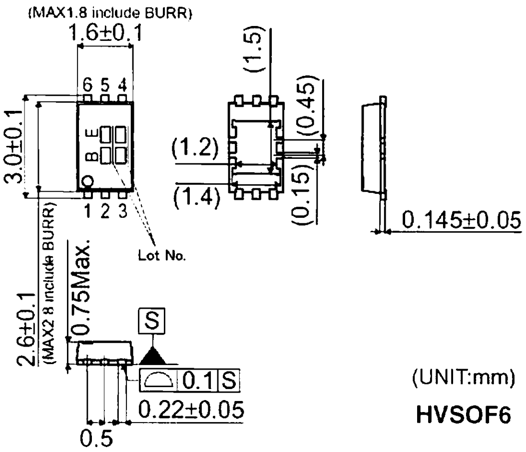
Status of this document
The Japanese version of this document is the official specification.
This translated version is intended only as a reference, to aid in understanding the official version.
If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

○ ELECTRICAL CHARACTERISTICS (unless otherwise noted,Ta=25℃ V_{CC}=5V V_{IN}=1.8V V_{REF}=1.2V V_{EN}=3V)

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
Bias current	I_{CC}	-	0.4	0.7	mA	
Shut-Down Mode Current 1	I_{STB}	-	0	10	μA	V_{EN}=0V
Shut-Down Mode Current 2	I_{INSTB}	-	0	10	μA	V_{EN} =0V
Output Voltage 1	Vo1	1.188	1.200	1.212	V	Io=0mA
Output Voltage 2	Vo2	1.188	1.200	1.212	V	Io=300mA
Output Voltage 3	Vo3	1.176	1.200	1.224	V	Io=0mA to 550mA V_{CC}=4.5V to 5.5V Ta=-10℃ to 100℃ *5
Output Voltage 4	Vo4	2.475	2.500	2.525	V	V_{IN} =3.3V,V_{REF}=2.5V Io=0mA
Output Voltage 5	Vo5	2.475	2.500	2.525	V	V_{IN} =3.3V, V_{REF} =2.5V Io=300mA
Output Voltage 6	Vo6	2.450	2.500	2.550	V	V_{IN} =3.3V, V_{REF} =2.5V Io=0mA to 550mA V_{CC} =4.5V to 5.5V Ta=-10℃ to 100℃ *5
Over Current Protect	I_{CL}	600	-	-	mA	
Output ON Resistance	R_{ON}	-	300	550	mΩ	
High level Enable Input Voltage	EN_{HIGH}	2.0	-	-	V	EN:Sweep-up
Low level Enable Input Voltage	EN_{LOW}	-0.2	-	0.8	V	EN:Sweep-down
Enable pin Input Current	I_{EN}	-	7	10	μA	V_{EN} =3V
VCC UVLO	V_{UVLO}	3.5	3.8	4.1	V	V_{CC}:Sweep-up
VCC UVLO Hysterisis	V_{HYS}	100	160	220	mV	V_{CC}:Sweep-down
V_{REF} Pin Bias Current	I_{VREF}	-0.1	-	0.1	μA	V_{REF} =0→2.7 V *5
V_{REF} Discharge ON Voltage	R_{ONREF}	-	1.0	2.0	kΩ	
Output Discharge ON Voltage	R_{ONDIS}	-	0.1	0.3	kΩ	

*5 Design Guarantee

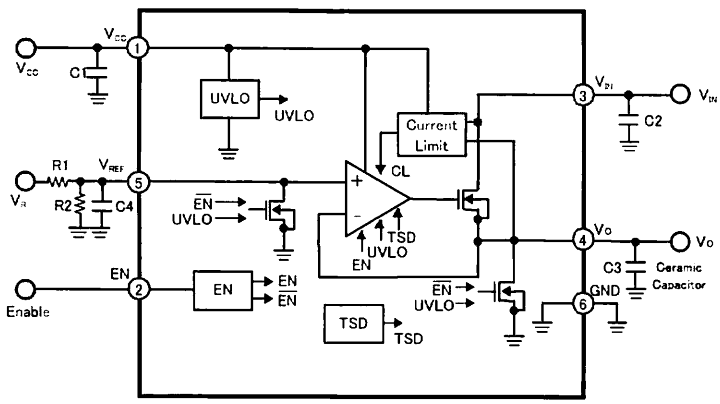
○ PHYSICAL DIMENSIONS



(UNIT:mm)

HVSOF6

○ BLOCK DIAGRAM



○ Pin number　Pin name

PIN No.	Pin name
1	V_{CC}
2	EN
3	V_{IN}
4	V_O
5	V_{REF}
6	GND
-	FIN

OΝOTES FOR USE

(1) Absolute maximum range
Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.

(2) Ground potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.

(3) Thermal Design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(4) Using in the strong electromagnetic field
Use in strong electromagnetic fields may cause malfunctions.

(5) ASO
Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.

(6) Thermal shutdown circuit
The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off (open) state. Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions. It is not intended to protect the IC per se or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

TSD ON temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
175	15

(7) GND pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(8) Output Voltage Setting (R1, R2)
Output volage is adjusted with reference voltage V_R and resistor (R1 and R2). output voltage is calculated as V_Rx(R1+R2)/R1. Total 10kohm resistor (R1+R2) is recommended so that the output voltage is not affected by the V_{REF} bias current (Typ. 100nA).

(9) Output Capacitor (C3)
Mount an output capacitor between Vo and GND for stability purposes. The output capacitor is for the open loop gain phase compensation and reduces the output voltage load regulation. If the capacitor value is not large enough, the output voltage may oscillate. And if the equivalent series resistance (ESR) is too large, the output voltage rise/drop increases during a sudden load change. A 22uF ceramic capacitor is recommended. However, the stability depends on the characteristics of temperature and load. And if several kinds of capacitors are utilized in parallel, the output voltage may oscillate due to lack of phase margin. Please confirm operation across a variety of temperature and load conditions.

(10) Input Capacitor (C1, C2)
The input capacitor reduces the output impedence of the voltage supply source connected in the VCC and VIN. If the output impedence of this power supply increases, the input voltage (VCC,VIN) may become unstable. This may result in the output voltage oscillation or lowering ripple rejection. A low ESR 10uF capacitor with minimal susceptibility to temperature is preferable, but stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

(11) V_{REF} Capacitor (C4)
The start up time of the output voltage can be adjusted by the value of C4, R1 and R2 in V_{REF}. When EN is High or UVLO function is deactivated, the output voltage starts up with the specific equation determined by C4, R1, and R2. The capacitor C4 with minimal susceptibility to temperature such as X5R or X7R is recommended.

(12) Input Terminal (V_{CC},V_{IN},EN, V_{REF})
The EN, V_{IN}, V_{CC}, and V_{REF} are isolatetd. The UVLO protects incorrect operation when the voltage level of V_{CC} are low. The output becomes high when V_{CC} and EN reach the individual threshold level independent of the start-up pin order.

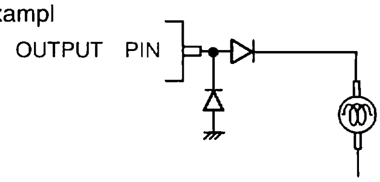
(13) Heat sink (FIN)
Since the heat sink (FIN) is connected with the Sub, short it to the GND. It is possible to minimize the thermal resistance by soldering it to GND plane of PCB.

(14) Short-circuits between pins and and mounting errors
Do not short-circuit between output pin (Vo) and supply pin (Vcc) or ground (GND), or between supply pin (Vcc) and ground (GND). Mounting errors, such as incorrect positioning or orientation, may destroy the device.

(15) This product is not designed for protection against radioactive rays.

(16) Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.

(Exampl



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