



# 200-MHz 24-Output Buffer for 4 DDR or 3 SDRAM DIMMS

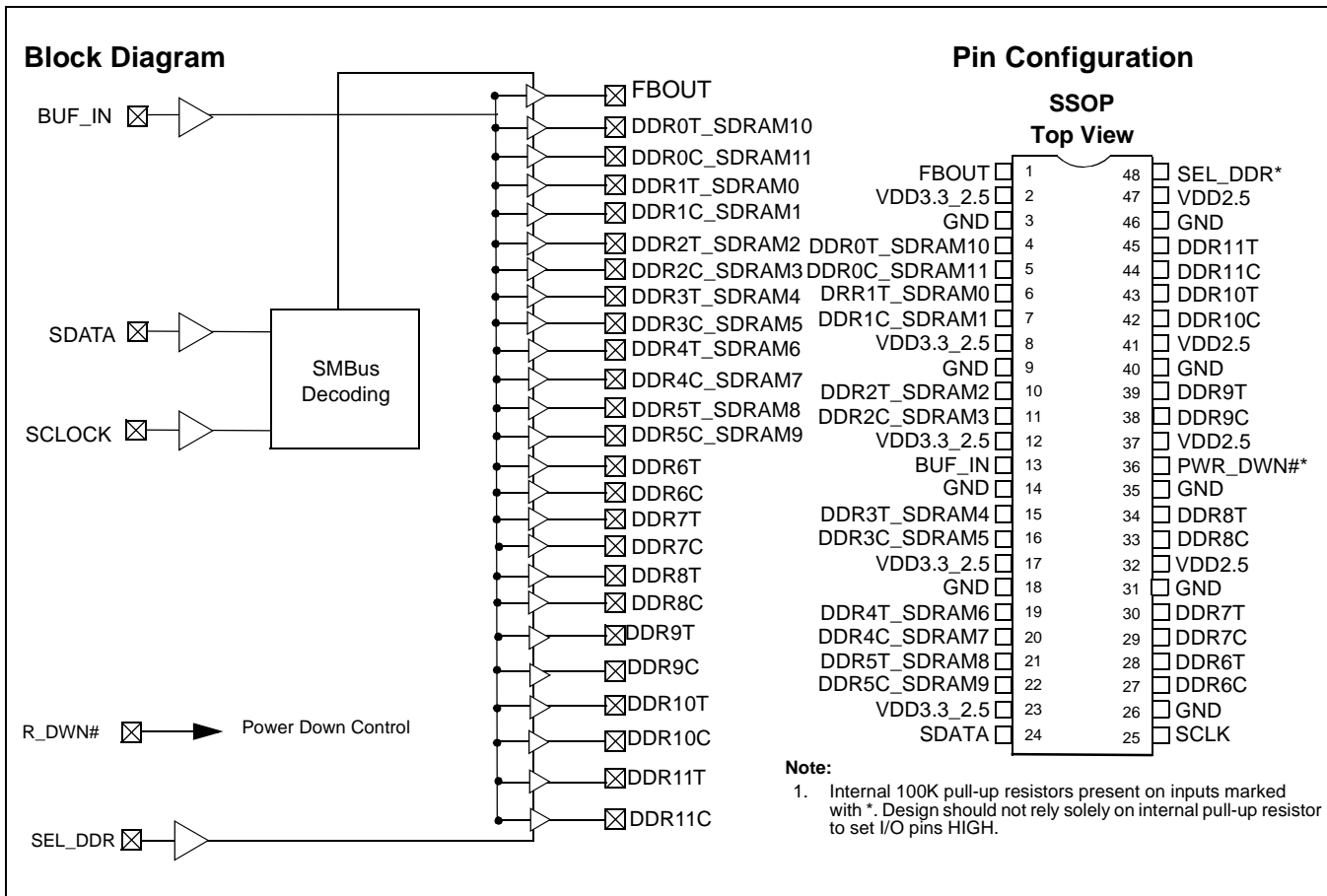
## Features

- One input to 24-output buffer/driver
- Supports up to 4 DDR DIMMs or 3 SDRAM DIMMS
- One additional output for feedback
- SMBus interface for individual output control
- Low skew outputs (< 100 ps)
- Supports 266-, 333-, and 400-MHz DDR SDRAM
- Dedicated pin for power management support
- Space-saving 48-pin SSOP package

## Functional Description

The W255 is a 3.3V/2.5V buffer designed to distribute high-speed clocks in PC applications. The part has 24 outputs. Designers can configure these outputs to support four unbuffered DDR DIMMS or to support three unbuffered standard SDRAM DIMMs and two DDR DIMMS. The W255 can be used in conjunction with the W250 or similar clock synthesizer for the VIA Pro 266 chipset.

The W255 also includes an SMBus interface which can enable or disable each output clock. On power-up, all output clocks are enabled (internal pull up).



**Pin Summary**

Pin Name	Pins	Pin Description
SEL_DDR	48	<p><b>Input to configure for DDR-ONLY mode or STANDARD SDRAM mode.</b>            1 = DDR-ONLY mode.            0 = STANDARD SDRAM mode.</p> <p>When SEL_DDR is pulled HIGH or configured for DDR-ONLY mode, pin 4, 5, 6, 7, 10, 11, 15, 16, 19, 20, 21, 22, 27, 28, 29, 30, 33, 34, 38, 39, 42, 43, 44 and 45 will be configured as DDR outputs.</p> <p>Connect VDD3.3_2.5 to a 2.5V power supply in DDR-ONLY mode.</p> <p>When SEL_DDR is pulled LOW or configured for STANDARD SDRAM output, pin 4, 5, 6, 7, 10, 11, 15, 16, 19 and 20, 21, 22 will be configured as STANDARD SDRAM outputs. Pin 27, 28, 29, 30, 33, 34, 38, 39, 42, 43, 44 and 45 will be configured as DDR outputs.</p> <p>Connect VDD3.3_2.5 to a 3.3V power supply in STANDARD SDRAM mode.</p>
SCLK	25	<b>SMBus clock input</b>
SDATA	24	<b>SMBus data input</b>
BUF_IN	13	<b>Reference input from chipset.</b> 2.5V input for DDR-ONLY mode; 3.3V input for STANDARD SDRAM mode.
FBOUT	1	<b>Feedback clock for chipset.</b> Output voltage depends on VDD3.3_2.5V.
PWR_DWN#	36	<b>Active LOW input to enable power-down mode;</b> all outputs will be pulled LOW.
DDR[6:11]T	28, 30, 34, 39, 43, 45	<b>Clock outputs.</b> These outputs provide copies of BUF_IN.
DDR[6:11]C	27, 29, 33, 38, 42, 44	<b>Clock outputs.</b> These outputs provide complementary copies of BUF_IN.
DDR[0:5]T_SDRAM [10,0,2,4,6,8]	4, 6, 10, 15, 19, 21	<b>Clock outputs.</b> These outputs provide copies of BUF_IN. Voltage swing depends on VDD3.3_2.5 power supply.
DDR[0:5]C_SDRAM [11,1,3,5,7,9]	5, 7, 11, 16, 20, 22	<b>Clock outputs.</b> These outputs provide complementary copies of BUF_IN when SEL_DDR is active. These outputs provide copies of BUF_IN when SEL_DDR is inactive. Voltage swing depends on VDD3.3_2.5 power supply.
VDD3.3_2.5	2, 8, 12, 17, 23	<b>Connect to 2.5V power supply</b> when W255 is configured for DDR-ONLY mode. Connect to 3.3V power supply, when W255 is configured for standard SDRAM mode.
VDD2.5	32, 37, 41, 47	<b>2.5V voltage supply</b>
GND	3, 9, 14, 18, 26, 31, 35, 40, 46	<b>Ground</b>

**Serial Configuration Map**

- The serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

.

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

- Reserved and unused bits should be programmed to "0."
- SMBus Address for the W255 is:

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	1	----

**Byte 6: Outputs Active/Inactive Register  
(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description	Default
Bit 7	–	Reserved, drive to 0	0
Bit 6	–	Reserved, drive to 0	0
Bit 5	–	Reserved, drive to 0	0
Bit 4	1	FBOUT	1
Bit 3	45,44	DDR11T, DDR11C	1
Bit 2	43, 42	DDR10T, DDR10C	1
Bit 1	39, 38	DDR9T, DDR9C	1
Bit 0	34, 33	DDR8T, DDR8C	1

**Byte 7: Outputs Active/Inactive Register  
(1 = Active, 0 = Inactive), Default = Active**

Bit	Pin #	Description	Default
Bit 7	30, 29	DDR7T, DDR7C	1
Bit 6	28, 27	DDR6T, DDR6C	1
Bit 5	21, 22	DDR5T_SDRAM8, DDR5C_SDRAM9	1
Bit 4	19, 20	DDR4T_SDRAM6, DDR4C_SDRAM7	1
Bit 3	15,16	DDR3T_SDRAM4, DDR3C_SDRAM5	1
Bit 2	10, 11	DDR2T_SDRAM2, DDR2C_SDRAM3	1
Bit 1	6, 7	DDR1T_SDRAM0, DDR1C_SDRAM1	1
Bit 0	4, 5	DDR0T_SDRAM10, DDR0C_SDRAM11	1

**Maximum Ratings**

Supply Voltage to Ground Potential .....-0.5 to +7.0V  
 DC Input Voltage (except BUF\_IN) .....-0.5V to  $V_{DD}+0.5$

Storage Temperature..... -65°C to +150°C  
 Static Discharge Voltage ..... > 2000V  
 (per MIL-STD-883, Method 3015)

**Operating Conditions** <sup>[2]</sup>

Parameter	Description	Min.	Typ.	Max.	Unit
VDD3.3	Supply Voltage	3.135		3.465	V
VDD2.5	Supply Voltage	2.375		2.625	V
T <sub>A</sub>	Operating Temperature (Ambient Temperature)	0		70	°C
C <sub>OUT</sub>	Output Capacitance		6		pF
C <sub>IN</sub>	Input Capacitance		5		pF

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Input LOW Voltage	For all pins except SMBus			0.8	V
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
I <sub>IL</sub>	Input LOW Current	V <sub>IN</sub> = 0V			50	μA
I <sub>IH</sub>	Input HIGH Current	V <sub>IN</sub> = V <sub>DD</sub>			50	μA
I <sub>OH</sub>	Output HIGH Current	V <sub>DD</sub> = 2.375V V <sub>OUT</sub> = 1V	-18	-32		mA
I <sub>OL</sub>	Output LOW Current	V <sub>DD</sub> = 2.375V V <sub>OUT</sub> = 1.2V	26	35		mA
V <sub>OL</sub>	Output LOW Voltage <sup>[3]</sup>	I <sub>OL</sub> = 12 mA, V <sub>DD</sub> = 2.375V			0.6	V
V <sub>OH</sub>	Output HIGH Voltage <sup>[3]</sup>	I <sub>OH</sub> = -12 mA, V <sub>DD</sub> = 2.375V	1.7			V
I <sub>DD</sub>	Supply Current <sup>[3]</sup> (DDR-only mode)	Unloaded outputs, 133 MHz			400	mA
I <sub>DD</sub>	Supply Current (DDR-only mode)	Loaded outputs, 133 MHz			500	mA
I <sub>DDS</sub>	Supply Current	PWR_DWN# = 0			100	μA
V <sub>OUT</sub>	Output Voltage Swing	See test circuitry (refer to Figure 1)	0.7		V <sub>DD</sub> +0.6	V
V <sub>OC</sub>	Output Crossing Voltage		(V <sub>DD</sub> /2) -0.1	V <sub>DD</sub> /2	(V <sub>DD</sub> /2) +0.1	V
I <sub>NDC</sub>	Input Clock Duty Cycle		48		52	%

**Switching Characteristics** <sup>[4]</sup>

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
–	Operating Frequency		66		200	MHz
–	Duty Cycle <sup>[3, 5]</sup> = t <sub>2</sub> + t <sub>1</sub>	Measured at 1.4V for 3.3V outputs Measured at V <sub>DD</sub> /2 for 2.5V outputs	I <sub>NDC</sub> -5%		I <sub>NDC</sub> +5%	%
t <sub>3</sub>	SDRAM Rising Edge Rate <sup>[3]</sup>	Measured between 0.4V and 2.4V	1.0		2.75	V/ns
t <sub>4</sub>	SDRAM Falling Edge Rate <sup>[3]</sup>	Measured between 2.4V and 0.4V	1.0		2.75	V/ns
t <sub>3d</sub>	DDR Rising Edge Rate <sup>[3]</sup>	Measured between 20% to 80% of output (refer to Figure 1)	0.5		1.50	V/ns

**Notes:**

- Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- Parameter is guaranteed by design and characterization. Not 100% tested in production.
- All parameters specified with loaded outputs.
- Duty cycle of input clock is 50%. Rising and falling edge rate is greater than 1 V/ns.

**Switching Characteristics** (continued)<sup>[4]</sup>

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
$t_{4d}$	DDR Falling Edge Rate <sup>[3]</sup>	Measured between 20% to 80% of output (refer to <i>Figure 1</i> )	0.5		1.50	V/ns
$t_5$	Output to Output Skew for DDR <sup>[3]</sup>	All outputs equally loaded			100	ps
$t_6$	Output to Output Skew for SDRAM <sup>[3]</sup>	All outputs equally loaded			150	ps
$t_7$	SDRAM Buffer LH Prop. Delay <sup>[3]</sup>	Input edge greater than 1 V/ns	5		10	ns
$t_8$	SDRAM Buffer HL Prop. Delay <sup>[3]</sup>	Input edge greater than 1 V/ns	5		10	ns

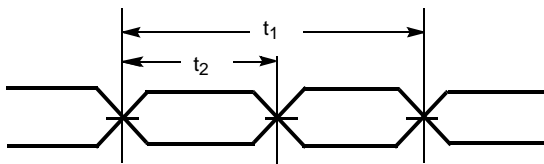
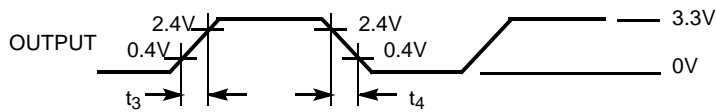
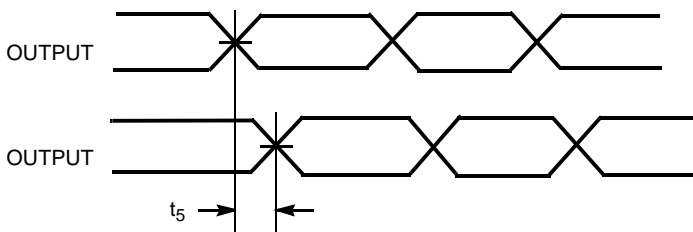
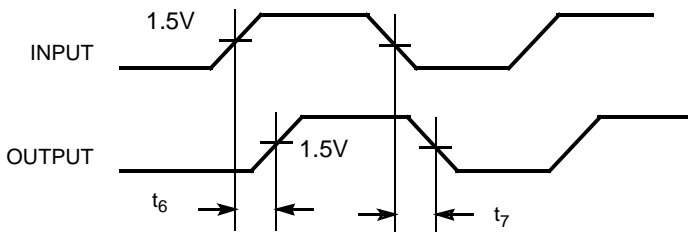
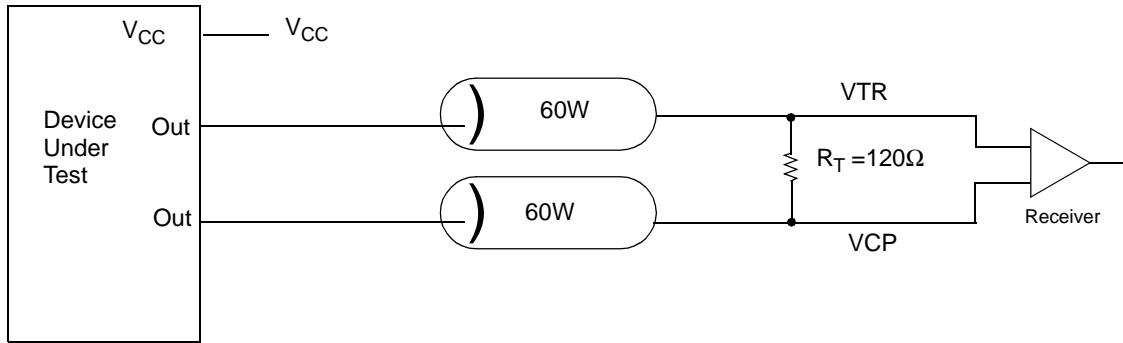
**Switching Waveforms**
**Duty Cycle Timing**

**All Outputs Rise/Fall Time**

**Output-Output Skew**

**SDRAM Buffer HH and LL Propagation Delay**


Figure 1 shows the differential clock directly terminated by a 120Ω resistor.

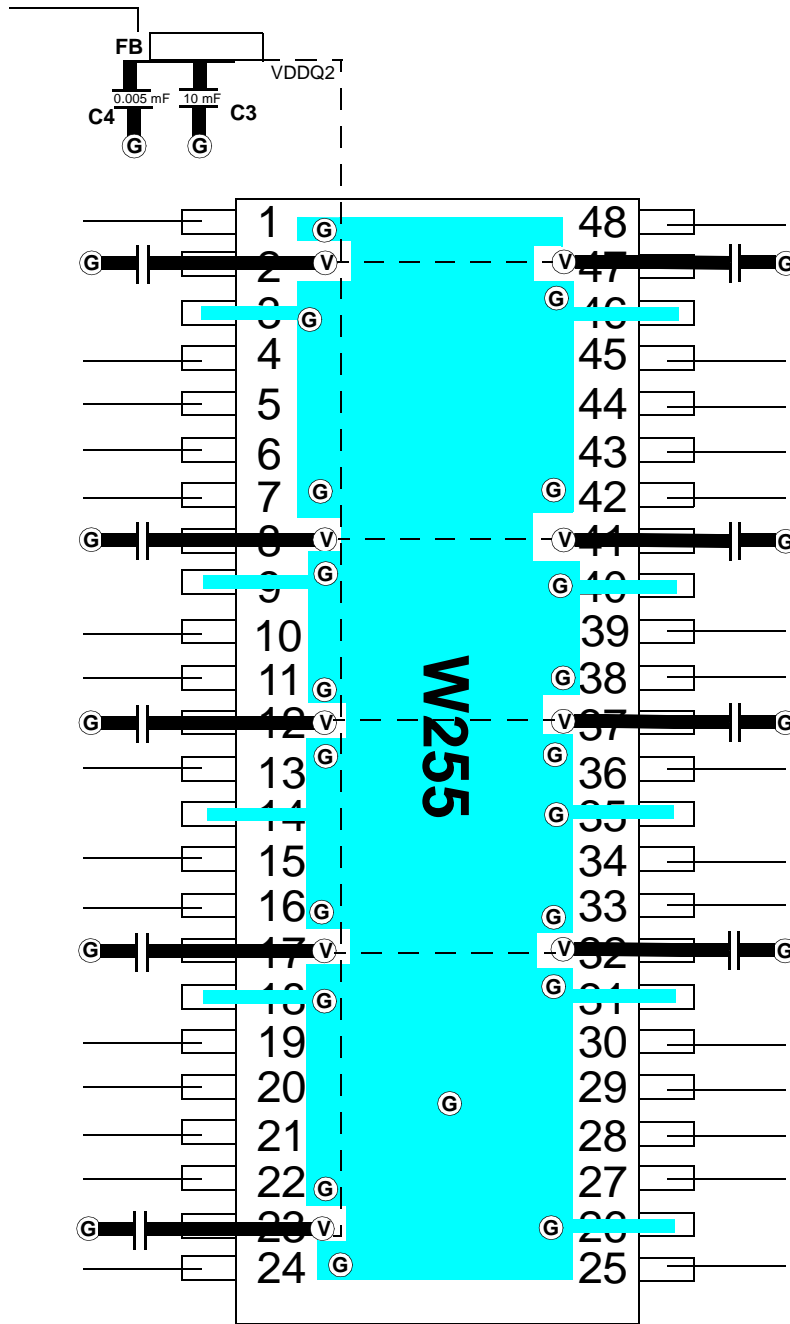


**Figure 1. Differential Signal Using Direct Termination Resistor**

### Ordering Information

Ordering Code	Package Type	Operating Range
W255H	48-pin SSOP	Commercial
W255HT	48-pin SSOP–Tape and Reel Option	Commercial

Layout Example for DDR 2.5V Only

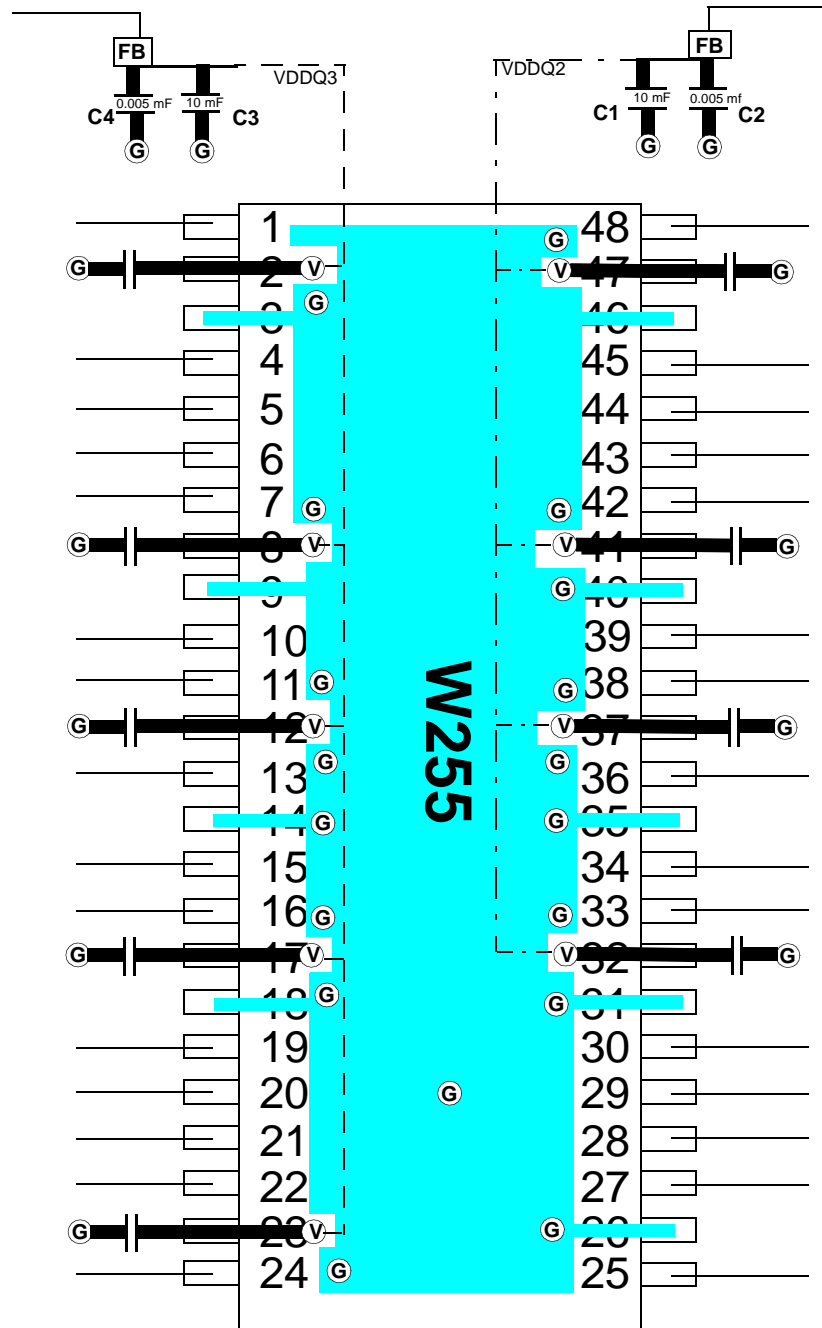


FB = Dale ILB1206 - 300 (300Ω @ 100 MHz) or TDK ACB 2012L-120

Ceramic Caps C3 = 10–22 μF      C4 = 0.005 μF

Ⓞ = VIA to GND plane layer    Ⓧ = VIA to respective supply plane layer

Note: Each supply plane or strip should have a ferrite bead and capacitors  
All bypass caps = 0.1 μF ceramic

**Layout Example SDRAM (Mixed Voltage)**


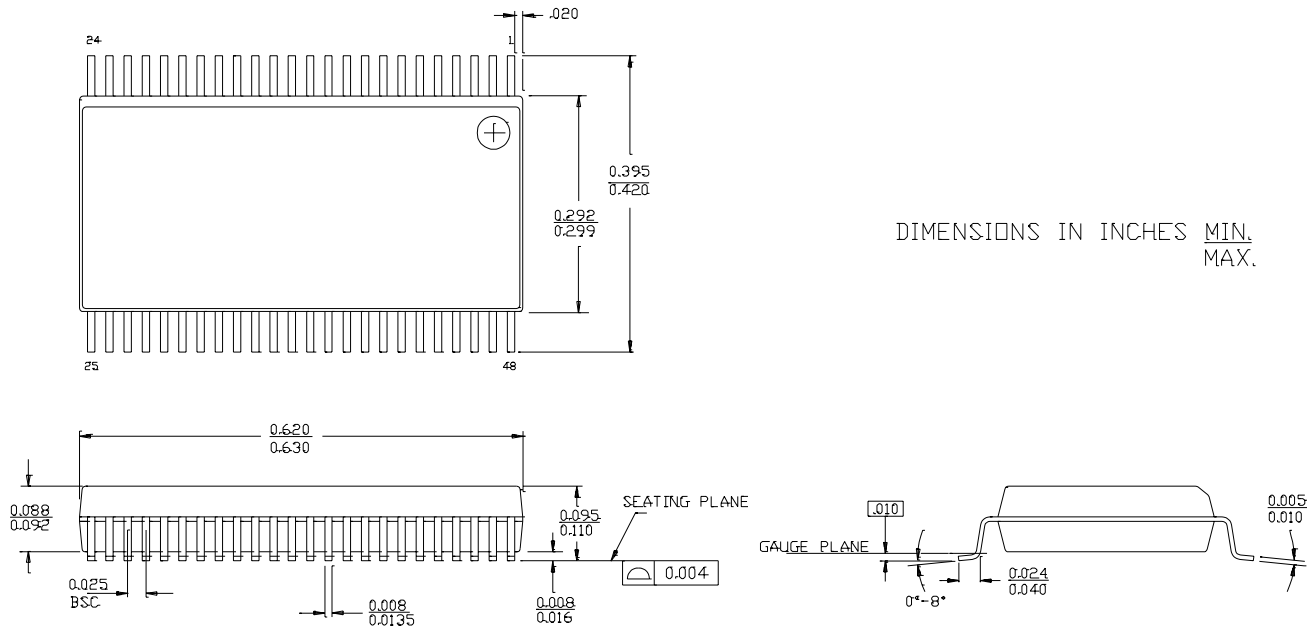
**FB = Dale ILB1206 - 300 (300Ω @ 100 MHz) or TDK ACB 2012L-120**

**Ceramic Caps C1 and C3 = 10–22 μF C2 & C4 = 0.005 μF C6 = 0.1 μF**

**ⓐ = VIA to GND plane layer ⓑ = VIA to respective supply plane layer**

**Note: Each supply plane or strip should have a ferrite bead and capacitors  
All bypass caps = 0.1 μF ceramic**



**Package Diagram**
**48-lead Shrunken Small Outline Package O48**


DIMENSIONS IN INCHES MIN. MAX.

51-85061-°C

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Document Title: W255 200MHz 24 Output Buffer for 4 DDR or 3 SDRAM DIMMs				
Document Number: 38-07255				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	110520	12/04/01	SZV	Change from Spec number: 38-01082 to 38-07255
*A	112154	03/01/02	IKA	Added 333 MHz for DDR SDRAM
*B	114554	05/07/02	INA	Added 400 MHz for DDR SDRAM
*C	122857	12/14/02	RBI	Power up requirements added to Operating Conditions Information