HSDL-3210

IrDA® Compliant Low Power
1.15 Mbit/s Infrared Transceiver

Data Sheet

Description

The HSDL-3210 is one of a new generation of low-cost Infrared (IR) transceiver modules from Avago Technologies. It features one of the smallest footprint in the industry at 2.5 H x 8.0 W x 3.0 D mm. Although the supply voltage can range from 2.7 V to 3.6 V, the LED is driven by an internal constant current source of 60 mA at SIR data rates and 150 mA at MIR data rates.

The HSDL-3210 incorporates the capability for adjustable optical power. The optical power can be adjusted lower when the nominal desired link distance is very short. At 5 cm link distance, only 6% of the full power is required.

The HSDL-3210 supports the Serial Interface for Transceiver Control Specification that provides a common interface between the transceiver and controller. It is also designed to interface to input/output logic circuits as low as 1.5 V.

Features

- **Fully Compliant to IrDA 1.4 low power specification from 9.6 kbit/s to 1.15 Mbit/s**
- **Ultra small surface mount package**
- **Minimal height: 2.5 mm**
- **V_{CC} from 2.7 to 3.6 volts**
- **Interface to 1.5 volts input/output logic circuits**
- **Withstands 100 mV_{p-p} power supply ripple typically**
- **Adjustable optical power for link distance from 5 to 20 cm**
- **Low shutdown current – 10 nA typical**
- **Complete shutdown – TxD, RxD, PIN diode**
- **Three optional external components**
- **Temperature performance guaranteed, -25°C to 85°C**
- **Integrated EMI shield**
- **IEC60825-1 class 1 eye safe**
- **Edge detection input – Prevents the LED from long turn on time**

Applications

- **Mobile telecom**
  - **– Cellular phones**
  - **– Pagers**
  - **– Smart phones**
- **Data communication**
  - **– PDAs**
  - **– Portable printers**
- **Digital imaging**
  - **– Digital cameras**
  - **– Photo-imaging printers**

Application Support Information

The Application Engineering group in Avago Technologies is available to assist you with the Technical understanding associated with HSDL-3210 infrared transceiver module. You can contact them through your local Avago sales representatives for additional details.

Ordering Information

Part Number	Packaging Type	Package	Quantity
HSDL-3210-021	Tape and Reel	Front View	2500

Application Circuit

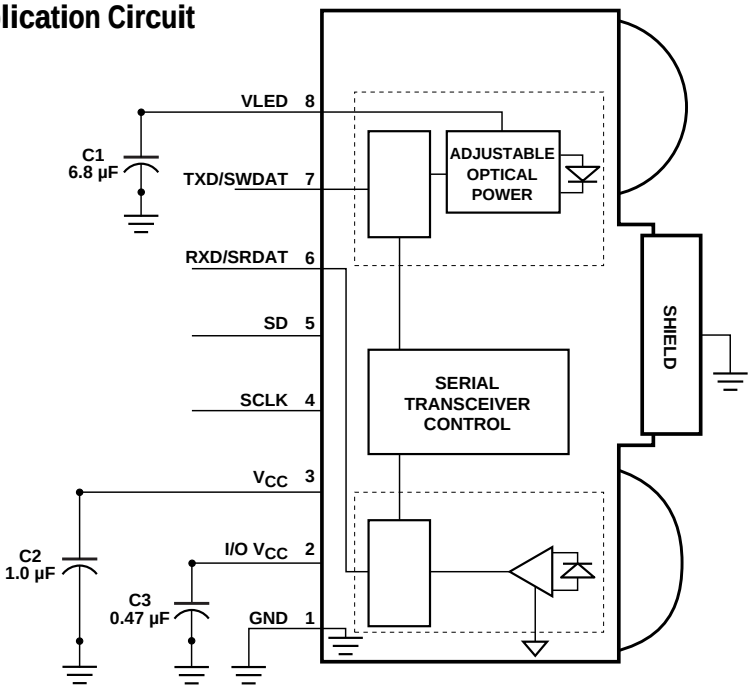

Figure 1. Functional block diagram of HSDL-3210.

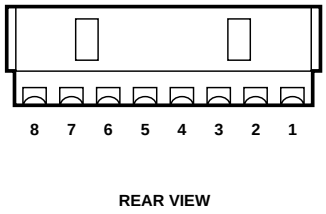

Figure 2. Rear view diagram with pin-out.

I/O Pin Configuration Table

Pin	Symbol	Description	Notes
1	GND	Ground	Connect to system ground.
2	IOV_{CC}	Input/Output V_{CC}	Connect to ASIC logic controller V_{CC} voltage.
3	V_{CC}	Supply Voltage	Regulated, 2.7 to 3.6 Volts
4	SCLK	Serial Clock	Use as clock input pin for programming mode. See Table 1 for details.
5	SD	Shut Down Active High	This pin must be driven either high or low, do NOT float the pin.
6	RXD/SRDAT	Receiver Data Output. Active Low	Output is a low pulse when a light pulse is received. SRDAT is the read data for the Serial Transceiver Control (STC). Do NOT float this pin.
7	TXD/SWDAT	Transmitter Data Input/ Serial Write Data	Logic High turns on the LED. If held high longer than ~20 µs, the LED is turned off. SWDAT is the write data for the Serial Transceiver Control (STC). Do NOT float this pin.
8	VLED	LED Supply Voltage	May be unregulated, 2.7 to 5.5 volts.
-	SHIELD	EMI Shield	Connect to system ground via a low inductance trace. For best performance, do not connect to GND directly at the part.

Recommended Application Circuit Components

Component	Recommended Value	Notes
C1	6.8 µF, ± 20%, Tantalum	1
C2	1.0 µF, ± 20%, Tantalum	
C3	0.47 µF, ± 20%, Ceramic	

Note:

1. C1, which is optional, must be placed within 0.7 cm of the HSDL-3210 to obtain optimum noise immunity.

Serial Interface for Transceiver Control

The Serial Interface for Transceiver Control (STC) is used to control and program the features of the transceiver. These features include input/output (I/O) control, optical power adjustment and shut down.

The STC requires three signals: a serial clock (SCLK) that is used for timing, and two unidirectional lines multiplexed with the transmitter (write) TXD/SWDAT and receiver (read) RXD/SRDAT infrared signal lines.

The HSDL-3210 supports the write function to disable/enable the TXD line, disable/enable the RXD line and 4-level optical power adjustment.

A set of commands is provided to handle the programming control features. The general command format is shown in Figure 3. The HSDL-3210 STC Write Data Commands are shown in Table 1.

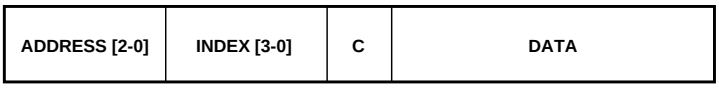

Figure 3. General command format.

Table 1. Serial Interface for Transceiver Control – Write Data Format

	Address [2-0]	Index [3-0]	C	Data
IrDA Data –data rates				
SIR (2.4 to 115.2 Kbps)	000	0001	1	00000000
MIR (0.576, 1.152 Mbps)	000	0001	1	00000001
I/O Control				
SD Normal Mode	000	0000	1	XXXXXXX1
SD Sleep Mode	000	0000	1	XXXXXXX0
RXD disable	000	0000	1	XXXXXX0X
RXD enable	000	0000	1	XXXXXX1X
TXD disable	000	0000	1	XXXXX0XX
TXD enable	000	0000	1	XXXXX1XX
Optical Power Adjustment				
10% link distance	000	0010	1	00XXXXXX
25% link distance	000	0010	1	01XXXXXX
50% link distance	000	0010	1	10XXXXXX
100% link distance	000	0010	1	11XXXXXX

Table 2. Serial Interface for Transceiver Control – Read Data Format

	Address [2-0]	Index [3-0]	C	Data
IrDA Data –data rates				
SIR (2.4 to 115.2 Kbps)	000	0001	0	00000000
MIR (0.576, 1.152 Mbps)	000	0001	0	00000001
I/O Control				
SD Normal Mode	000	0000	0	XXXXXXX0
SD Sleep Mode	000	0000	0	XXXXXXX1
RXD disable	000	0000	0	XXXXXX0X
RXD enable	000	0000	0	XXXXXX1X
TXD disable	000	0000	0	XXXXX0XX
TXD enable	000	0000	0	XXXXX1XX
Optical Power Adjustment				
10% link distance	000	0010	0	00XXXXXX
25% link distance	000	0010	0	01XXXXXX
50% link distance	000	0010	0	10XXXXXX
100% link distance	000	0010	0	11XXXXXX
ID				
Manufacturer	000	1111	0	00000001
Product	000	1111	0	01000001

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Transceiver I/O Truth Table

STC SD Mode	SCLK	SD	TXD	LED	Receiver	RXD	Notes
Normal Mode	Low	Low	High	On	Don't care	Not Valid	2,3
			Low	Off	IrDA Signal	Low	4,5
					No Signal	High	
Sleep Mode			Don't care	Off	Don't care	High	6
Don't care	Don't care	High	Don't care	Off	Don't care	High	6

Notes:

2. If TXD is stuck in the high state, the LED will turn off after about 14 µs.
3. RXD will echo the TXD signal while TXD is transmitting data.
4. In-Band IrDA signals and data rates ≤ 1.152 Mbps.
5. RXD Logic Low is pulsed response.
6. RXD Logic High during shutdown is a weak pull up (equivalent to an approximately 300 kΩ resistor).

Caution: *The BiCMOS inherent to this design of this component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is ≤50°C/W.

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-40	100	°C
Operating Temperature	T_A	-25	85	°C
LED Supply Voltage	V_{LED}	0	6.5	V
Supply Voltage	V_{CC}	0	6.5	V
Input/Output Voltage	IOV_{CC}	0	V_{CC}	V
Input Voltage: TXD, SCLK, SD	V_I	0	V_{CC}+ 0.5	V
Output Voltage: RXD	V_O	-0.5	V_{CC}+ 0.5	V

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Units	Conditions	Notes
Operating Temperature		T_A	-25	85	°C		
Supply Voltage		V_{CC}	2.7	3.6	V		
Logic Input Voltage	Logic High	V_{IH}	2/3 IOV_{CC}	IOV_{CC}	V	1.5 V ≤IOV_{CC} ≤3.6 V	
for TXD ,SCLK, SD	Logic Low	V_{IL}	0	1/3 IOV_{CC}	V	1.5 V ≤IOV_{CC} ≤3.6 V	
Logic High Receiver Input Irradiance EIH		EI_H	0.0081	500	mW/cm^2	For in-band signals ≤115.2kb/s (SIR)	7
			0.0225	500	mW/cm^2	0.576 Mb/s ≤ in-band signals ≤ 1.15 Mb/s (MIR)	7
Logic Low Receiver Input		EI_L		0.3	μW/cm^2	For in-band signals.	
Input/Output Voltage		IOV_{CC}	1.5	V_{CC}	V		
Receiver Data Rate			0.0024	1.152	Mb/s		

Electrical and Optical Specifications

Specifications hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values are at 25°C and 3.0 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions	Notes
Receiver								
RXD Output Voltage	Logic High	V_{OH}	IOV_{CC} -0.2		IOV_{CC}	V	I_{OH}=-200 µA, EI ≤0.3 µW/cm^2	
	Logic Low	V_{OL}	0		0.4	V	I_{OL}=200 µA	8
Viewing Angle		$2\phi_{1/2}$	30			°		
Peak Sensitivity Wavelength		λp		880		nm		
RXD Pulse Width (SIR)		t_{PW} (SIR)	1		7.5	µs	C_L =10 pF	8,9
RXD Pulse Width (MIR)		t_{PW}(MIR)	200		750	ns	C_L =10 pF	9
RXD Rise and Fall Times		t_R, t_F		25	100	ns	C_L =10 pF	
Receiver Latency Time		t_L		25	50	µs		10
Receiver Wake Up Time		t_{RW}		30	100	µs		11
Transmitter								
Radiant Intensity (SIR)		IE_H	4	15	28.8	mW/Sr	T_A=25°C, $\theta_{1/2}$ ≤15°, TXD ≥ V_{IH}	
Radiant Intensity (MIR)		IE_H	9	30	72	mW/Sr	T_A=25°C, $\theta_{1/2}$ ≤15°, TXD ≥ V_{IH}	
Peak Wavelength		λp		875		nm		
Spectral Line Half Width		$\Delta\lambda_{1/2}$		35		nm		
Viewing Angle		$2\phi_{1/2}$	30		60	°		
Optical Pulse Width (SIR)		tpw	1.41	1.6	2.23	µs	tpw(TXD) = 1.6 µs	
Optical Pulse Width (MIR, IOV_{CC} ≥1.5 V)		tpw	148	217	260	ns	tpw(TXD) = 217 ns	
Optical Rise and Fall Times (SIR)		tr (EI) tf (EI)		50	600	ns	tpw(TXD) = 1.6 µs	
Optical Rise and Fall Times (MIR)		tr (EI) tf (EI)		30	40	ns	tpw(TXD) = 1.6 µs	
LED Current	On (SIR)	I_{VLED}		60	72	mA	V_{VLED}=V_{CC}=3.6 V, V_I(TXD) ≥ V_{IH}	
	On (MIR)	I_{VLED}		150	180	mA	V_{VLED}=V_{CC}=3.6 V, V_I(TXD) ≥ V_{IH}	
	Current Off	I_{VLED}		0.005	1	µs	V_{VLED}=V_{CC}=3.6 V, V_I(TXD) ≤ V_{IL}	
Transceiver								
TXD Input Current	High	I_H		10	200	nA	V_I ≥ V_{IH}	
	Low	I_L		-10	-200	nA	0 ≤ V_I ≤ V_{IL}	
Supply Current	Shutdown	I_{CC1}		0.01		µA	V_{CC}=3.6 V, V_{SD} ≥ V_{CC} - 0.5, T_A=25°C	
	Idle	I_{CC2}		300	450	µA	V_{CC}=3.6 V, V_I(TXD) ≤ V_{IL},EI=0	
	Active, Receive	I_{CC3}		0.8	3.0	mA	V_{CC}=3.6 V, V_I(TXD) ≤ V_{IL}	12,13

Notes:

7. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 nm ≤ λp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification.
8. For in band signals ≤ 1.152 Mbps where 9 µW/cm^2 ≤ EI ≤ 500 mW/cm^2.
9. For 0.576 Mbps ≤ in band signals ≤ 1.152 Mbps where 22.5 µW/cm^2 ≤ EI ≤ 500 mW/cm^2 .
10. Latency is defined as the time from the last TXD light output pulse until the receiver has recovered full sensitivity.
11. Receiver wake up time is measured from the SD pin high to low transition or V_{CC} power on, to valid RXD output.
12. Typical values are at EI = 10 mW/cm^2.
13. Maximum value is at EI = 500 mW/cm^2.

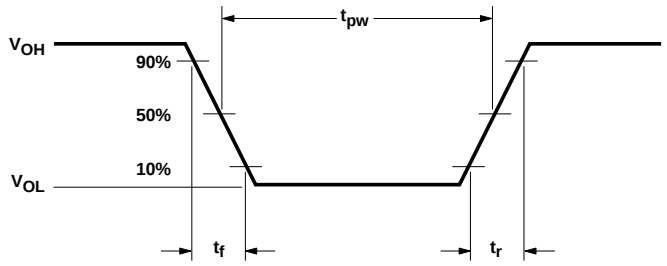


Figure 4. RXD output waveform.

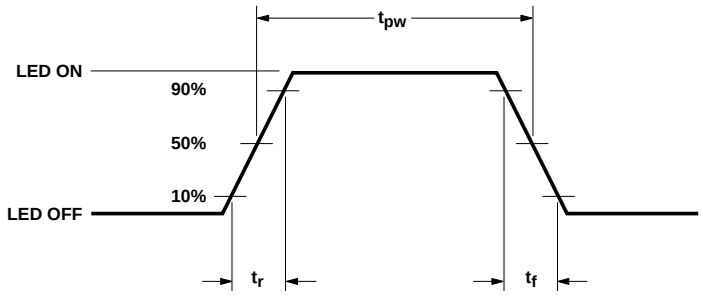


Figure 5. LED optical waveform.

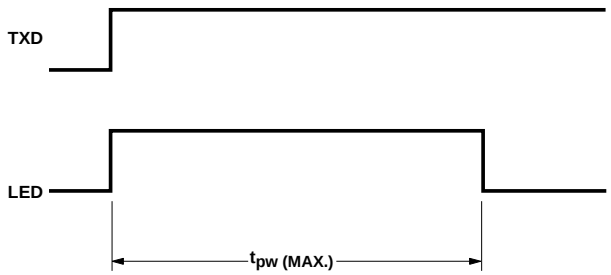


Figure 6. TXD 'Stuck On' protection waveform.

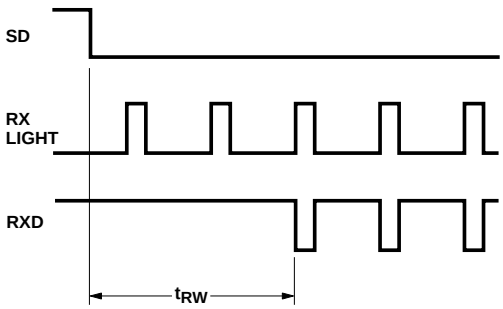


Figure 7. Receiver wakeup time waveform.

Package Dimensions

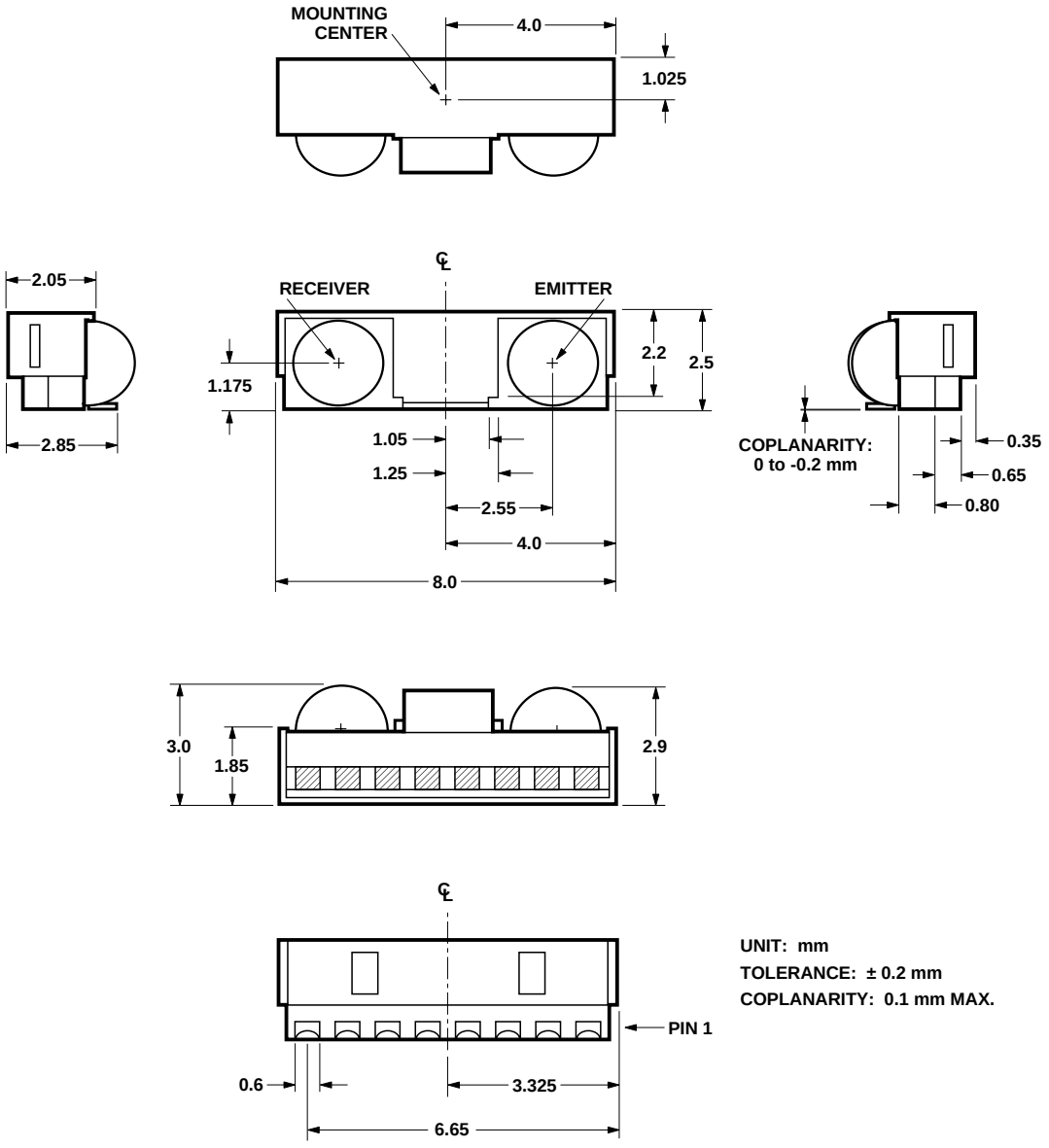
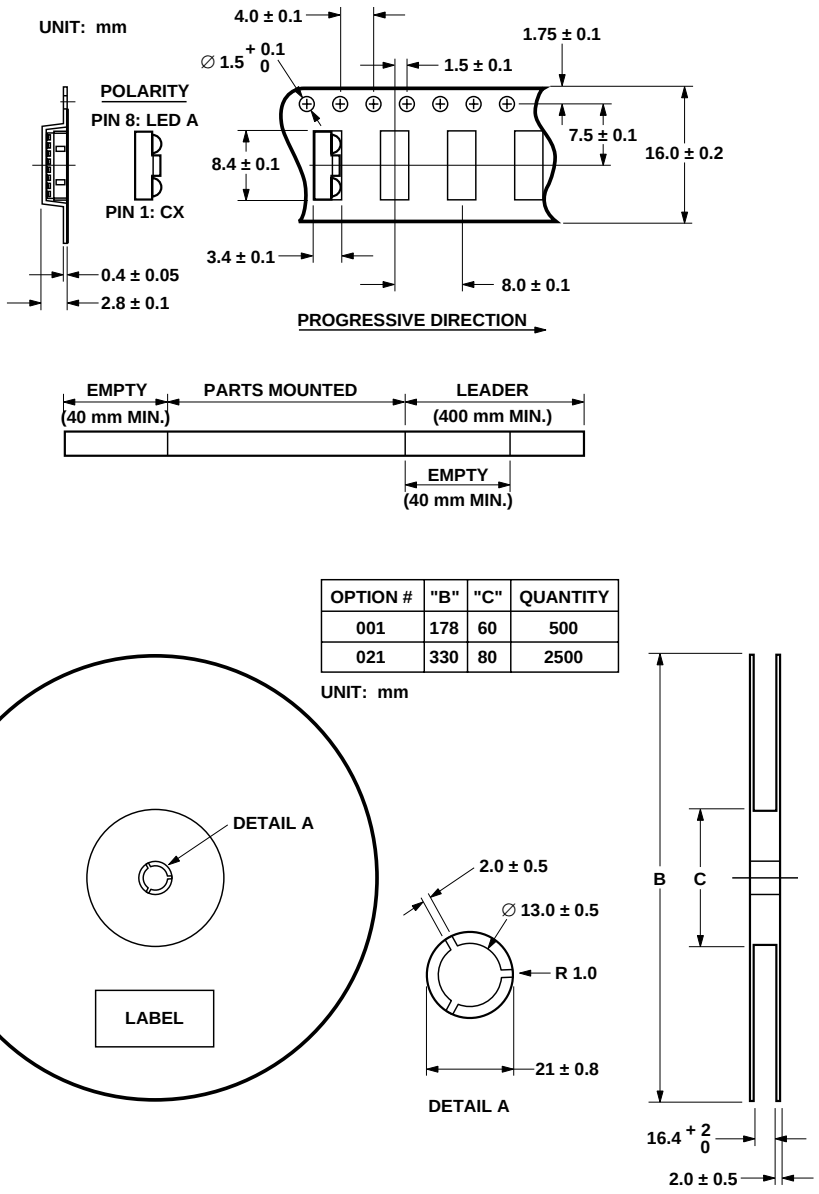


Figure 8. Package outline dimensions.

Tape and Reel Dimensions



OPTION #	"B"	"C"	QUANTITY
001	178	60	500
021	330	80	2500

UNIT: mm

Figure 9. Tape and reel dimensions.

Moisture-Proof Packaging

All HSDL-3210 options are shipped in moisture-proof packaging. Once opened, moisture absorption begins. This product is compliant to JEDEC level 4.

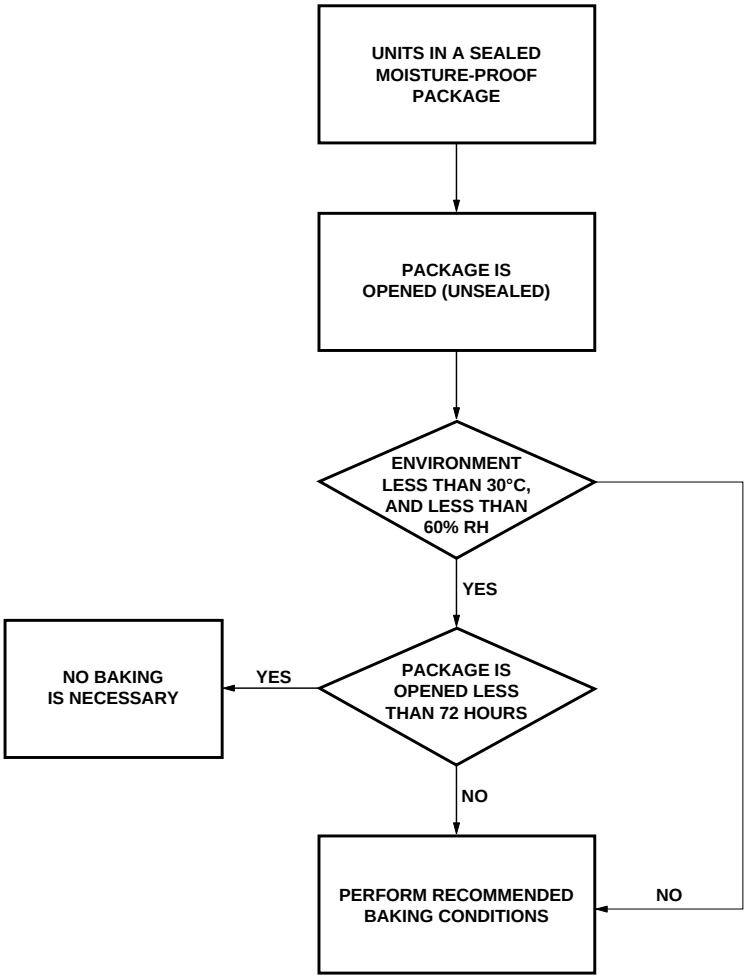


Figure 10. Baking conditions chart.

Baking Conditions

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Packaging	Temp.	Time
In Reels	60˚C	≥ 48 hours
In Bulk	100˚C	≥ 4 hours
	125˚C	≥ 2 hours
	150˚C	≥ 1 hour

Baking should only be done once.

Recommended Storage Conditions

Storage Temp.	10˚C to 30˚C
Relative Humidity	Below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within three days if stored at the recommended storage conditions.

Reflow Profile

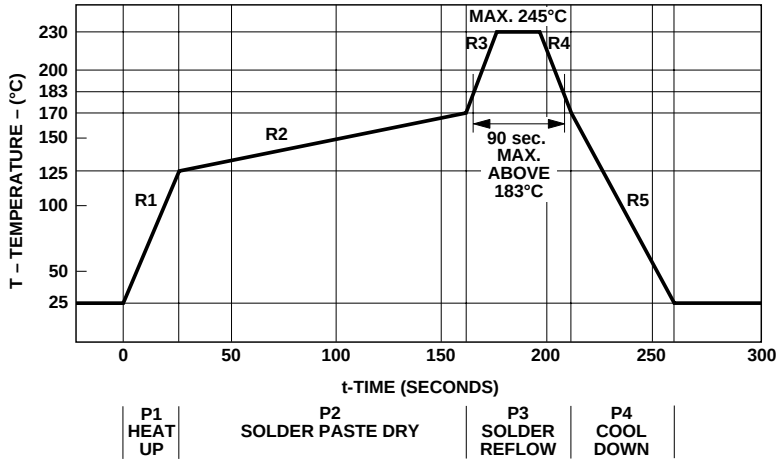


Figure 11. Reflow graph.

Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 125°C	4°C/s
Solder Paste Dry	P2, R2	125°C to 170°C	0.5°C/s
Solder Reflow	P3, R3	170°C to 230°C (245°C at 10 seconds max.)	4°C/s
	P3, R4	230°C to 170°C	–4°C/s
Cool Down	P4, R5	170°C to 25°C	–3°C/s

The reflow profile is a straight line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and HSDL-3210 castellation I/O pins are heated to a temperature of 125°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3210 castellation I/O pins.

Process zone P2 should be of sufficient time duration (> 60 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 170°C (338°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 230°C (446°F) for optimum results. The dwell time above the liquidus point of solder should be between 15 and 90 seconds. It usually takes about 15 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 90 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 170°C (338°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed –3°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3210 castellation I/O pins to change dimensions evenly, putting minimal stresses on the HSDL-3210 transceiver.

Appendix A : SMT Assembly Application Note

1.0 Solder Pad, Mask and Metal Solder Stencil Aperture

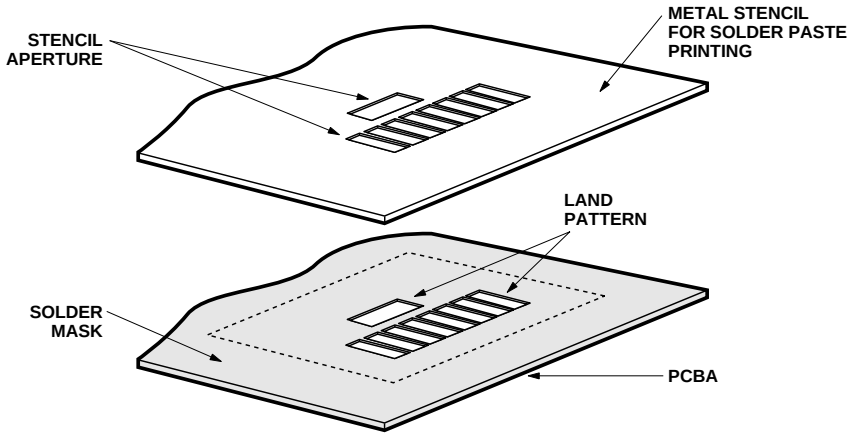


Figure 12. Stencil and PCBA.

1.1 Recommended Land Pattern

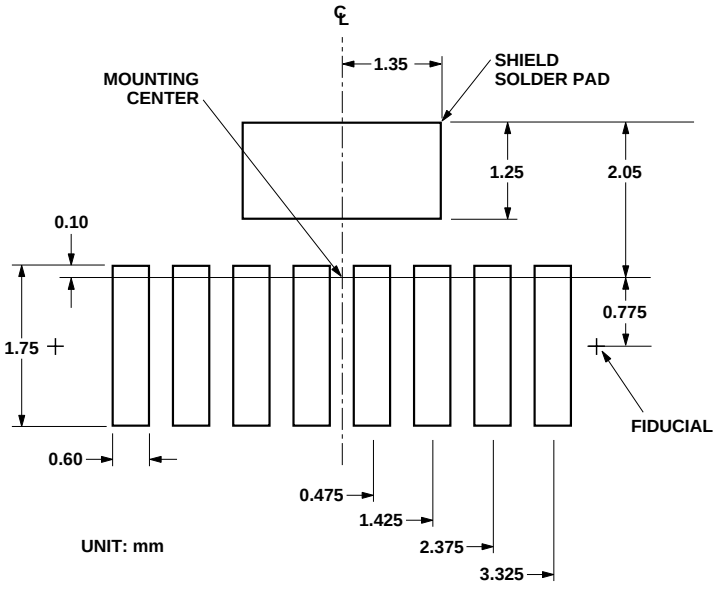


Figure 13. Land pattern.

1.2 Recommended Metal Solder Stencil Aperture

It is recommended that only a 0.152 mm (0.006 inches) or a 0.127 mm (0.005 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the table below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used.

Aperture opening for shield pad is 2.7 mm x 1.25 mm as per land pattern.

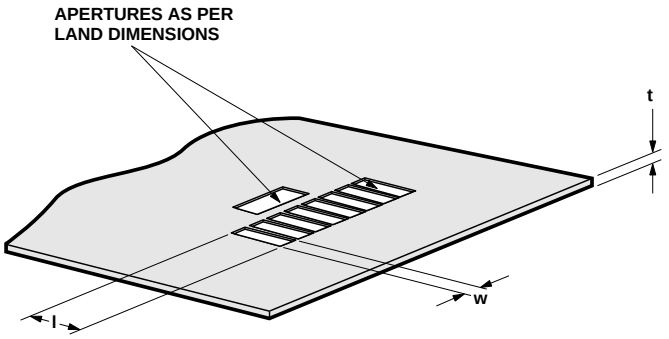


Figure 14. Solder stencil aperture.

Stencil Thickness, t (mm)	Aperture Size (mm)	
	Length, l	Width, w
0.152 mm	2.60 ± 0.05	0.55 ± 0.05
0.127 mm	3.00 ± 0.05	0.55 ± 0.05

1.3 Adjacent Land Keepout and Solder Mask Areas

Adjacent land keep-out is the **maximum space** occupied by the unit relative to the land pattern. There should be no other SMD components within this area.

The minimum solder resist strip width required to avoid solder bridging adjacent pads is **0.2 mm**. It is recommended that two fiducial crosses be placed at mid-length of the pads for unit alignment.

Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.

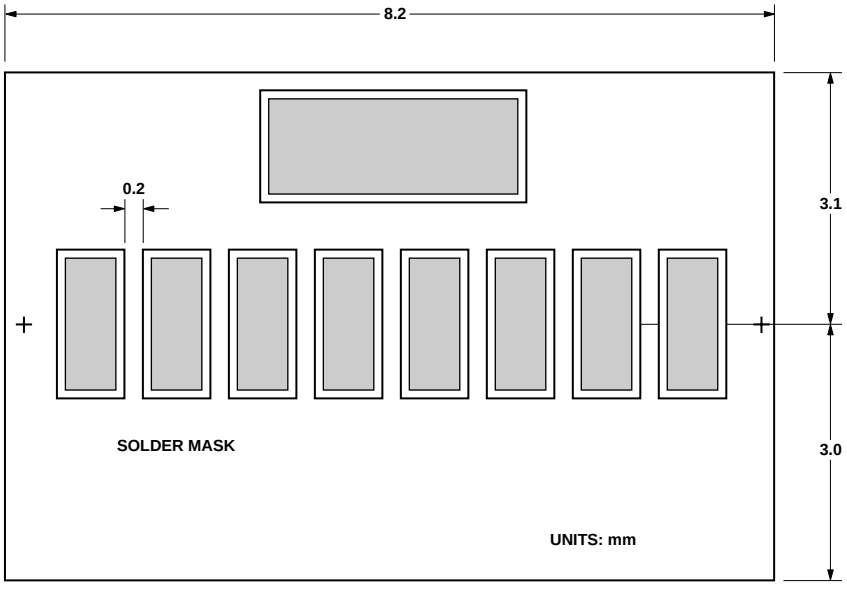


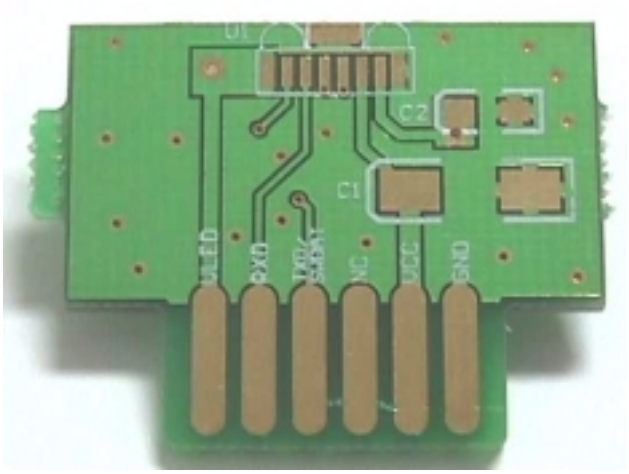
Figure 15. Adjacent land keep-out and solder mask areas.

Appendix B: PCB Layout Suggestion

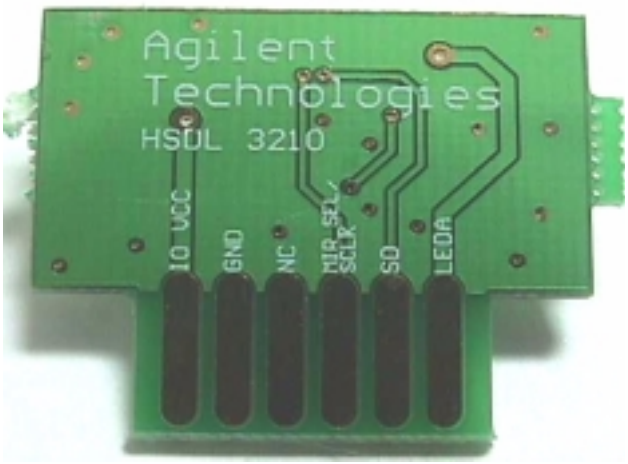
The following PCB layout shows a recommended layout that should result in good electrical and EMI performance. Things to note:

1. The ground plane should be continuous under the part, but should not extend under the shield trace.
2. The shield trace is a wide, low inductance trace back to the system ground.
3. C1 is an optional V_{CC} filter capacitor. It may be left out if the V_{CC} is clean.
4. V_{LED} can be connected to either unfiltered or unregulated power. If C1 is used, and if V_{LED} is connected to V_{CC}, the connection should be before the C1 cap.

A reference layout of a 2-layer Avago evaluation board for HSDL-3210 based on the guidelines stated above is shown below. For more details, please refer to Avago Application Note 1114, Infrared Transceiver PC Board Layout for Noise Immunity.



Top Layer



Bottom Layer

Figure 16. PCB layout suggestions.

Appendix C: General Application Guide for the HSDL-3210 Infrared IrDA® Compliant 1.15 Mb/s Transceiver

Description

The HSDL-3210, a low-cost and small form factor infrared transceiver, is designed to address the mobile computing market such as PDAs, as well as small embedded mobile products such as digital cameras and cellular phones. It is fully compliant to IrDA 1.3 low power specification from 9.6 kb/s to 1.152 Mb/s, and supports HP-SIR and TV Remote modes. The design of the HSDL-3210 also includes the following unique features:

- Supports the serial interface for transceiver control (STC) specification.
- Low passive component count.
- Shutdown mode for low power consumption requirement.
- Interface to input/output logic circuits as low as 1.5 V.
- Adjustable optical power management

Interface to Recommended I/O chips

The HSDL-3210's TXD data input is buffered to allow for CMOS drive levels. No peaking circuit or capacitor is required. Data rate from 9.6 kb/s up to 1.152 Mbp/s is available at the RXD pin.

The block diagram below shows how the IR port fits into a mobile phone and PDA platform.

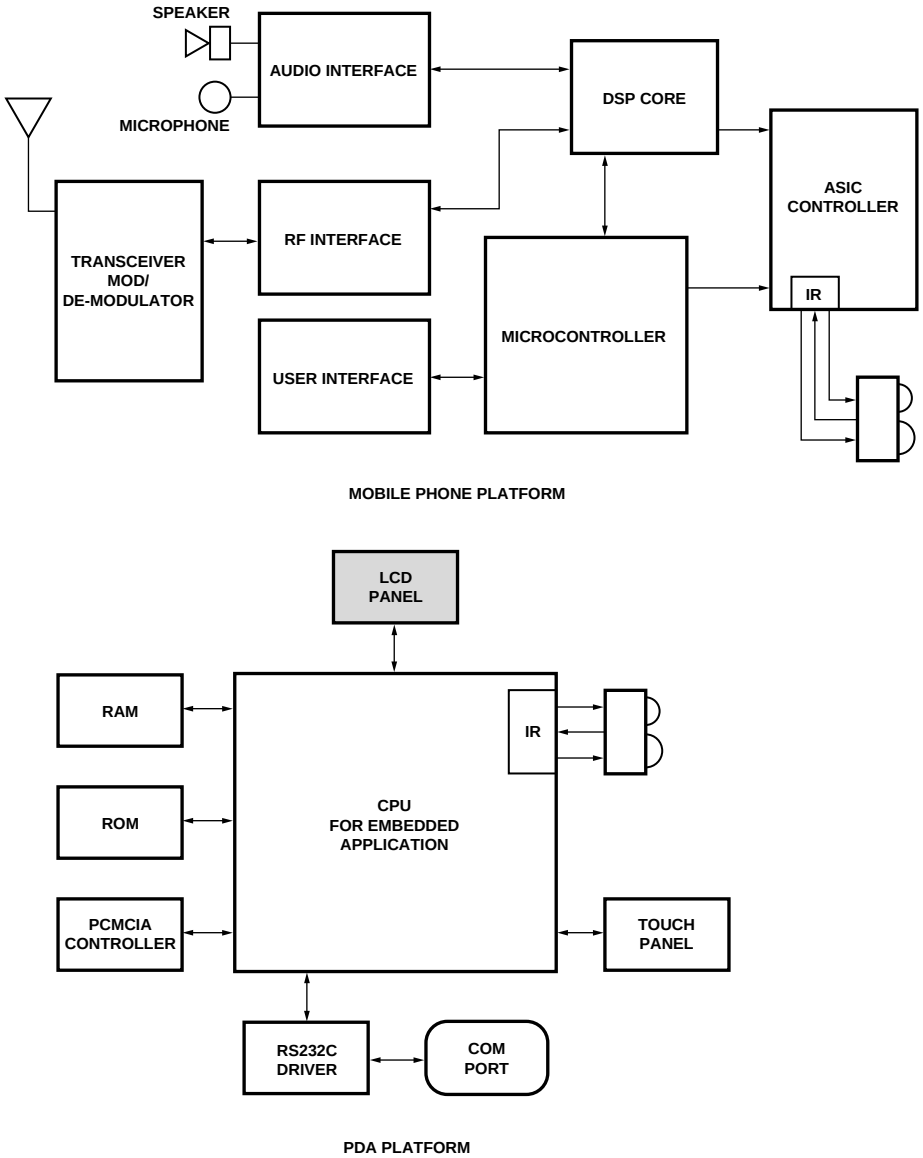


Figure 17. Mobile phone and PDA platform diagrams.

Serial Interface Transceiver Control (STC)

HSDL-3210 supports the serial interface for transceiver control specification that provides a common interface between the transceiver and controller.

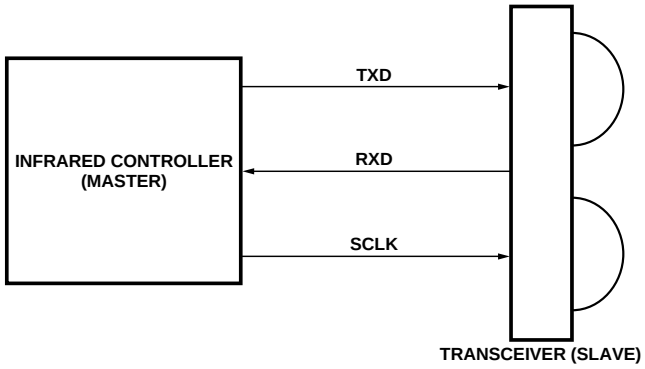
STC comprises a 3-wire interface: TXD/SWDAT, RXD/ARDAT and SCLK. This 3-wire interface abolishes the use of different modes and logic pins of existing transceivers. Instead registers on board the transceiver store operating modes and states, thus electrical interface can be standardized across different vendors and transceivers.

The diagram below shows the STC I/O between the transceiver and the IrDA controller.

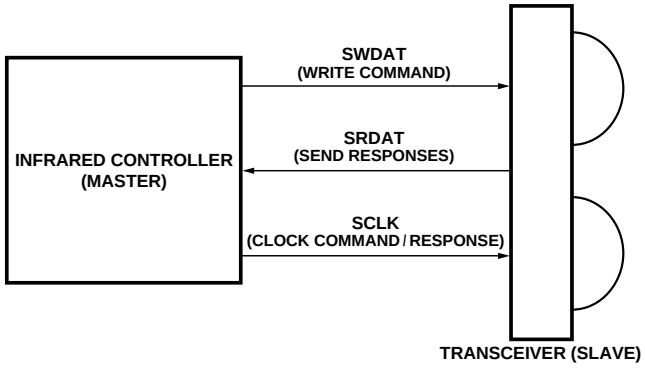
In normal operation, the TXD and RXD carry IR transmit and receive signals. In STC mode, SWDAT and SRDAT carry command and responses to and from the transceiver respectively.

Activity on the SCLK line determines whether the transceiver is to operate in the normal or STC mode.

Please refer to Avago Application Note 1270 Serial Transceiver Control for Infrared Transceivers for further information on implementing STC using HSDL-3210 as well as the lists of registers supported by HSDL-3210.



STC – NORMAL MODE



STC – COMMAND / RESPONSE MODE

Figure 18. STC block diagram.

STC Bus Protocol and Timing Diagrams

Bus Protocol

A set of commands is provided to handle the various transactions between the master and the slave. The general format is shown in Figure 19 whereby communications consist of a mandatory command phase followed by an optional response phase. The response phase occurs only when the slave needs to respond to a command.

The command format consists of either 2 or 3 bytes command. The first byte, which is mandatory and common to all transactions, consists of the address/index/control bits. There are two control fields. The first one is the "C" field which determines whether the command is a read or write operation or to act as a qualifier for a special operation. The second one is the "INDX" field whereby certain patterns define Special Transactions while others are for normal Data Transactions. The "ADDR" field is used to specify which transceiver the command is for. In a single transceiver system, this field is set to "000".

The second byte contains the data payload for a 2 byte command. For a 3 byte command, this second byte is an 8 bit extended index.

The third byte is the data payload when the extended index is used.

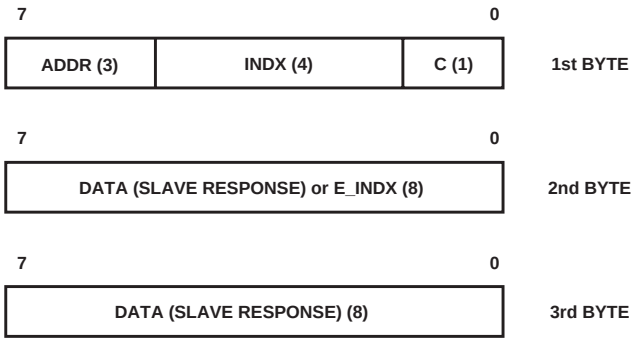


Figure 19. General command format.

Write Transactions

Write transactions are when the master writes data to the slave to select the slave's operational mode. This requires only the command phase as shown below.

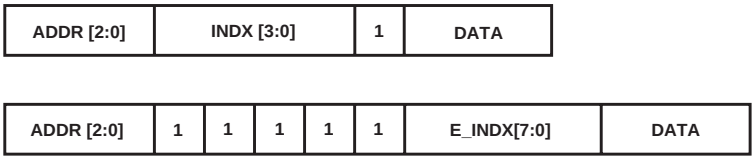


Figure 20. Write command phase format.

Read Transactions

Read transactions occur when the master queries the internal registers of the slave. The initial command phase is always followed by the response phase from the slave as shown below.

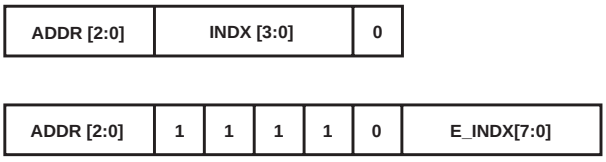


Figure 21a. Read command phase format.

Figure 21b. Slave response format.

Bus Timing Diagrams

The bus timings are designed to be simple and to minimize the effects of timing skew. This section discusses some key points with regard to bus timings and illustrates typical STC transactions with the use of waveforms.

Bus Timing Notes

1. Data is transferred in Little Endian order, that is, the LSB on the first byte is transmitted first and the MSB of the second or third byte is transmitted last.
2. There are no gaps between bytes in the command or response phases.
3. Each byte in the command and response phase is preceded by a start bit on the SCLK line.
4. For data sampling and clocking,
   - 4.1. Input data is sampled on the rising edge of SCLK.
   - 4.2. Output data from the controller is clocked out on the falling edge of SCLK.
   - 4.3. Output data from the slave is clocked out on the rising edge of SCLK.
5. The first low-to-high transition of SCLK indicates that an STC transition is pending. On receipt of his rising edge, the slave will disable the LED. The next SCLK low-to-high transition indicates the start cycle, followed by the command phase (which the controller puts out on the SWDAT line). The LED needs to be disabled since TXD and SWDAT are multiplexed. If the LED is not disabled, then the LED will pulse according to the SWDAT bit stream.
6. The LED is re-enabled (by the slave) on the last SCLK of the STC transaction bit stream. Normal infrared transmission can resume. No SCLK transitions should take place until the next STC transaction else the LED will be disabled.
7. The response from the slave is carried on the SRDAT line, which is multiplexed with RXD. The detector is (internally) disabled by the slave during the response phase. This is to prevent stray IR transitions from corrupting the SRDAT bit stream.
8. During a READ transaction, the controller holds the SWDAT line low for 1 clock after sending the ADDRESS and INDEX byte. It then holds it high and low for 3 clocks before the end of the transaction. This is to allow the transceiver to monitor the impending end of a transaction rather than by counting pulses.
9. When powered up, the transceiver is not ready to perform IR transmissions. The controller has to initialize the transceiver. The brief powered up sequences are:
   - 9.1. On power up, an internally generated signal in the transceiver sets the 3 control registers:
     - a) Control Register 0:
       - Bit 0: shutdown mode
       - Bit 1: RXD disabled
       - Bit 2: LED disabled
     - b) Control Register 1:
       - Bit 0-7: SIR mode
     - c) Control Register 2:
       - Bit 0-7: Power at 100% level
   - 9.2. The controller has to initialize the transceiver by:
     - a) Hold SWDAT low
     - b) Toggle SCLK for at least 30 cycles

The transceiver is in STC mode and ready to accept STC transactions.

Bus Timing Sample Waveforms

The following diagrams are sample waveforms for 2 byte write and read transactions and a 3 byte read transaction.

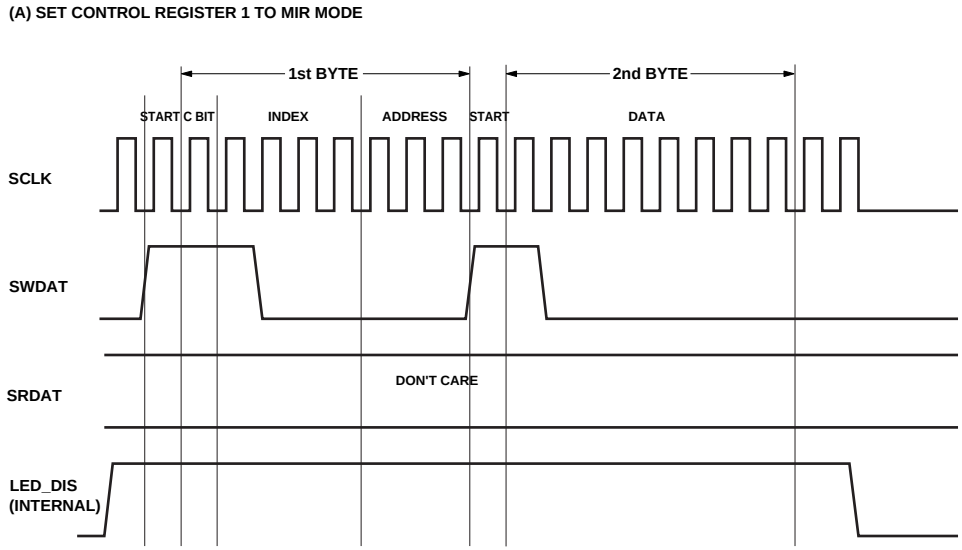


Figure 22. Write waveform – set control register 1 to MIR mode.

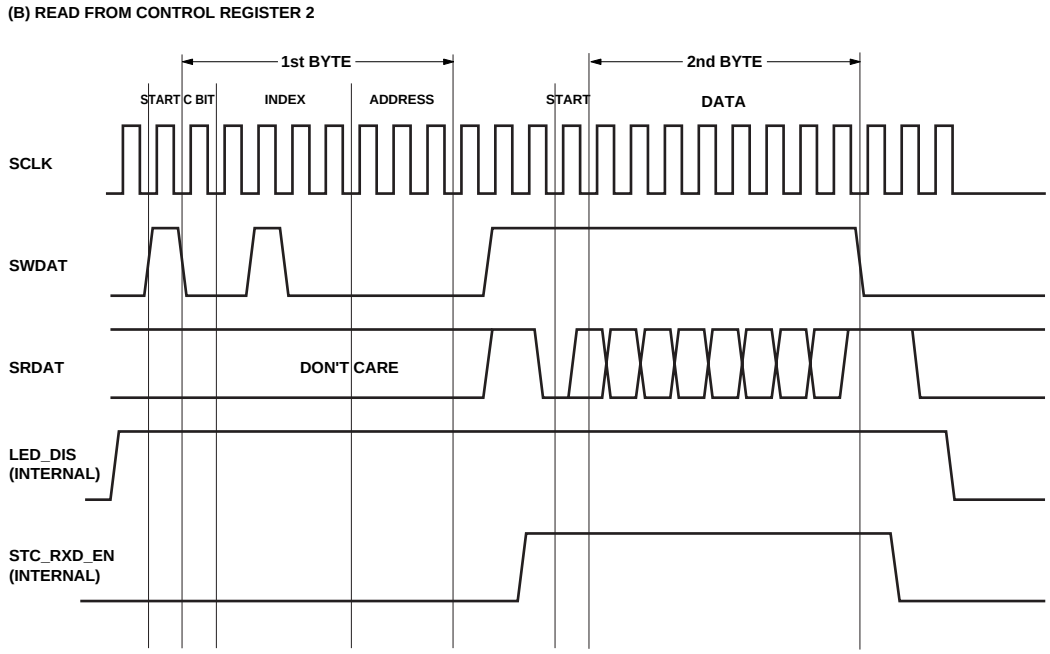


Figure 23. Read waveform – read from control register 2 (transmitter power level).

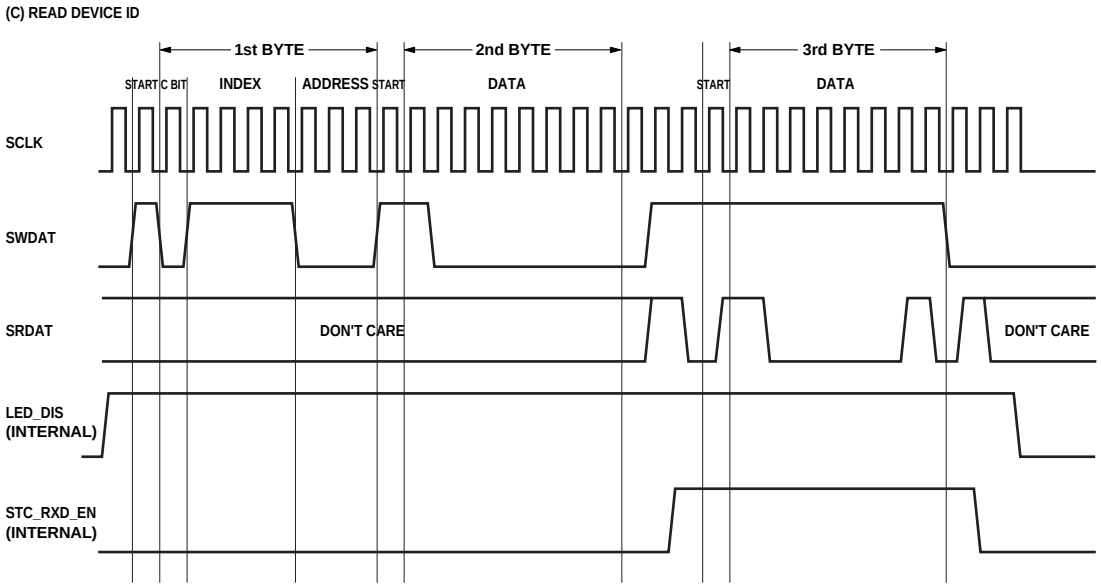


Figure 24. Extended index read waveform – read device ID.

Electrical Specifications

Timing specifications are given in the table and diagram below.

Symbol	Parameter	Min.	Max.	Units
tCKp	SCLK Clock Period	250	∞	ns
tCKh	SCLK Clock High Time	60		ns
tCKl	SCLK Clock Low Time	80		ns
tDOtv	Output Data Valid (from infrared controller)		40	ns
tDOth	Output Data Hold (from infrared controller)	0		ns
tDOrv	Output Data Valid (from optical transceiver)		40	ns
tDOrh	Output Data Hold (from optical transceiver)		40	ns
tDOrf	Line float Delay		60	ns
tDIs	Input Data Setup	10		ns
tDIh	Input Data Hold	5		ns

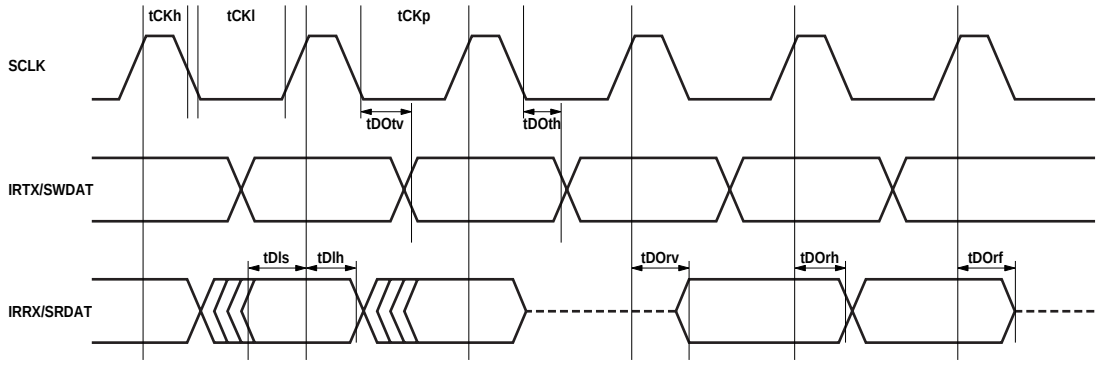


Figure 25. Timing diagram.

The link distance testing was done using typical HSDL-3210 units with National Semiconductor's PC87109 3V Super I/O controller and SMC's FDC37C669 and FDC37N769 Super I/O controllers. An IR link distance of up to 40 cm was demonstrated for SIR at full power. On the other hand, for MIR at full power, an IR link distance of up to 35 cm was demonstrated.

Appendix D: Optical port dimensions for HSDL-3210

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30˚ and the maximum size corresponds to a cone angle of 60˚.

In the figure below, X is the width of the window, Y is the height of the window, and Z is the distance from the HSDL-3210 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens, K, is 5.1 mm. The equations for computing the window dimensions are as follows:

$$X = K + 2*(Z + D)*\tan A$$

$$Y = 2*(Z + D)*\tan A$$

The above equations assume that the thickness of the window is negligible compared to the distance of the module from the back of the window (Z). If they are comparable, Z' replaces Z in the above equation. Z' is defined as:

$$Z' = Z + t/n$$

where ‘t’ is the thickness of the window and ‘n’ is the refractive index of the window material.

The depth of the LED image inside the HSDL-3210, D, is 3.17 mm. ‘A’ is the required half angle for viewing. For IrDA compliance, the minimum is 15˚ and the maximum is 30˚. Assuming the thickness of the window to be negligible, the equations result in the following tables and graphs.

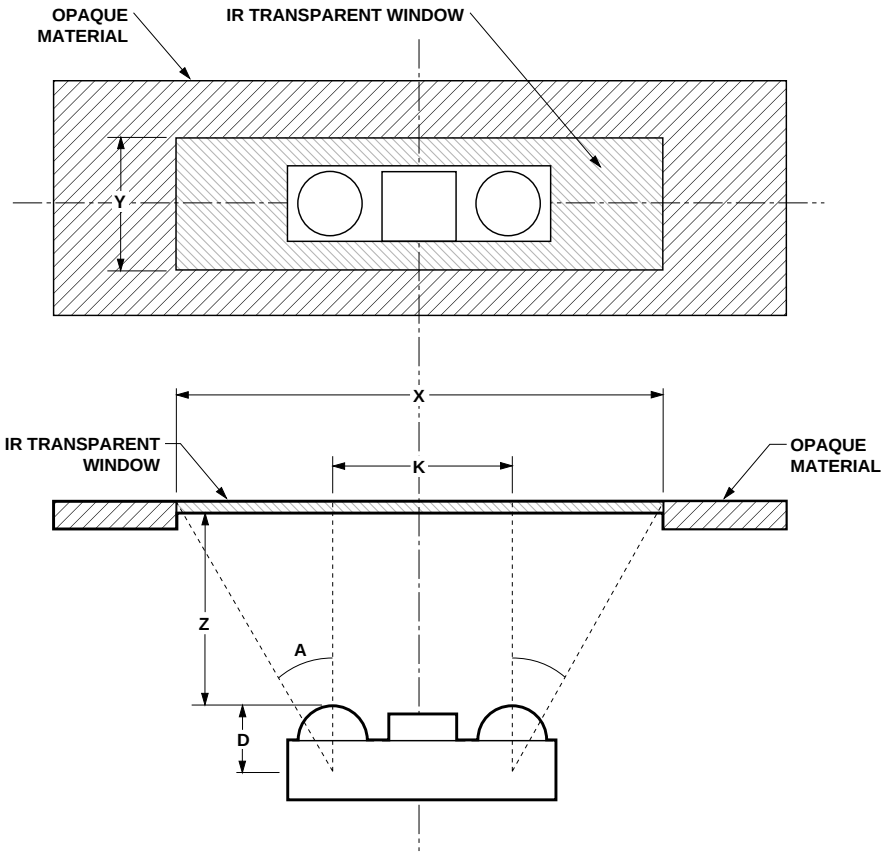


Figure 26. Window design diagram.

Module Depth	Aperture Width (x, mm)		Aperture Height (y, mm)	
(z) mm	Max.	Min.	Max.	Min.
0	8.76	6.80	3.66	1.70
1	9.92	7.33	4.82	2.33
2	11.07	7.87	5.97	2.77
3	12.22	8.41	7.12	3.31
4	13.38	8.94	8.28	3.84
5	14.53	9.48	9.43	4.38
6	15.69	10.01	10.59	4.91
7	16.84	10.55	11.74	5.45
8	18.00	11.09	12.90	5.99
9	19.15	11.62	14.05	6.52

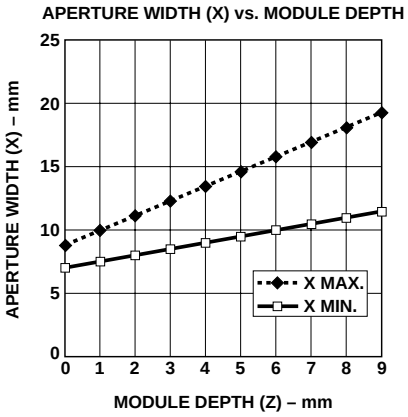


Figure 27. Aperture width (X) vs. module depth.

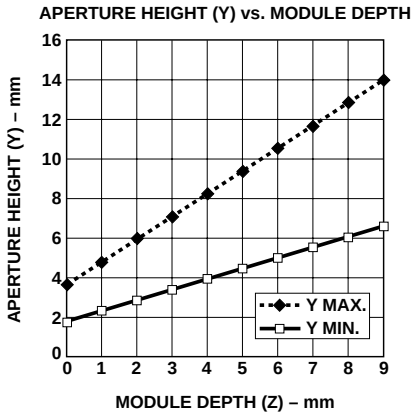


Figure 28. Aperture height (Y) vs. module depth.

Window Material

Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture. An IR filter dye may be used in the window to make it look black to the eye, but the total optical loss of the window should be 10% or less for best optical performance. Light loss should be measured at 875 nm.

The recommended plastic materials for use as a cosmetic window are available from General Electric Plastics.

Recommended Plastic Materials:

Material Number	Light Transmission	Haze	Refractive Index
Lexan 141L	88%	1%	1.586
Lexan 920A	85%	1%	1.586
Lexan 940A	85%	1%	1.586

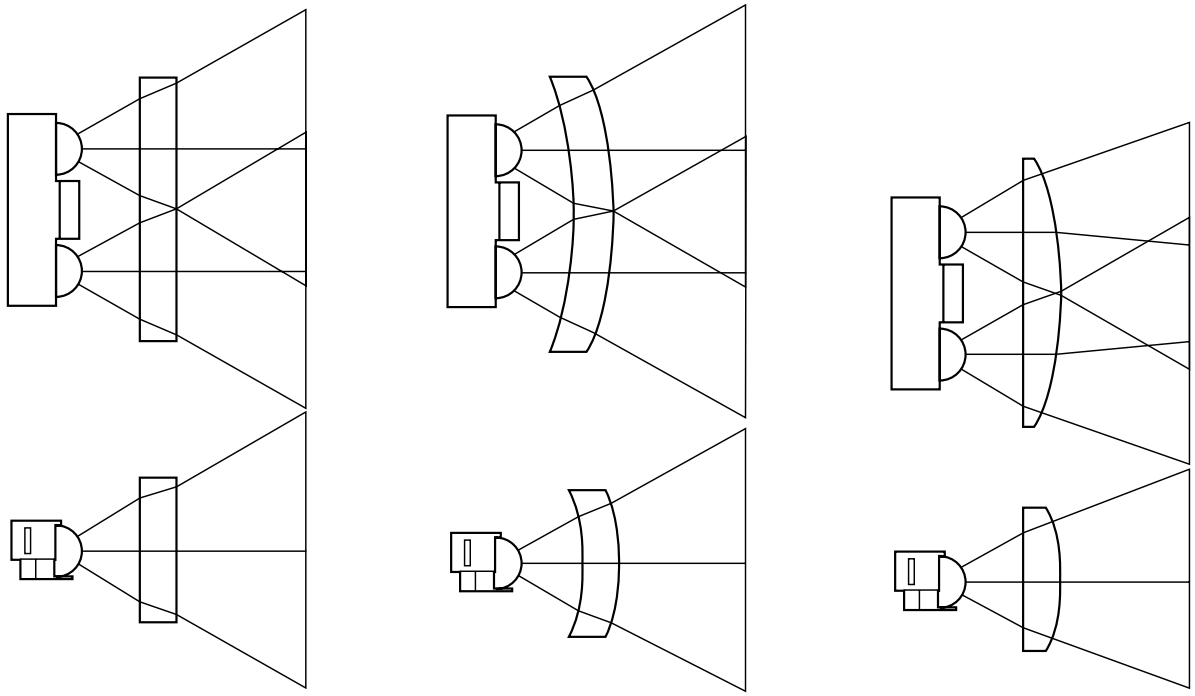
Note: 920A and 940A are more flame retardant than 141L.
Recommended Dye: Violet #21051 (IR transmissant above 625 nm).

Shape of the Window

From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

If the window must be curved for mechanical or industrial design reasons, place the same curve on the back side of the window that has an identical radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will significantly reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.



Flat Window (First Choice)

Curved Front and Back (Second Choice)

Curved Front, Flat Back (Do Not Use)

Figure 29. Shape of windows.

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