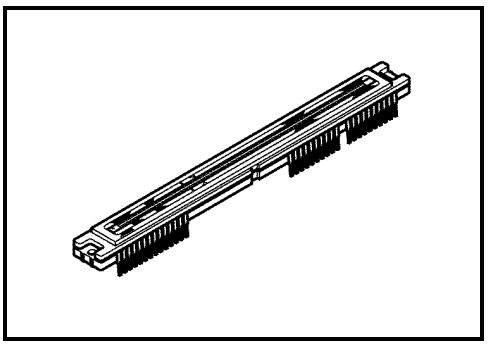
TOSHIBA CCD Linear Image Sensor CCD (Charge Coupled Device)

TCD2703D

The TCD2703D is a high sensitive and low dark current 7500 pixels × 3 line CCD color image sensor.
The sensor is designed for color scanner.
The device contains a row of 7500 pixels × 3 line photodiodes which provide a 24 lines/mm across a A3 size paper. The device is operated by 5-V pulse, and 12-V power supply.



Weight: 16.0 g (typ.)

Features

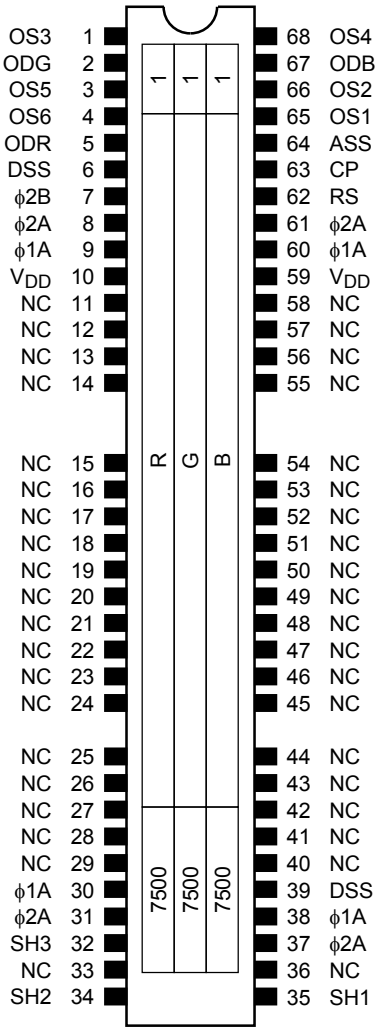
- Number of image sensing pixels
  : 22500 pixels (7500 pixels × 3 line)
- Image sensing pixels size
  : 9.325 μm by 9.325 μm on 9.325 μm center
- Photo sensing region: High sensitive pn photodiode
- Clock: 2-phase (5 V)
- Distance between photodiode array
  : Pixel R to pixel G: 37.3 μm (4 lines)
  Pixel G to pixel B: 37.3 μm (4 lines)
- Internal circuit: Clamp circuit
- Package: 68-pin CERDIP
- Color filter: Red, Green, Blue

Maximum Ratings (Note 1)

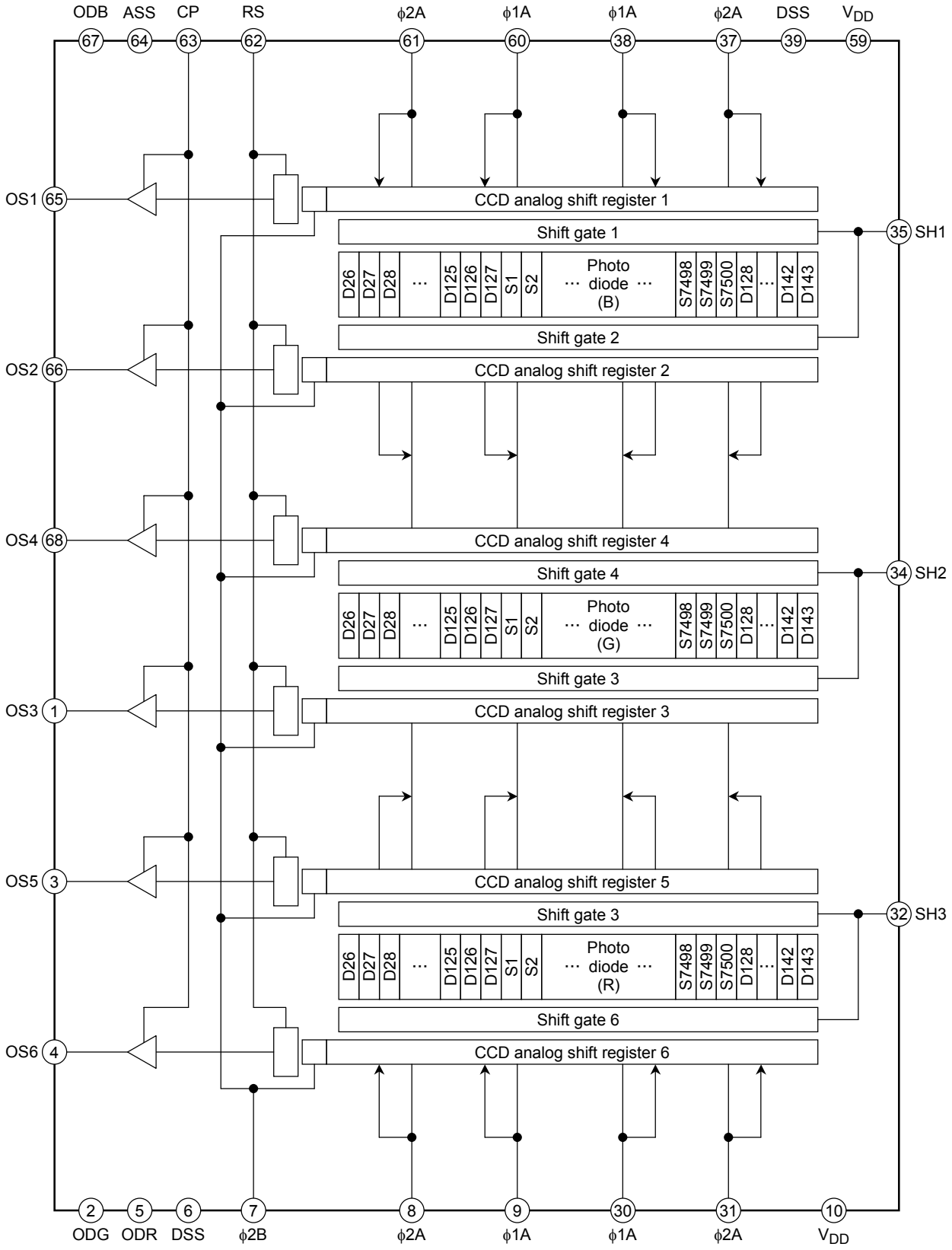
Characteristics	Symbol	Rating	Unit
Clock pulse voltage	$V_{\phi A}$	−0.3 to 8	V
Last stage clock pulse voltage	$V_{\phi B}$		
Shift pulse voltage	V_{SH}		
Reset pulse voltage	V_{RS}		
Clamp pulse voltage	V_{CP}		
Power supply voltage	V_{OD}, V_{DD}	−0.3 to 15	V
Operating temperature	T_{opr}	0 to 60	°C
Storage temperature	T_{stg}	−25 to 85	°C

Note 1: All voltages are with respect to SS pins (ground).

Pin Connections (top view)



Circuit Diagram



Pin Names

Pin No.	Symbol	Name	Pin No.	Symbol	Name
1	OS3	Output signal 3 (green)	35	SH1	Shift gate 1
2	ODG	Power supply (green)	36	NC	No connect
3	OS5	Output signal 5 (red)	37	ϕ2A	Transfer clock (phase 2)
4	OS6	Output signal 6 (red)	38	ϕ1A	Transfer clock (phase 1)
5	ODR	Power supply (red)	39	DSS	Ground (digital)
6	DSS	Ground (digital)	40	NC	No connect
7	ϕ2B	Last stage clock (phase 2)	41	NC	No connect
8	ϕ2A	Transfer clock (phase 2)	42	NC	No connect
9	ϕ1A	Transfer clock (phase 1)	43	NC	No connect
10	V_{DD}	Power supply (digital)	44	NC	No connect
11	NC	No connect	45	NC	No connect
12	NC	No connect	46	NC	No connect
13	NC	No connect	47	NC	No connect
14	NC	No connect	48	NC	No connect
15	NC	No connect	49	NC	No connect
16	NC	No connect	50	NC	No connect
17	NC	No connect	51	NC	No connect
18	NC	No connect	52	NC	No connect
19	NC	No connect	53	NC	No connect
20	NC	No connect	54	NC	No connect
21	NC	No connect	55	NC	No connect
22	NC	No connect	56	NC	No connect
23	NC	No connect	57	NC	No connect
24	NC	No connect	58	NC	No connect
25	NC	No connect	59	V_{DD}	Power supply (digital)
26	NC	No connect	60	ϕ1A	Transfer clock (phase 1)
27	NC	No connect	61	ϕ2A	Transfer clock (phase 2)
28	NC	No connect	62	RS	Reset gate
29	NC	No connect	63	CP	Clamp gate
30	ϕ1A	Transfer clock (phase 1)	64	ASS	Ground (analog)
31	ϕ2A	Transfer clock (phase 2)	65	OS1	Output signal 1 (blue)
32	SH3	Shift gate 3	66	OS2	Output signal 2 (blue)
33	NC	No connect	67	ODB	Power supply (blue)
34	SH2	Shift gate 2	68	OS4	Output signal 4 (green)

Optical/Electrical Characteristics (bit clamp)

(Ta = 25°C, V_{OD} = V_{DD} = 11 V, V_ϕ = V_{RS} = V_{SH} = V_{CP} = 5 V (pulse), f_ϕ = 1 MHz, load resistance = 100 kΩ, t_{INT} (integration time) = 10 ms, light source = A light source + CM500S filter (t = 1.0 mm))

Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	Red	R (R)	7.9	11.4	14.9	V/lx·s	(Note 2)
	Green	R (G)	10.7	15.4	20.1		
	Blue	R (B)	4.2	6.1	8.0		
Photo response non uniformity		PRNU (1)	—	10	20	%	(Note 3)
		PRNU (3)	—	3	12	mV	(Note 4)
Saturation output voltage		V_{SAT}	1.0	1.5	—	V	(Note 5)
Saturation exposure		SE	0.05	0.1	—	lx·s	(Note 6)
Dark signal voltage		V_{DRK}	—	3	6	mV	(Note 7)
Dark signal non uniformity		DSNU	—	8	12	mV	(Note 8)
Dc power dissipation		P_D	—	900	1300	mW	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z_O	—	0.2	0.5	kΩ	—
Dc signal output voltage		V_{OS}	4.5	6.0	7.5	V	(Note 9)
Random noise		$N_{D\sigma}$	—	1.0	—	mV	(Note 10)

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

$$\text{PRNU (1)} = \frac{\Delta X}{\overline{X}} \times 100\ (\%)$$

$\overline{X}$: Average of total signal outputs
ΔX: The maximum deviation from $\overline{X}$.

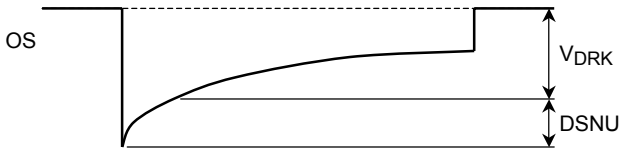
Note 4: PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (typ.).

Note 5: V_{SAT} is defined as minimum Saturation Output voltage of all effective pixels.

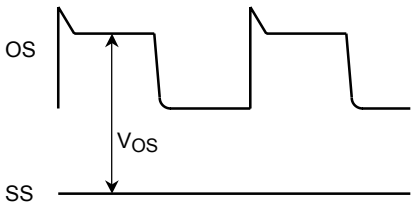
Note 6: Definition of SE: $\text{SE} = \frac{V_{SAT}}{RG}$

Note 7: V_{DRK} is defined as average dark signal voltage of all effective pixels.

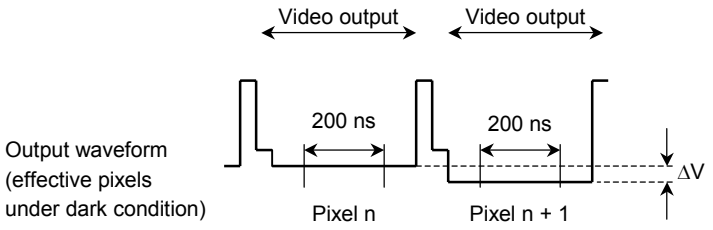
Note 8: DSNU is defined by the difference between average value (V_{DRK}) and the maximum value of the dark voltage.



Note 9: DC signal output voltage is defined as follows :



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark condition) calculated by the following procedure.



(1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.

(2) Each of the output levels at video output periods averaged over 200 nanosecond period to get Vn and Vn + 1.

(3) Vn + 1 is subtracted from Vn to get ΔV.

$$\Delta V = Vn - Vn + 1$$

(4) The standard deviation of ΔV is calculated after procedure (2) and (3) are repeated 30 times (30 readings).

$$\Delta V = \frac{1}{30}\sum_{i=1}^{30} |\Delta Vi| \qquad \sigma = \sqrt{\frac{1}{30}\sum_{i=1}^{30}(|\Delta V_i| - \overline{\Delta V})^2}$$

(5) Procedure (2), (3) and (4) are repeated 10 times to get 10 sigma values.

$$\overline{\sigma} = \frac{1}{10}\sum_{j=1}^{10}\sigma_j$$

(6) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify the random noise as follows.

$$\text{Random noise} = \frac{1}{\sqrt{2}}\overline{\sigma}$$

Operating Condition (Ta = 25°C)

Characteristics		Symbol	Min	Typ.	Max	Unit
Clock pulse voltage	High level	$V_{\phi 1A}$, $V_{\phi 2A}$	4.5	5.0	5.5	V
	Low level		0	—	0.3	
Final stage clock pulse voltage	High level	$V_{\phi 2B}$	4.5	5	5.5	V
	Low level		0	—	0.3	
Shift pulse voltage (Note 11)	High level	V_{SH}	V_ϕ "H" − 0.5	V_ϕ "H"	V_ϕ "H"	V
	Low level		0	—	0.3	
Reset pulse voltage	High level	V_{RS}	4.5	5	5.5	V
	Low level		0	—	0.3	
Clamp pulse voltage	High level	V_{CP}	4.5	5	5.5	V
	Low level		0	—	0.3	
Power supply voltage		V_{OD}, V_{DD}	10.5	11.0	13.0	V

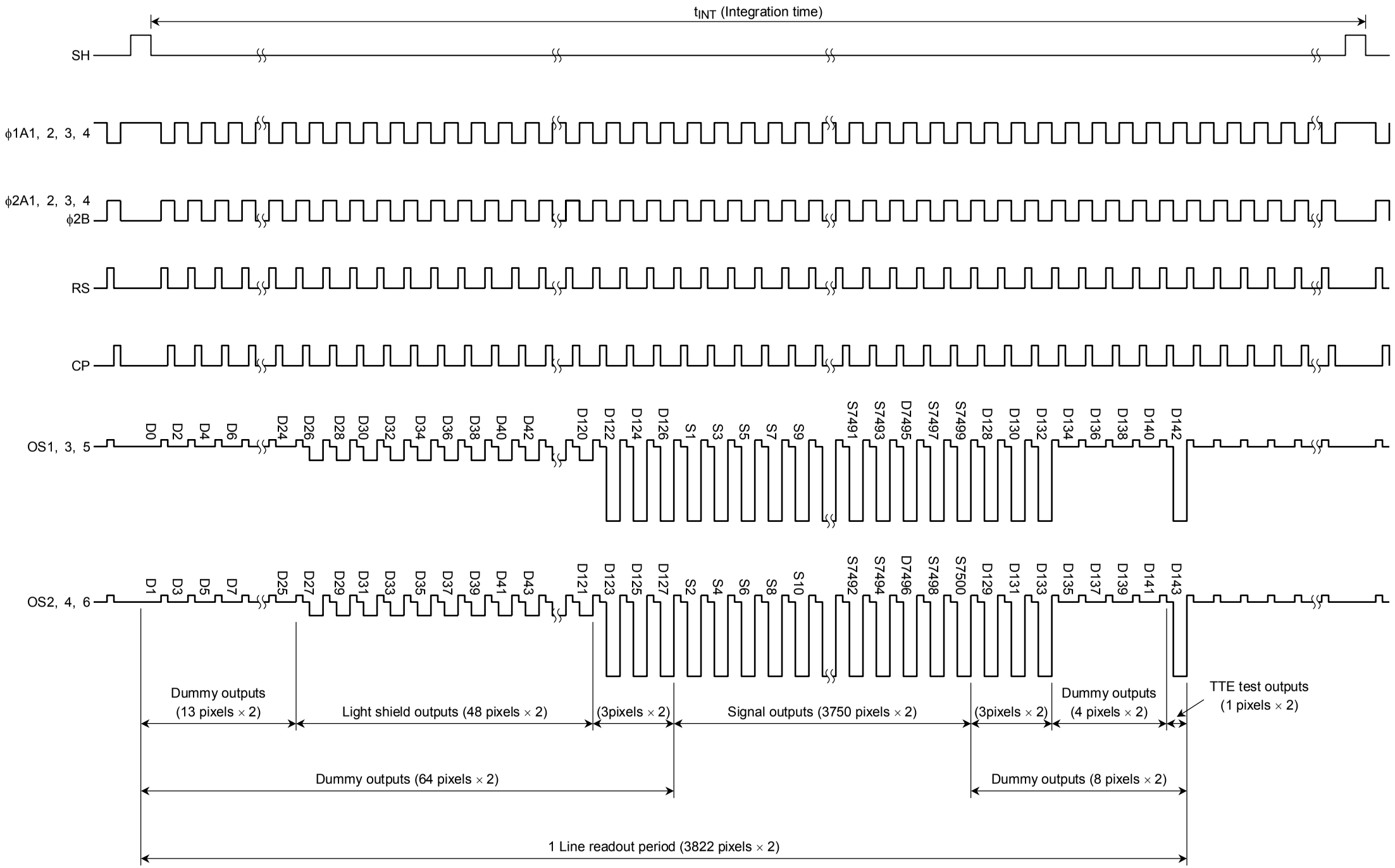
Note 11: V_ϕ "H" means the high level voltage of $V_{\phi A}$ when SH pulse is high level.

Clock Characteristics (Ta = 25°C)

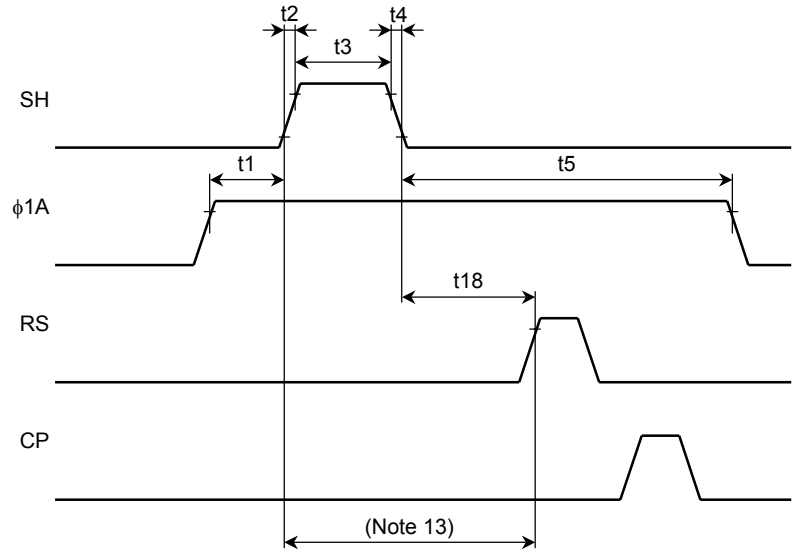
Characteristics	Symbol	Min	Typ.	Max	Unit
Clock pulse frequency	f_ϕ	—	1	25	MHz
Reset pulse frequency	f_{RS}	—	1	25	MHz
Clamp pulse frequency	f_{CP}	—	1	25	MHz
Clock capacitance (Note 12)	$C_{\phi A}$	—	150	—	pF
Final stage clock capacitance	$C_{\phi B}$	—	20	—	pF
Shift gate capacitance	C_{SH}	—	40	—	pF
Reset gate capacitance	C_{RS}	—	20	—	pF
Clamp gate capacitance	C_{CP}	—	20	—	pF

Note 12: V_{OD} = 11 V

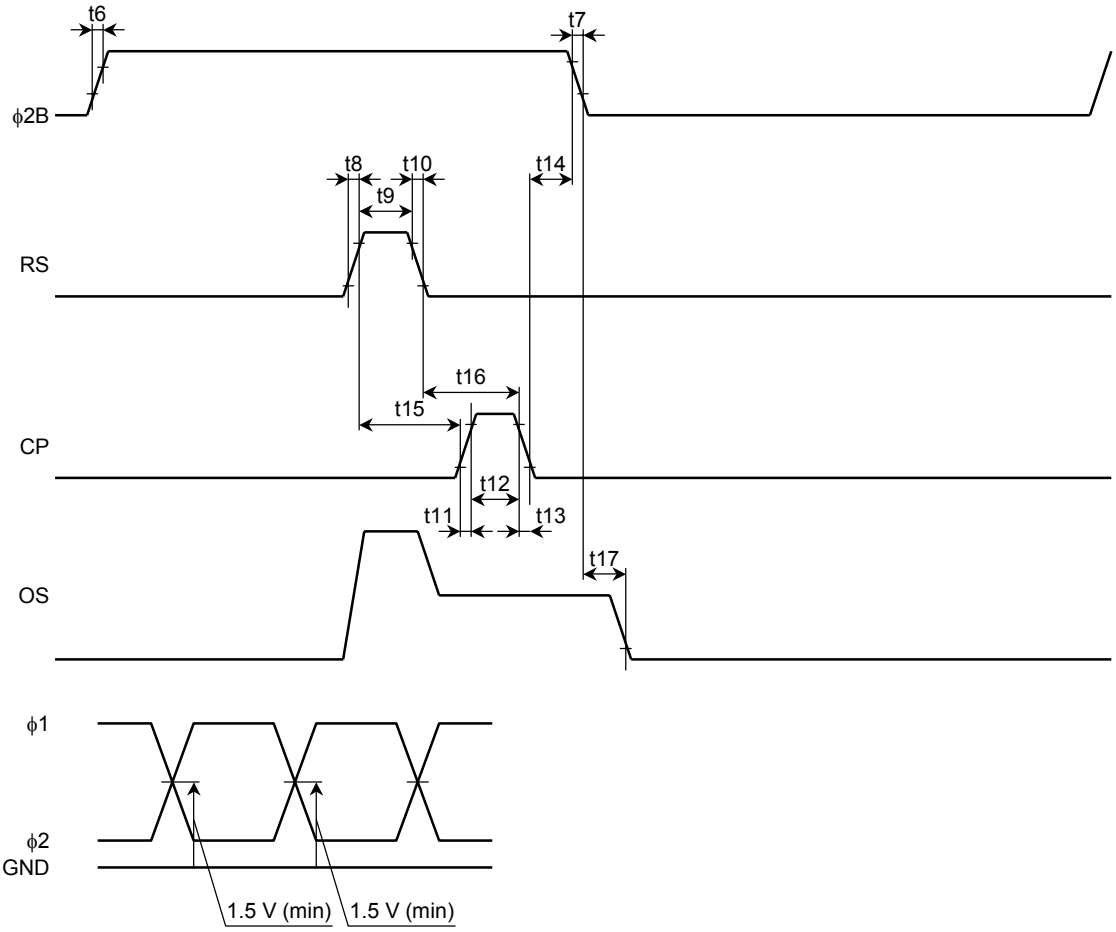
Timing Chart



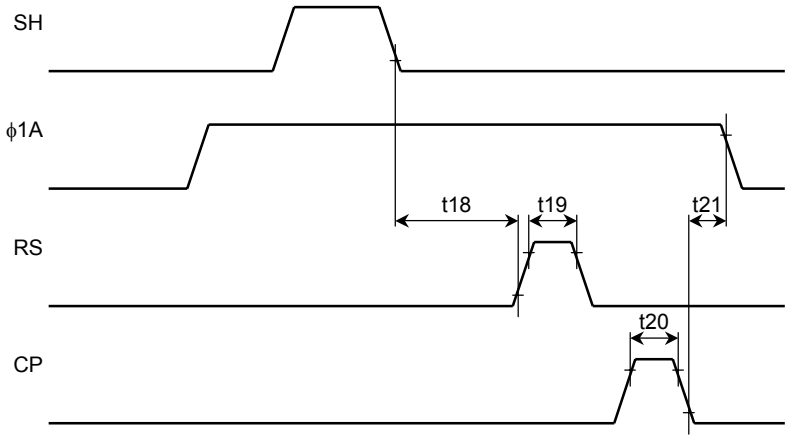
Timing Requirements



Note 13: Hold the RS and CP pins at low during this period.



Timing Requirements (line clamp)

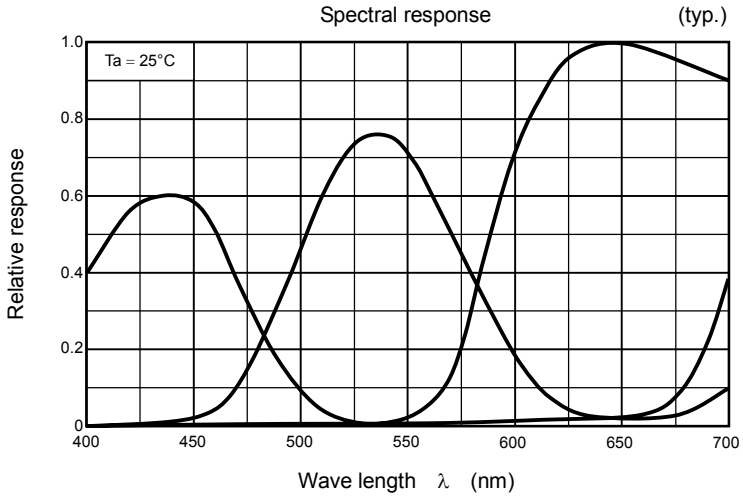


Characteristics	Symbol	Min	Typ. (Note 14)	Max	Unit
Pulse timing of SH and ϕ1A	t1	60	1000	—	ns
	t5	300	1000	—	ns
SH pulse rise time, fall time	t2, t4	0	50	—	ns
SH pulse width	t3	1000	2000	—	ns
ϕ1, ϕ2 Pulse rise time, fall time	t6, t7	0	50	—	ns
RS pulse rise time, fall time	t8, t10	0	20	—	ns
RS pulse width	t9	10	100	—	ns
CP pulse rise time, fall time	t11, t13	0	20	—	ns
CP pulse width	t12	10	100	—	ns
Pulse timing of ϕ2B and CP	t14	0	40	—	ns
Pulse timing of RS and CP	t15	0	0	—	ns
	t16	10	100	—	ns
Video data delay time (Note 15)	t17	—	10	—	ns
SH, RS pulse timing	t18	300	—	—	ns
RS pulse width (line clamp)	t19	10	—	—	ns
CP pulse width (line clamp)	t20	10	—	—	ns
CP, ϕ1A pulse timing (line clamp)	t21	5	—	—	ns

Note 14: Measured with f_{RS} = 1 MHz.

Note 15: Load resistance is 100 kΩ.

Typical Spectral Response



Caution

1. Electrostatic Breakdown

The dust and stain on the glass window of the package degrade optical performance of CCD sensor. Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
c. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
   It is not necessarily required to execute all precaution items for static electricity.
   It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

2. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor. Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

3. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

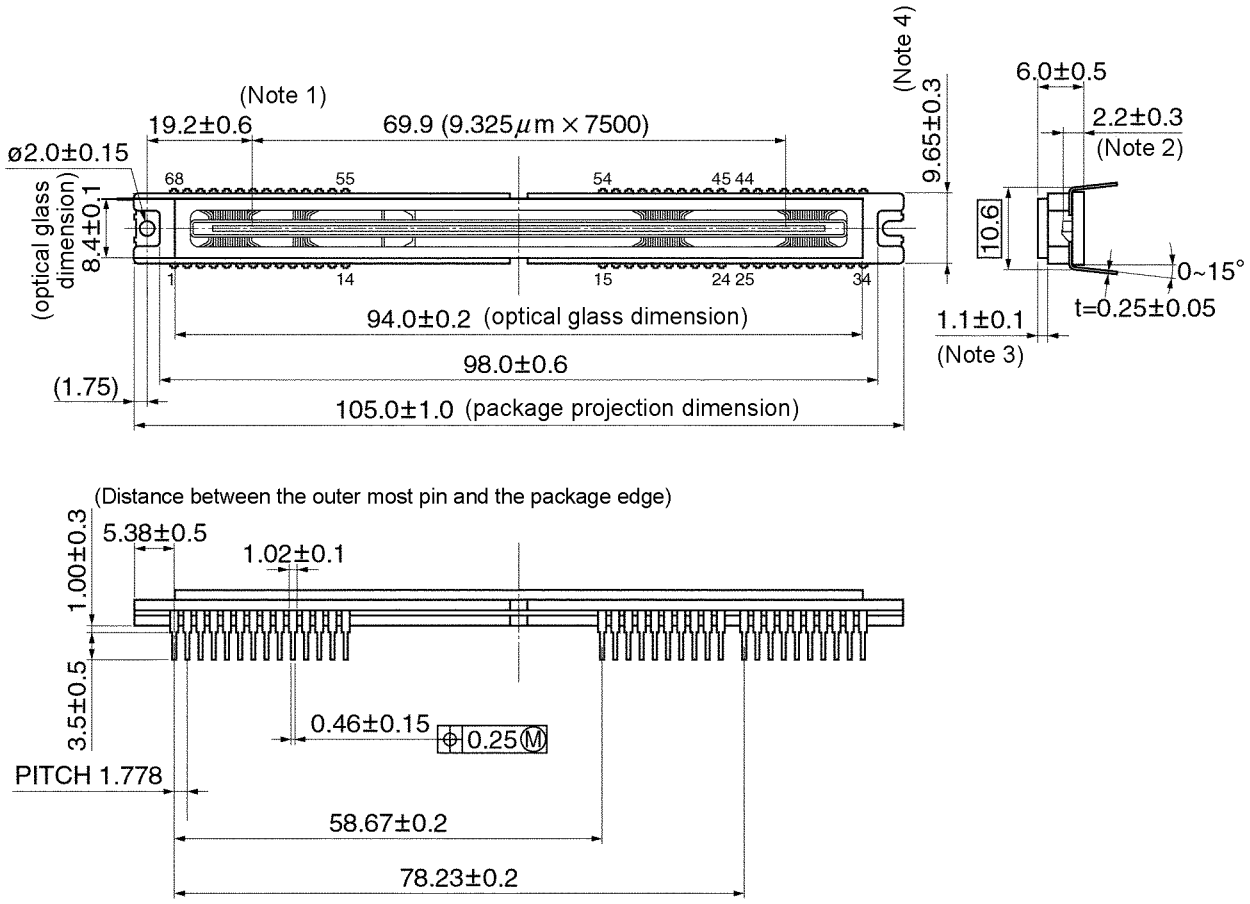
4. Mounting on a PCB

This package is sensitive to mechanical stress.
Toshiba recommends using IC inserters for mounting, instead of using lead forming equipment.

5. Soldering

Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.
Using a soldering iron, complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

Package Dimensions



Note 1: Distance between the center of the hole and the first pixel (S1)
Note 2: Distance between the of the chip and bottom of the package.
Note 3: Glass thickness (n = 1.5)
Note 4: Dimensional tolerance is ±0.3 mm for the 10-mm range from each ceramic edge, ±0.4 mm for the 10-mm to 27-mm range and ±0.5 mm for the inner range.

Weight: 16.0 g (typ.)

RESTRICTIONS ON PRODUCT USE

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