Target Specification

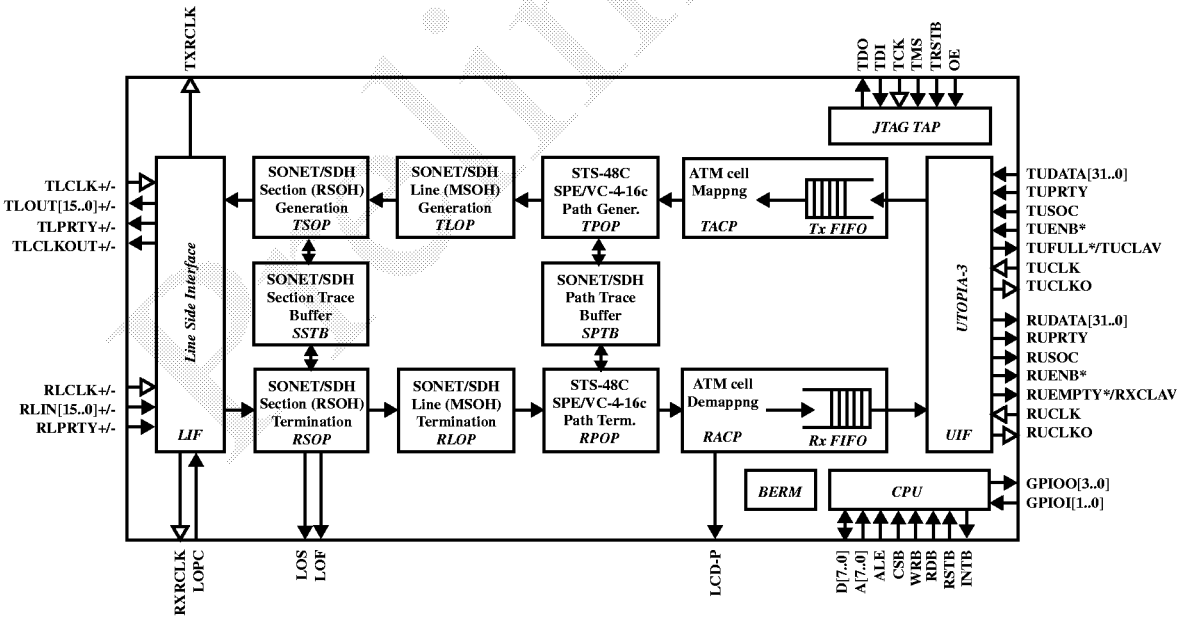
VSC9110

STS-48 Physical Layer
ATM UNI/NNI Device

Features

- STS-48c ATM Framing Device for User Network Interface and Network Node Interface Applications
- STS-48c / STM-16c Support. Terminates and Generates SONET/SDH Section, Line, and Path Layers
- UTOPIA-3 Interface
- 16 bit PECL Interface to High-speed MUX/ DEMUX Transceivers
- Generic 8-bit Microprocessor Interface
- +3.3V Power Supply
- +5V Tolerant TTL I/O
- Compliant with SONET and SDH Requirements as Stated in ANSI T1.105, Bellcore GR-253-CORE and ITU-T G.707 Documents
- 0.35 Micron CMOS Technology
- Thermally Enhanced 256 BGA Package
- Provides JTAG TAP Controller Conforming to the IEEE 1149.1 Standard

VSC9110 Block Diagram



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Functional Overview

The VSC9110 is an ATM over SONET framing device that can be used in equipment interconnecting ATM switches over public or private SONET/SDH networks. When used in conjunction with a high-speed MUX/DEMUX transceiver, the device provides a complete physical layer solution for ATM over SONET at the OC-48 rate. By using this device, highly integrated OC-48 single line card solutions can be developed. The basic features of the receive and transmit datapaths along with features of other interfaces are listed below.

Receive Datapath:

- Performs framing on the A1 and A2 bytes. Supports 12 bit, 24 bit and 48 bit wide A1 A2 framing patterns
- Generates OOF, LOF and LOS status alarms
- Performs SONET descrambling
- Monitors and extracts section overhead bytes B1 and J0. The section trace messages are extracted and checked for persistency and mismatch and provides accumulating counters
- Monitors and extracts line overhead bytes B2, K1, K2, S1 and M1. Detects AIS-L and RDI-L and performs persistency checking and provides accumulating counters
- Monitors and extracts path overhead bytes J1, B3, C2 and G1. The path trace messages are extracted and checked for persistency and mismatch and provides accumulating counters
- Performs H1 H2 pointer interpretation and locates the position of the SPE
- Performs ATM cell delineation with OCD and LCD detection
- ATM cell filtering, payload descrambling, performance monitor counters and HEC correction/error detection
- Provides an eight ATM cell deep FIFO and detects FIFO overflow/underflow
- Presents the ATM cells on the UTOPIA-3 interface

Transmit Datapath:

- Provides eight cell deep ATM cell FIFO. Detects FIFO overflow
- ATM cell rate adaptation with Idle/Unassigned cells
- ATM cell payload scrambling and performance monitoring counters
- SPE generation with insertion of J1 (section trace message), B2, C2 and G1
- Backreporting functions for the REI-P and RDI-P (G1 byte)
- Pointer H1 H2 insertion and diagnostic function for pointer increment/decrement
- Line overhead generation by inserting B2, K1, K2, S1 and M1 and insertion of AIS-L and RDI-L
- Backreporting function for B2 byte
- Section overhead generation by inserting A1 A2 and J0/Z0 bytes
- Performs SONET scrambling

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Line Interface:

- Differential PECL IO running at 155.52 MHz
- Two 16 bit unidirectional busses, one for transmitting and one for receiving data to/from the front-end MUX/DEMUX
- Provides parity bits and looped clock in Tx path

CPU and Test Interface

- Generic microprocessor (CPU) interface used for device configuration, status and performance information extraction and test mode operations
- 8 bit data bus and 8 bit address bus
- Interrupt pin
- General Purpose IOs
- Standard 5 pin JTAG Test Access Port

UTOPIA Interface

- 32 bit databus
- 100MHz operation (max)
- 52/56 ATM cell byte format
- Cell- and word-level flow control
- Programmable "latency in" flow control flags
- Flow control algorithm supports operation as defined in UTOPIA-1/2 and SCI-PHY

Diagnostic Functions

- Line loopback mode. The incoming data on the line interface is looped back to the outgoing line interface
- Equipment loopback. The internal generated SONET frames are looped back to the receive path internally
- UTOPIA loopback. The ATM cell stored in the Tx ATM cell FIFO are looped directly to the receiver ATM cell FIFO
- Various diagnostic functions for testing of the SONET/SDH overhead bytes
- Bit Error rate monitor with two programmable thresholds

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Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND ..... -0.5V to +4V
Power Supply Voltage (V_{DD5}) Potential to GND ..... -0.5V to +6V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} + 0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to V_{DD5} + 0.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 0.5V
DC Output Voltage (TTL 5V Tolerant Outputs) ..... -0.5V to V_{DD5} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55° to +125°C
Storage Temperature ..... -65°C to +150°C
Maximum Input ESD (Human Body Model) ..... 2000 V

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) ..... +3.3V ±10%
Power Supply Voltage (V_{DD5}) ..... +5.0V ±10%
Operating Temperature Range* (T) ..... -40° to 85°C

** Lower limit of specification is ambient temperature and upper limit is case temperature.*

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DC Characteristics

Table 1: TTL and PECL Inputs and Outputs

Parameters	Description	Min	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	V	I_{OH} = -2,-4,-12,-16 mA
V_{OL}	Output LOW voltage (TTL)	—	0.5	V	I_{OL} = 2,4,12,16 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	5.5	V	—
V_{IL}	Input LOW voltage (TTL)	0	0.8	V	—
I_{IT}	Input current (TTL)	—	10	µA	$0V < V_{IN} < 5V$
V_{OD50}	Differential output swing (PECL)	0.800	1.200	V	50Ω to V_{DD} - 2.0V
V_{OH50}	Output HIGH voltage (PECL)	V_{DD} - 1.050	V_{DD} - 0.750	V	50Ω to V_{DD} - 2.0V
V_{OL50}	Output LOW voltage (PECL)	V_{DD} - 1.950	V_{DD} - 1.850	V	50Ω to V_{DD} - 2.0V
V_{OD75}	Differential output swing (PECL)	1.050	1.450	V	75Ω to V_{DD} - 2.0V
V_{OH75}	Output HIGH voltage (PECL)	V_{DD} - 0.850	V_{DD} - 0.550	V	75Ω to V_{DD} - 2.0V
V_{OL75}	Output LOW voltage (PECL)	V_{DD} - 2.0000	V_{DD} - 1.900	V	75Ω to V_{DD} - 2.0V
V_{ID}	Required diff. input voltage (PECL)	0.300	—	V	—
V_{IH}	Input HIGH voltage (PECL)	V_{DD} - 1.32	V_{DD}	V	—
V_{IL}	Input LOW voltage (PECL)	0.0	V_{IH} - 0.300	V	—
I_{IP}	Input current (PECL)	-1000	1000	µA	$0V < V_{IN} < 3.3V$

NOTE: Negative current flow into the device (sinking), positive currents flow out of the device (sourcing)

Power Dissipation

Table 2: Power Supply Currents

Parameter	*Description*	*(Max)*	*Units*
I_{DD}	Power supply current from V_{DD}	830	mA
P_D	Power dissipation	3.0	W

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Package Pin Definitions

Pin	*Name*	*I/O*	*Freq Type*	*Description*
RLIN[15:0]+/ RLIN[15:0]-	Parallel Line Receive Data.	I	78MHz PECL	This parallel data bus carries the incoming STS-48c/ STM-4-16c data stream. RLIN[15] is the most significant bit and RLIN[0] is the least significant bit. RLIN[15] is the first arriving bit on the serial data stream. RLIN[15:0] is sampled on the rising edge of RLCLK+.
RLCLK+/ RLCLK-	Parallel Line Receive Clock.	I	155MHz PECL	The clock reference for the 2.5Gb/s receive flow carried in RLIN[15:0]. The clock frequency is nominally 155.52MHz equivalent to STS-48c/ STM-4-16c operation.
RLPRTY+/ RLPRTY-	Parallel Line Receive Parity.	I	78MHz PECL	This input carries the even/odd parity over the parallel data input (RLIN[15:0]+). RLPRTY is sampled on the rising edge of RLCLK+.
TLOUT[15:0]+ /TLOUT[15:0]-	Parallel Line Transmit Data.	O	78MHz PECL	This parallel data bus carries the outgoing STS-48c/ STM-4-16c data stream. TLOUT[15] is the most significant bit and TLOUT[0] is the least significant bit. TLOUT[15] is the first transmitted bit on the serial data stream. TLOUT[15:0] is generated on the rising edge of the incoming TLCLK+.
TLCLK+/ TLCLK-	Parallel Line Transmit Clock.	O	155MHz PECL	The clock reference for the 2.5Gb/s transmit flow carried in TLOUT[15:0]. The clock frequency is nominally 155.52MHz equivalent to STS-48c/ STM-4-16c operation.
TLCLKOUT+/ TLCLKOUT-	Looped Parallel Line Transmit Clock.	O	155MHz PECL	This signal is the looped TLCLK signal. The timing for the clock is defined with reference to the TLOUT data bus signals. The clock frequency is nominally 155.52MHz equivalent to STS-48c/ STM-4-16c operation.
TLPRTY+/ TLPRTY-	Parallel Line Transmit Parity.	O	78MHz PECL	This signal carries the even/odd parity over the parallel data output (TLOUT[15:0]+). TLPRTY is generated on the rising edge of TLCLK+.
RXRCLK	Receive Reference Clock.	O	78MHz TTL	This output is a reference clock derived directly from RLCLK in a 78MHz/38MHz/19MHz/8kHz version
TXRCLK	Transmit Reference Clock.	O	78MHz TTL	This output is a reference clock derived directly from TLCLK in a 78MHz/38MHz/19MHz/8kHz version
RUDATA[31:0]	Receive UTOPIA data.	O	50MHz TTL	Four-octet wide data driven from PHY to ATM layer. RUDATA[31] is the MSB.
RUPRTY	Receive UTOPIA parity.	O	50MHz TTL	RUPRTY is the odd/even (programmable, default odd) parity for RUDATA[31:0]. To support multiple PHY configurations.
RUSOC	Receive UTOPIA Start Of Cell.	O	3.5MHz TTL	Active high signal asserted by the PHY layer when RUDATA contains the first valid byte of a cell. To support multiple PHY configurations.
$\overline{\text{RUEMPTY}}$/ RUCLAV	Empty/Cell Available.	O	3.5MHz TTL	For UTOPIA flow control. The $\overline{\text{RUEMPTY}}$ definition applies to word level flow control, and RUCLAV definition applies to cell level flow control.
RUCLKO	Receive UTOPIA Clock Out	O	100MHz TTL	The RUCLK looped back out.

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Pin	*Name*	*I/O*	*Freq Type*	*Description*
RUCLK	Receive UTOPIA Clock	I	100MHz TTL	Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on RUDATA.
$\overline{\text{RUENB}}$	Receive UTOPIA Enable	I	3.5MHz TTL	Active low signal asserted by the ATM layer to indicate that RUDATA, RUSOC and RXPRTY will be sampled at the end of the next cycle. In MPHY configurations. $\overline{\text{RUENB}}$ is used to tri-state RUDATA, RUSOC and RUPRTY PHY layer outputs
TUDATA[31:0]	Transmit UTOPIA Data	I	50MHz TTL	Four-octet true data driven from ATM to PHY layer. TUDATA[31] is MSB.
TUCLK	Transmit UTOPIA Clock	I	100MHz TTL	Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on TUDATA.
TUPRTY	Transmit UTOPIA Parity	I	50MHz TTL	TUPRTY is the odd/even (programmable, default odd) parity bit over TUDATA[31:0], driven by the ATM layer. The signal is only valid when asserted simultaneously with $\overline{\text{TUENB}}$.
TUSOC	Transmit UTOPIA Start Of Cell.	I	3.5MHz TTL	Active high signal asserted by the ATM layer when TUDATA contains the first valid byte of the cell. The signal is only valid when asserted simultaneously with $\overline{\text{TUENB}}$.
$\overline{\text{TUENB}}$	Transmit UTOPIA Enable	I	3.5MHz TTL	Active low signal asserted by the ATM layer during cycles when TUDATA contains valid cell data.
TUCLKO	Transmit UTOPIA Clock Out	O	100MHz TTL	The TUCLK input looped back out.
$\overline{\text{TUFULL}}$/ TUCLAV	Full/Cell Available.	O	3.5MHz TTL	For UTOPIA flow control. The $\overline{\text{TUFULL}}$ definition applies to word level flow control, and TUCLAV definition applies to cell level flow control.
D[7:0]	Data Bus	B	7.0MHz TTL	This bidirectional data bus is used to transfer data for microcontroller read/write access to internal UNI registers.
A[7:0]	Address Bus	I	7.0MHz TTL	This address bus selects specific internal registers during register read/write access.
ALE	Address Latch Enable	I	7.0MHz TTL	This signal controls internal latching of the address bus signals. When low the address bus A[7:0] is latched internal. When high the internal address bus latches are transparent. This signal will allow for interfacing to a multiplexed address/ data bus. The ALE signal has an internal pull-up resistor.
$\overline{\text{CSB}}$	Chip Select signal	I	7.0MHz TTL	This signal (active low) must always be asserted during register read/write access cycles. The $\overline{\text{CSB}}$ signal is used in conjunction with either the $\overline{\text{RDB}}$ or the $\overline{\text{WRB}}$ signal. The $\overline{\text{CSB}}$ signal has an internal pull-up resistor.
$\overline{\text{WRB}}$	Write Signal	I	7.0MHz TTL	This signal (active low) is used for register write operations. The D[7:0] value is written into the register selected by A[7:0] when $\overline{\text{WRB}}$ and $\overline{\text{CSB}}$ are both asserted (low). The $\overline{\text{WRB}}$ signal has an internal pull-up resistor.
$\overline{\text{RDB}}$	Read Signal	I	7.0MHz TTL	This signal (active low) is used for register read operations. The content of the register selected by A[7:0] is driving D[7:0] when $\overline{\text{RDB}}$ and $\overline{\text{CSB}}$ are both asserted (low). The $\overline{\text{RDB}}$ signal has an internal pull-up resistor.

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Pin	*Name*	*I/O*	*Freq Type*	*Description*
$\overline{\text{RSTB}}$	Reset Signal	I	<1MHz TTL	This signal (active low) provides (asynchronous) reset of the UNI device. The device is held in a reset state while the $\overline{\text{RSTB}}$ signal is low. All outputs are tri-state when RSTB is asserted. All outputs are tri-state when $\overline{\text{RSTB}}$ is asserted.
$\overline{\text{INTB}}$	Interrupt Signal	O	7.0MHz TTL	This signal (active low) is asserted when an internal interrupt source is pending and the interrupt is unmasked (enabled). The $\overline{\text{INTB}}$ signal is negated when the interrupt pending bits have been cleared. The $\overline{\text{INTB}}$ is an open drain signal.
GPIOO[3:0]	General Purpose Outputs	O	<1MHz TTL	These general purpose outputs are programmable via internal CPU registers.
GPIOI[1:0]	General Purpose Inputs	I	<1MHz TTL	These general purpose inputs are accessible via internal status registers.
LOS	Loss Of Signal	O	<1MHz TTL	This is a status signal indicating if Loss Of Signal (LOS) has been detected. The LOS status is also available in an internal status register bit.
LOF	Loss Of Frame	O	<1MHz TTL	This is a status signal indicating if Loss Of Frame (LOF) has been detected and declared. The LOF status is also available in an internal status register bit.
LCD-P	Loss of Cell Delineation	O	<1MHz TTL	This signal is asserted when the cell delineation state machine in not in SYNC state. This alarm indication is also available via internal register access.
LOPC	Loss of Optical Carrier	I	<1MHz TTL	This signal is being monitored and changes in the signal status may cause generation of an interrupt. This will allow for monitoring of the LOPC signal via the UNI device CPU interface.
TDO	Test Data Output	O	<1MHz TTL	This signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. The TDO signal is a tristate output which is inactive except when data scan shifting is in progress.
TDI	Test Data Input	I	<1MHz TTL	The signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor.
TCK	Test Clock	I	<1MHz TTL	This signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Test Mode Select	I	<1MHz TTL	This signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-up resistor.
$\overline{\text{TRSTB}}$	Test Reset	I	<1MHz TTL	This signal (active low) provides an asynchronous test access port reset via the IEEE P1149.1 test access port. $\overline{\text{TRSTB}}$ is a schmitt triggered input with an internal pull-up resistor.
OE	Output Enable	I	<1MHz TTL	When deasserted (set low), all TTL device outputs are tri-stated. The OE signal has an internal pull-up.

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Package Pinout by Signal Name

Signal	BGA pin	Signal	BGA pin	Signal	BGA pin
D[7]	W4	RUDATA[23]	W15	TUDATA[25]	K19
D[6]	Y4	RUDATA[22]	V15	TUDATA[24]	J19
D[5]	V5	RUDATA[21]	Y16	TUDATA[23]	J18
D[4]	U6	RUDATA[20]	W16	TUDATA[22]	H20
D[3]	W5	RUDATA[19]	U15	TUDATA[21]	J17
D[2]	Y5	RUDATA[18]	V16	TUDATA[20]	H19
D[1]	V6	RUDATA[17]	Y17	TUDATA[19]	H18
D[0]	W6	RUDATA[16]	W17	TUDATA[18]	G20
A[7]	Y6	RUDATA[15]	U16	TUDATA[17]	G19
A[6]	V7	RUDATA[14]	V17	TUDATA[16]	H17
A[5]	U8	RUDATA[13]	U18	TUDATA[15]	G18
A[4]	W7	RUDATA[12]	T17	TUDATA[14]	F20
A[3]	Y7	RUDATA[11]	U19	TUDATA[13]	F19
A[2]	V8	RUDATA[10]	U20	TUDATA[12]	F18
A[1]	U9	RUDATA[9]	T18	TUDATA[11]	E20
A[0]	W8	RUDATA[8]	R17	TUDATA[10]	E19
ALE	V9	RUDATA[7]	T19	TUDATA[9]	F17
CSB	W9	RUDATA[6]	T20	TUDATA[8]	E18
WRB	Y9	RUDATA[5]	R18	TUDATA[7]	D20
RDB	U10	RUDATA[4]	R19	TUDATA[6]	D19
RSTB	V10	RUDATA[3]	R20	TUDATA[5]	E17
OE	W10	RUDATA[2]	P18	TUDATA[4]	D18
VDD5	Y10	RUDATA[1]	N17	TUDATA[3]	C17
INTB	V11	RUDATA[0]	P19	TUDATA[2]	D16
LOPC	W11	RUPRTY	P20	TUDATA[1]	B17
LOS	W12	RUSOC	N18	TUDATA[0]	A17
LOF	V12	RUEMPTY*/ RUCLAV	M17	TUPRTY	C16
LCD-P	Y13	RUCLKO	N19	TUSOC	D15
RUDATA[31]	U12	RUCLK	M18	TUCLK	B16
RUDATA[30]	W13	RUENB*	M19	TUENB*	A16
RUDATA[29]	V13	TUDATA[31]	M20	TUCLKO	C15
RUDATA[28]	Y14	TUDATA[30]	L17	TUFULL*/ TUCLAV	B15
RUDATA[27]	W14	TUDATA[29]	L18	RXRCLK	A15
RUDATA[26]	U13	TUDATA[28]	L19	TXRCLK	C14
RUDATA[25]	V14	TUDATA[27]	L20	TRSTB	D13
RUDATA[24]	Y15	TUDATA[26]	K18	TDO	B14

Signal	*BGA pin*	*Signal*	*BGA pin*	*Signal*	*BGA pin*
TDI	A14	RLIN[2]-	F4	TLOUT[14]+	U1
TCK	C13	RLIN[3]-	E2	TLOUT[14]-	U2
TMS	D12	RLIN[3]+	E1	TLOUT[15]-	T4
GPIOO[3]	B13	RLIN[0]-	F3	TLOUT[15]+	U3
GPIOO[2]	C12	RLIN[0]+	F2	TLPRTY+	V4
GPIOO[1]	B12	RLIN[1]+	F1	TLPRTY-	U5
GPIOO[0]	A12	RLIN[1]-	G3	GND	A1
GPIOI[1]	D11	TLCLK+	H4	GND	A2
GPIOI[0]	C11	TLCLK-	G2	GND	A3
VDD5	B11	TLCLKOUT-	G1	GND	A9
RLCLK+	A11	TLCLKOUT+	H3	GND	A10
RLCLK-	C10	TLOUT[0]-	J4	GND	A13
RLPRTY+	B10	TLOUT[0]+	H2	GND	A18
RLPRTY-	B9	TLOUT[2]-	J3	GND	A19
RLIN[15]-	C9	TLOUT[2]+	J2	GND	A20
RLIN[15]+	A8	TLOUT[1]+	J1	GND	B1
RLIN[14]-	D9	TLOUT[1]-	K4	GND	B20
RLIN[14]+	B8	TLOUT[4]-	K3	GND	C1
RLIN[13]-	C8	TLOUT[4]+	K2	GND	C20
RLIN[13]+	A7	TLOUT[3]+	K1	GND	H1
RLIN[12]+	B7	TLOUT[3]-	L3	GND	J20
RLIN[12]-	D8	TLOUT[5]+	L2	GND	K20
RLIN[11]-	C7	TLOUT[5]-	M2	GND	L1
RLIN[11]+	A6	TLOUT[6]-	M3	GND	M1
RLIN[10]+	B6	TLOUT[6]+	N1	GND	N20
RLIN[10]-	C6	TLOUT[7]-	M4	GND	V1
RLIN[9]+	A5	TLOUT[7]+	N2	GND	V20
RLIN[9]-	B5	TLOUT[8]-	N3	GND	W1
RLIN[8]-	D6	TLOUT[8]+	P1	GND	W20
RLIN[8]+	C5	TLOUT[9]+	P2	GND	Y1
RLIN[7]+	A4	TLOUT[9]-	N4	GND	Y2
RLIN[7]-	B4	TLOUT[10]-	P3	GND	Y3
RLIN[6]-	D5	TLOUT[10]+	R1	GND	Y8
RLIN[6]+	C4	TLOUT[11]+	R2	GND	Y11
RLIN[4]+	D3	TLOUT[11]-	R3	GND	Y12
RLIN[4]-	E4	TLOUT[12]+	T1	GND	Y18
RLIN[5]-	D2	TLOUT[12]-	T2	GND	Y19
RLIN[5]+	D1	TLOUT[13]-	R4	GND	Y20
RLIN[2]+	E3	TLOUT[13]+	T3	VDD	B2

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Signal	*BGA pin*	*Signal*	*BGA pin*	*Signal*	*BGA pin*
VDD	B3	VDD	D17	VDD	U17
VDD	B18	VDD	G4	VDD	V2
VDD	B19	VDD	G17	VDD	V3
VDD	C2	VDD	K17	VDD	V18
VDD	C3	VDD	L4	VDD	V19
VDD	C18	VDD	P4	VDD	W2
VDD	C19	VDD	P17	VDD	W3
VDD	D4	VDD	U4	VDD	W18
VDD	D7	VDD	U7	VDD	W19
VDD	D10	VDD	U11		
VDD	D14	VDD	U14		

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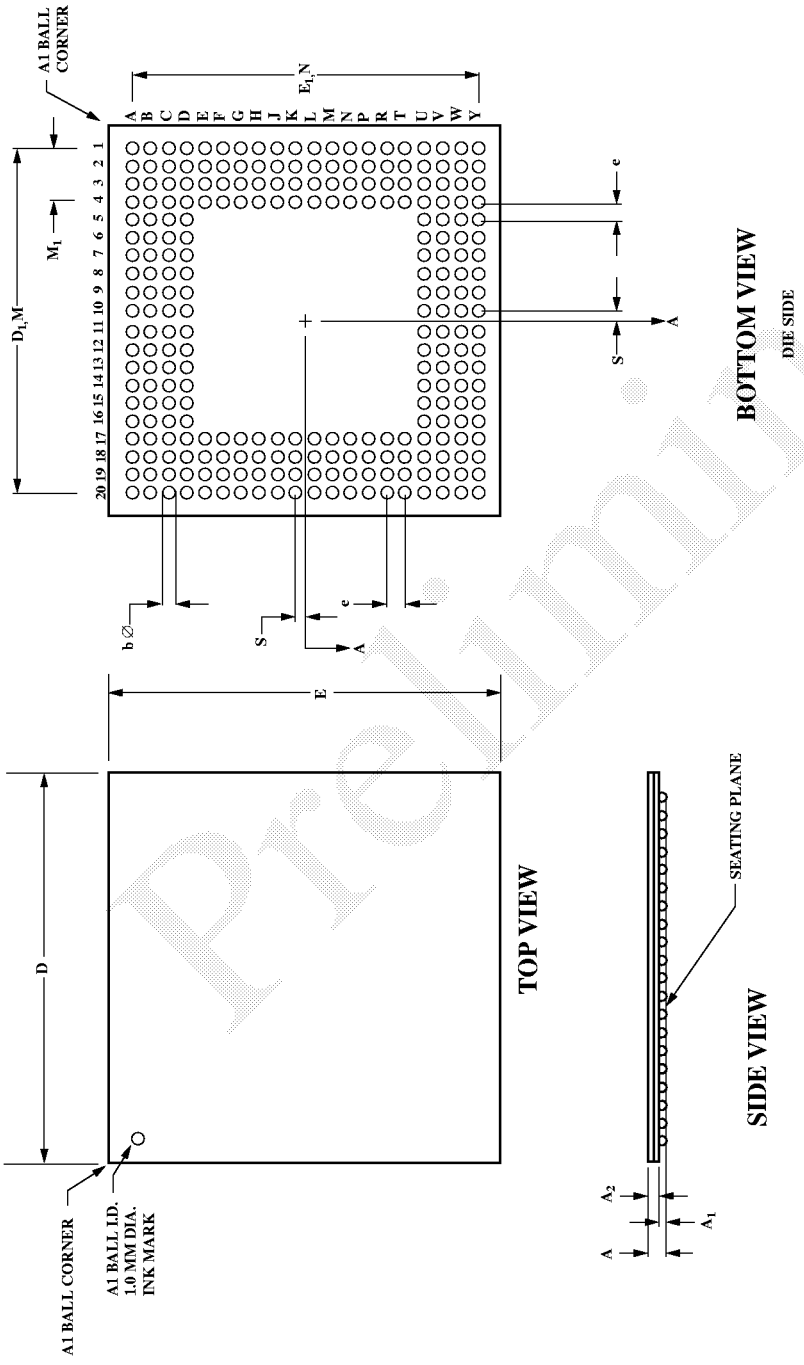
Package Information

BGA Package Dimensions



Item	*mm*	*Tolerance*
A	1.54	+/- .13
A1	0.63	+/- .07
A2	0.91	+/- .06
D	27.00	+/- .10
D1	24.13	+/- .10
E	27.00	+/- .10
E1	24.13	+/- .10
M,N	20 x 20	
M1	2-4	
b	0.75	+/- .15
e	1.27	
S	0.635	MAX

Package #: 101-324-6
Issue #: 1

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Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

Warning

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