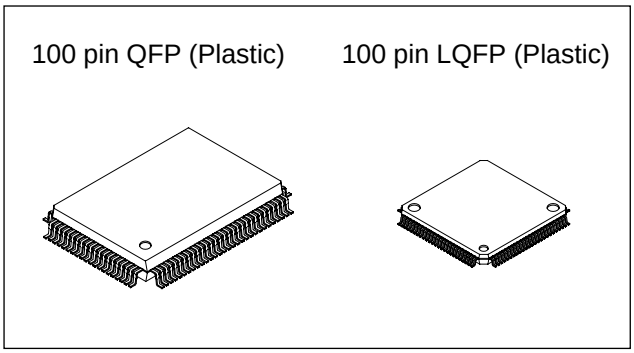
SONY

CXP974096

CMOS 16-bit Single Chip Microcomputer



Description

The CXP974096 is a CMOS 16-bit microcomputer integrating on a single chip an A/D converter, serial interface, I²C bus interface, timer, PWM output circuit, programmable pattern generator, remote control receive circuit, parallel interface, as well as basic configurations like a 16-bit CPU, ROM, RAM, and I/O port.

This LSI also provides the sleep/stop functions that enable lower power consumption.

Features

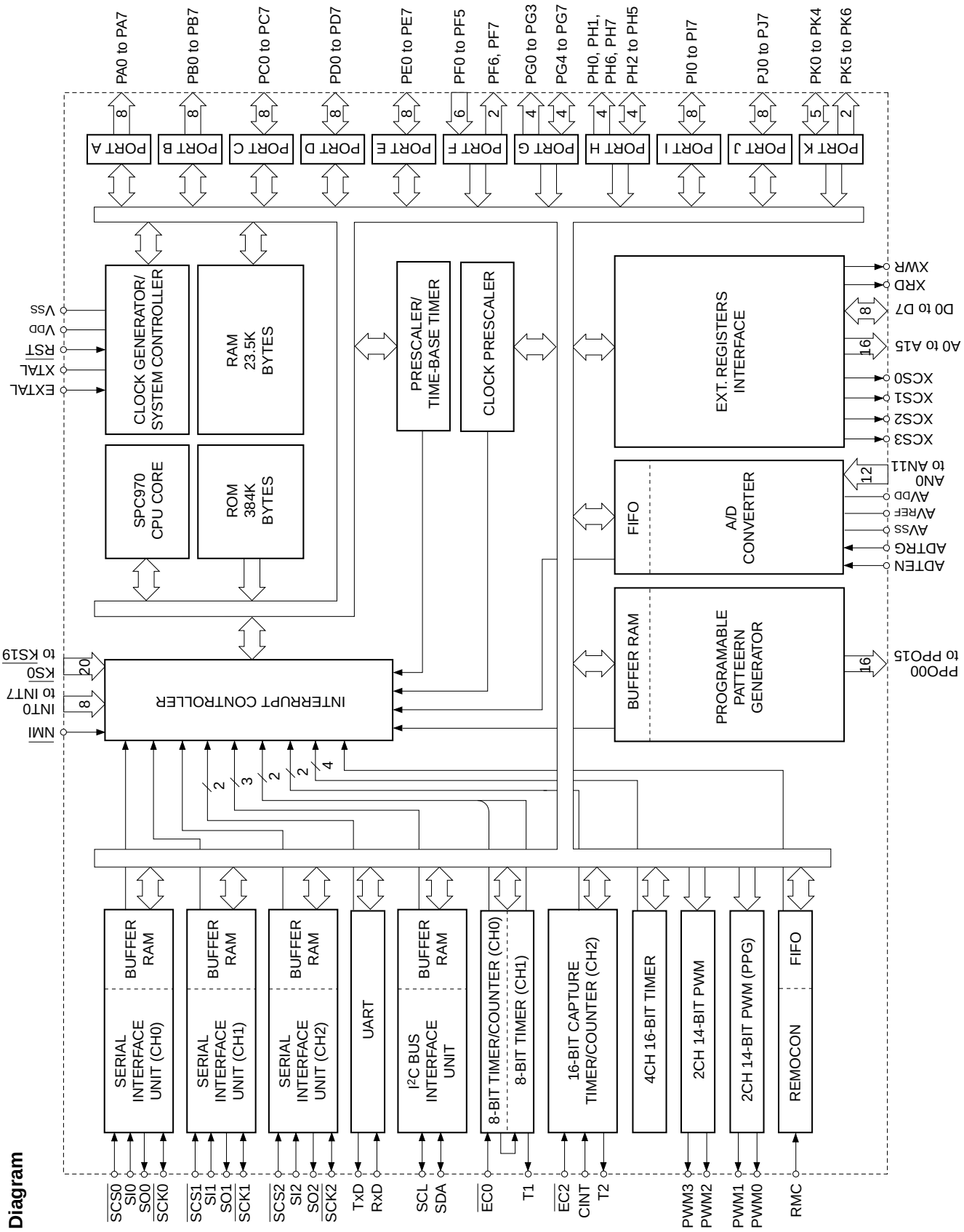
- An efficient instruction set as a controller
  - — Direct addressing, numerous abbreviated forms, multiplication and division instructions
- Instruction sets for C language and RTOS
  - — Highly quadratic instruction system, general-purpose register of 16-bit × 8-pin × 16-bank configuration
- Minimum instruction cycle
  50ns at 40MHz operation (2.7 to 3.6V)
- Incorporated ROM capacity 384K bytes
- Incorporated RAM capacity 23.5K bytes
- Peripheral functions
  - — A/D converter: 8-bit 12-analog input, successive approximation system, 3-stage FIFO (Conversion time: 1.55µs at 40MHz)
  - — Serial interface: Asynchronous serial interface (UART) 128-byte buffer RAM, 3 channels
  - — I²C bus interface: 64-byte buffer RAM (supports master/slave and automatic transfer mode)
  - — Timers: 8-bit timer/counter, 2 channels (with timing output) 16-bit capture timer/counter (with timing output) 16-bit timer, 4 channels, watchdog timer
  - — PWM output circuit: 14-bit PWM, 4 channels (2 channels of binary output switch function by PPG)
  - — Programmable pattern generator: 16-bit output, 64-byte buffer RAM, 1 channel
  - — Remote control receive circuit: 8-bit pulse measurement counter, 10-stage FIFO
  - — Parallel interface: External register interface (8-bit parallel bus), 4-chip select
- Interruption: 33 factors, 33 vectors, multi-interruption and priority selection possible
- Standby mode: Sleep/stop
- Package: 100-pin plastic QFP, 100-pin plastic LQFP
- Piggy/evaluation chip: CXP971000
- FLASH EEPROM incorporated version: CXP974F096

Structure

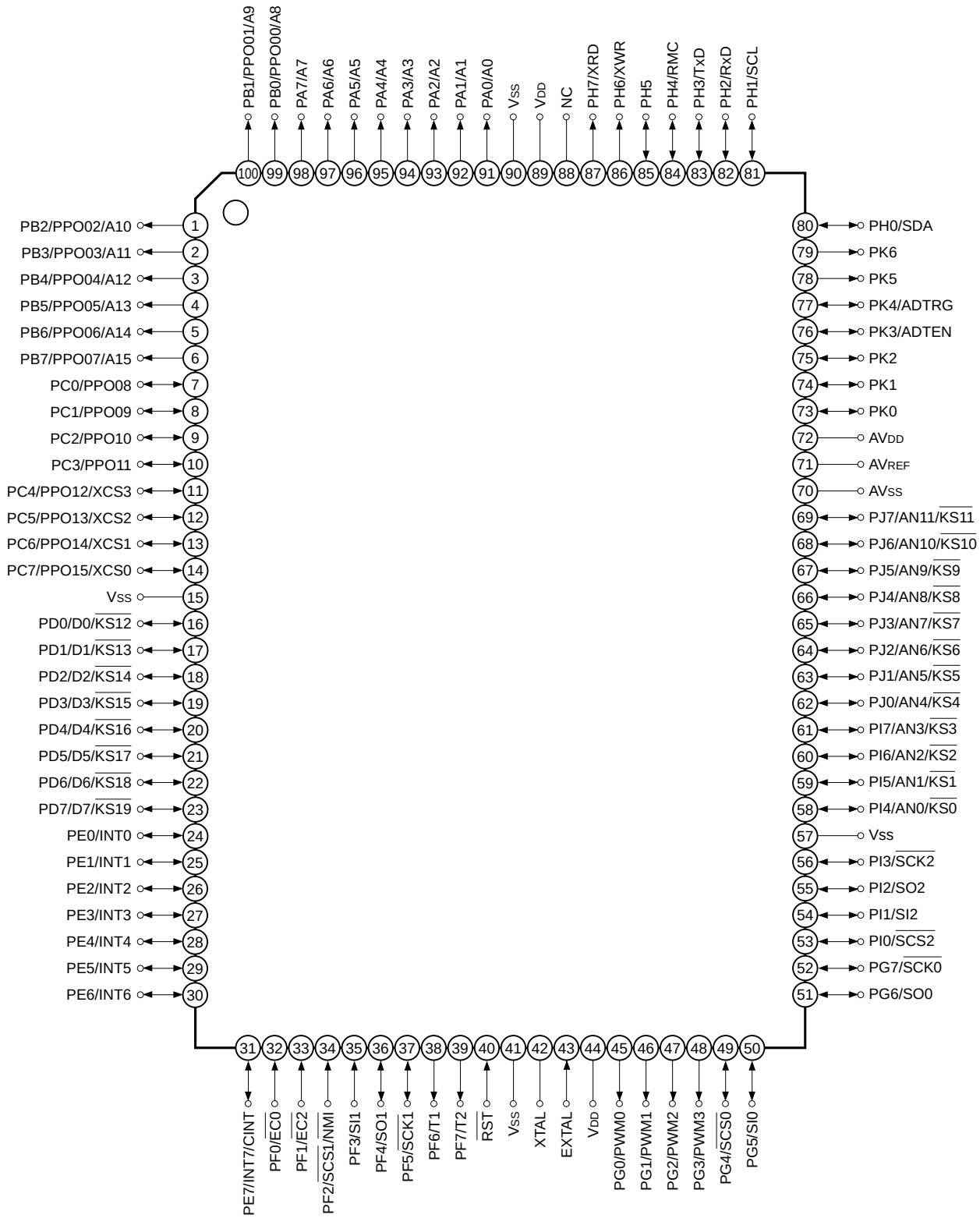
Silicon gate CMOS IC

E00Y30A18-PS

Block Diagram

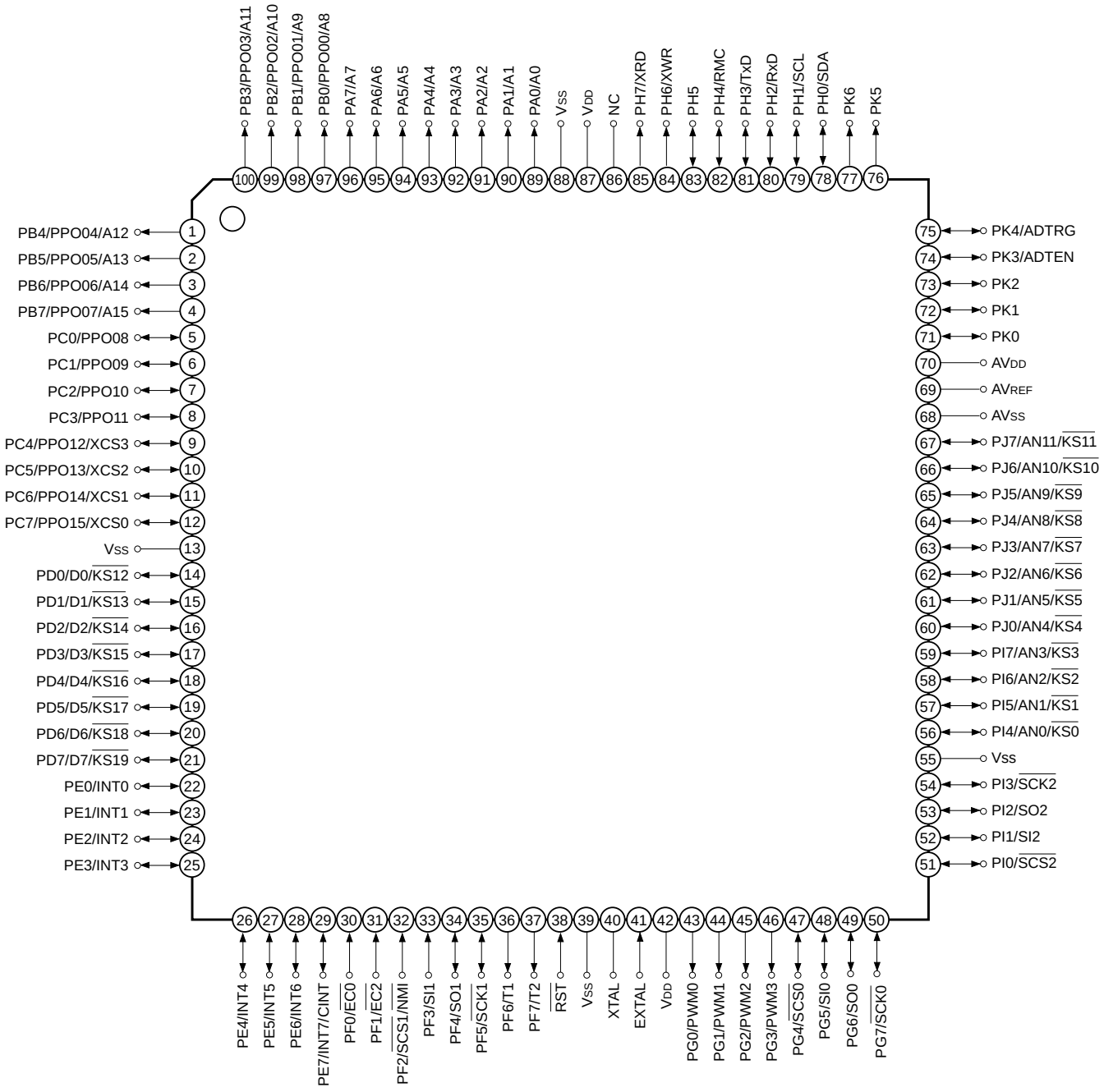


Pin Assignment 1 (Top View) 100-pin QFP package



Note) 1. NC (Pin 88) must be left open. However, use this pin for FLASH EEPROM incorporated version.
2. Vss and AVss (Pins 15, 41, 57, 70 and 90) must be connected to GND.
3. V_{DD} and AV_{DD} (Pins 44, 72 and 89) must be connected to V_{DD}.

Pin Assignment 2 (Top View) 100-pin LQFP package



Note) 1. NC (Pin 86) must be left open. However, use this pin for FLASH EEPROM incorporated version.

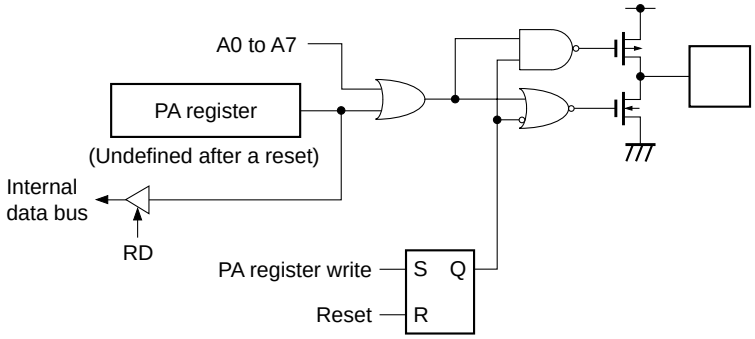
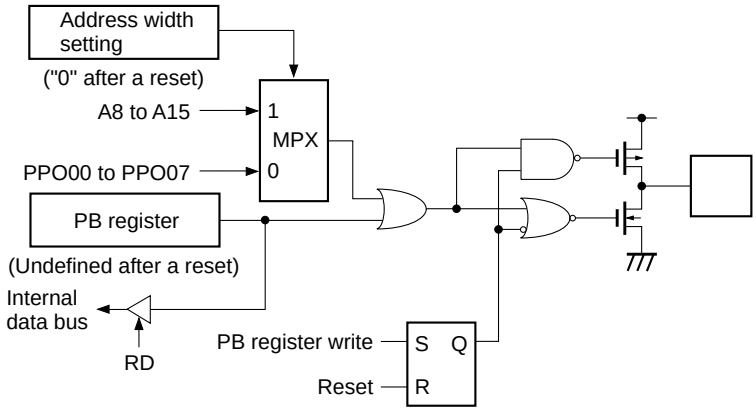
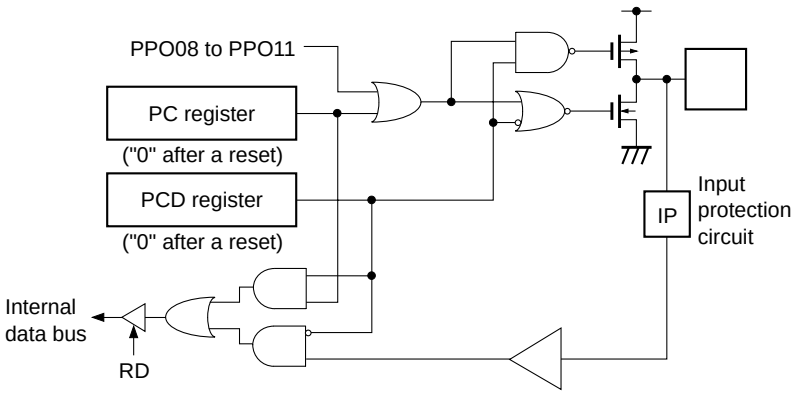
2. Vss and AVss (Pins 13, 39, 55, 68 and 88) must be connected to GND.
3. V_{DD} and AV_{DD} (Pins 42, 70 and 87) must be connected to V_{DD}.

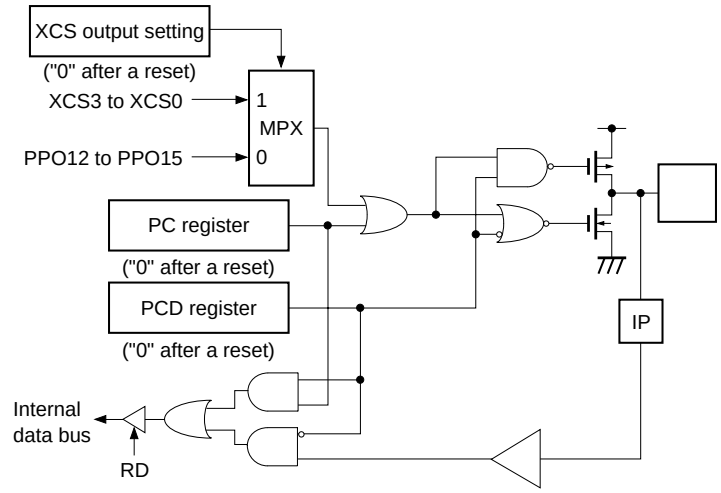
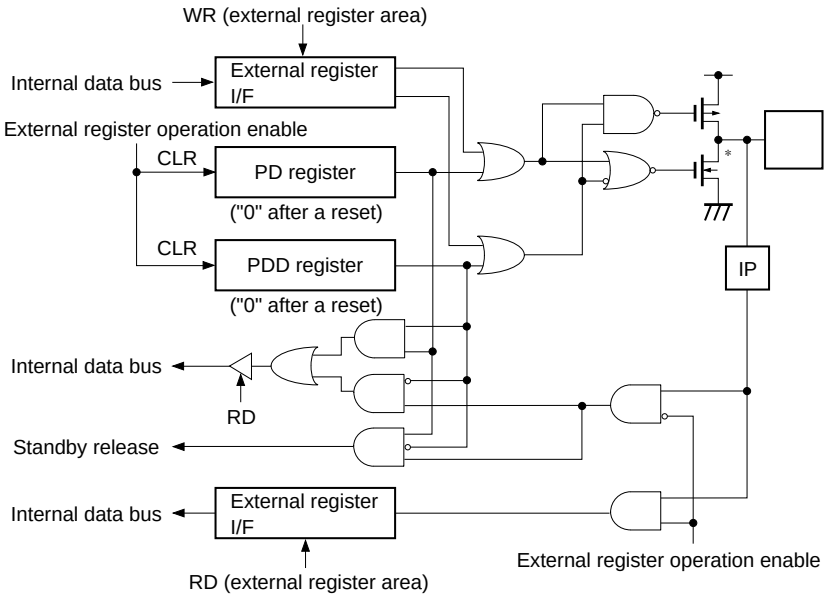
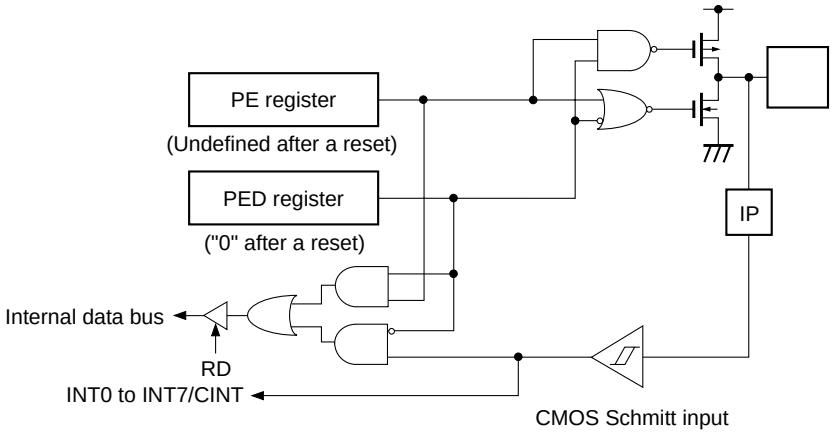
Pin Functions

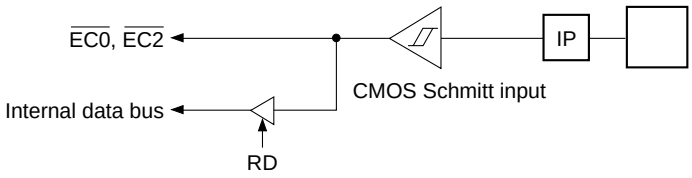
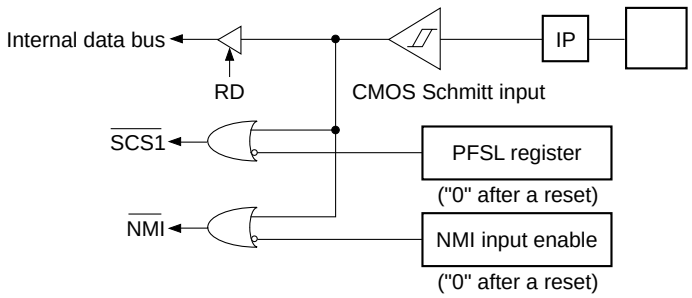
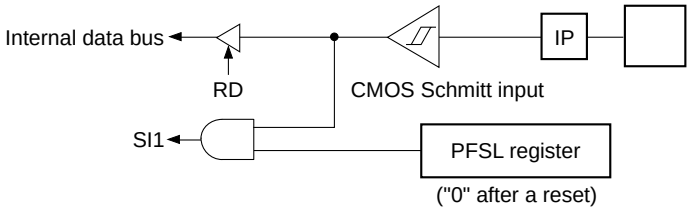
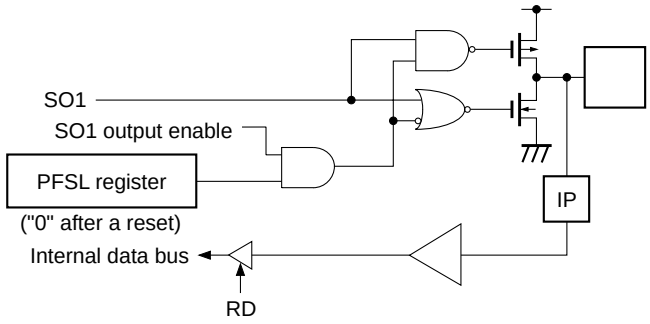
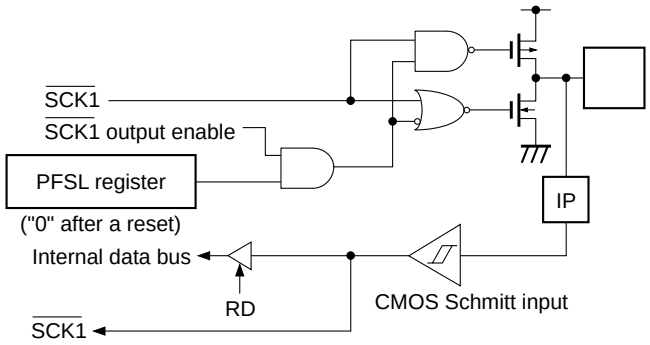
Symbol	I/O	Functions		
PA0/A0 to PA7/A7	Output / Output	(Port A) 8-bit output port. (8 pins)	External register interface address bus port output data value and OR output. (8 pins)	
PB0/PPO00/ A8 to PB7/PPO07/ A15	Output / Output / Output	(Port B) 8-bit output port. PPO value and OR output. (8 pins)		External register interface address bus. Address width can be extended in 1-bit units. (8 pins)
PC0/PPO08 to PC3/PPO11	I/O / Output	(Port C) 8-bit I/O port. I/O can be specified in 1-bit units. PPO value and OR output. (8 pins)	Programmable pattern generator outputs. (16 pins)	
PC4/PPO12/ XCS3 to PC7/PPO15/ XCS0	I/O / Output / Output			External register interface chip select signal. Chip select signal output function can be selected in 1-bit units. (4 pins)
PD0/D0/ $\overline{\text{KS12}}$ to PD7/D7/ $\overline{\text{KS19}}$	I/O / I/O / Input	(Port D) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	External register interface data bus. (8 pins)	Standby release input function can be specified in 1-bit units. (8 pins)
PE0/INT0 to PE6/INT6	I/O / Input	(Port E) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	External interrupt inputs. (8 pins)	
PE7/INT7/ CINT	I/O / Input / Input			External capture input for 16-bit capture timer/counter.
PF0/$\overline{\text{EC0}}$ PF1/$\overline{\text{EC2}}$	Input / Input	(Port F) 8-bit port. Lower 6 bits are for input; upper 2 bits are for output. (8 pins)	External event inputs for 8-bit timer/counter. (2 pins)	
PF2/$\overline{\text{SCS1}}$/ $\overline{\text{NMI}}$	Input / Input / Input		Serial chip select (CH1) input.	Non-maskable external interrupt input.
PF3/SI1	Input / Input		Serial data (CH1) input.	
PF4/SO1	Input / Output		Serial data (CH1) output.	
PF5/$\overline{\text{SCK1}}$	Input / I/O		Serial clock (CH1) I/O.	
PF6/T1	Output / Output		8-bit timer/counter output.	
PF7/T2	Output / Output		16-bit capture timer/counter timing output.	
PG0/PWM0 to PG1/PWM1	Output / Output	(Port G) 8-bit port. Lower 4 bits are for output; upper 4 bits are for I/O. Upper 4 bits can be specified in 1-bit units. (8 pins)	14-bit PWM output with output value switch control by programmable pattern generator. (2 pins)	
PG2/PWM2 PG3/PWM3	Output / Output		14-bit PWM output. (2 pins)	
PG4/$\overline{\text{SCS0}}$	I/O / Input		Serial chip select (CH0) input.	
PG5/SI0	I/O / Input		Serial data (CH0) input.	
PG6/SO0	I/O / Output		Serial data (CH0) output.	
PG7/$\overline{\text{SCK0}}$	I/O / I/O		Serial clock (CH0) I/O.	

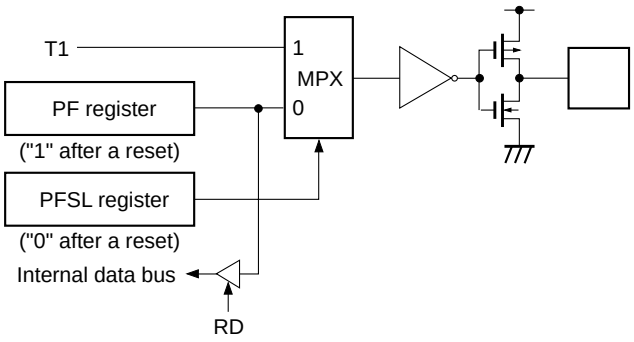
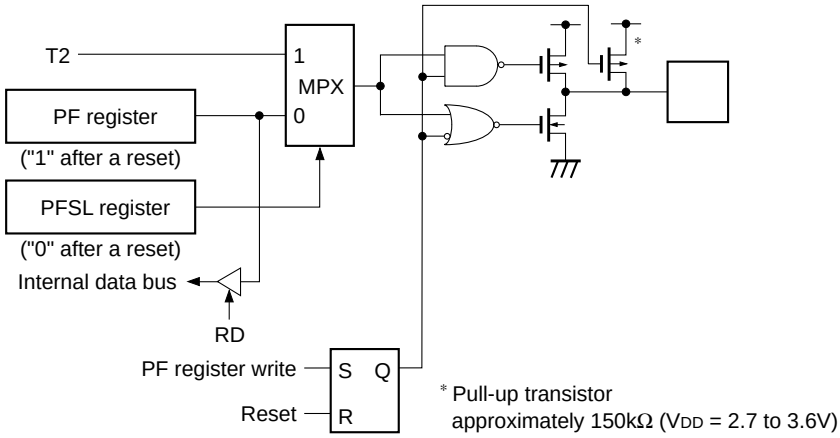
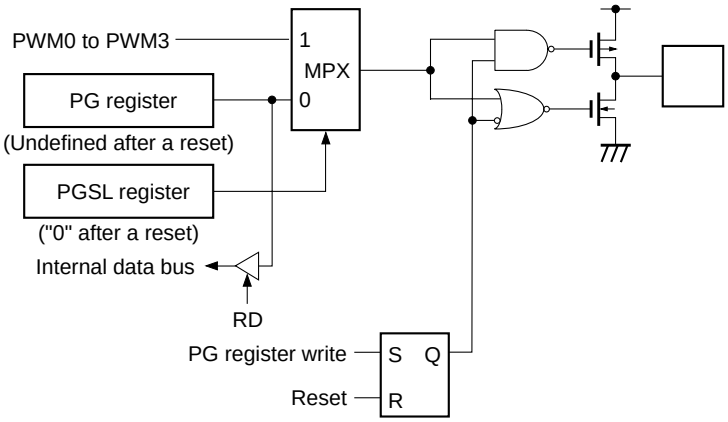
Symbol	I/O	Functions		
PH0/SDA	Output / I/O	(Port H) 8-bit port. Lower 2 bits are for large current N-ch open drain outputs; medium 4 bits are for I/O; upper 2 bits are for output. Medium 4 bits can be specified in 1-bit units. (8 pins)	I^2C bus interface data I/O.	
PH1/SCL	Output / I/O		I^2C bus interface clock I/O.	
PH2/RxD	I/O / Input		UART reception data input.	
PH3/TxD	I/O / Output		UART transmission data output.	
PH4/RMC	I/O / Input		Remote control receive circuit input.	
PH5	I/O			
PH6/XWR	Output / Output		External register interface write signal.	
PH7/XRD	Output / Output		External register interface read signal.	
PI0/$\overline{SCS2}$	I/O / Input	(Port I) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)	Serial chip select (CH2) input.	
PI1/SI2	I/O / Input		Serial data (CH2) input.	
PI2/SO2	I/O / Output		Serial data (CH2) output.	
PI3/$\overline{SCK2}$	I/O / I/O		Serial clock (CH2) I/O.	
$\overline{PI4}$/AN0/ $\overline{KS0}$ to $\overline{PI7}$/AN3/ $\overline{KS3}$	I/O / Input / Input		Analog input for A/D converter. (12 pins)	Standby release input function can be specified in 1-bit units. (12 pins)
$\overline{PJ0}$/AN4/ $\overline{KS4}$ to $\overline{PJ7}$/AN11/ $\overline{KS11}$	I/O / Input / Input	(Port J) 8-bit I/O port. I/O can be specified in 1-bit units. (8 pins)		
PK0 to PK2	I/O	(Port K) 7-bit port. Lower 5 bits are for I/O; upper 2 bits are for output. Lower 5 bits can be specified in 1-bit units. (7 pins)		
PK3/ADTEN	I/O / Input		A/D converter operation enable input by external trigger.	
PK4/ADTRG	I/O / Input		External trigger input for A/D converter.	
PK5 PK6	Output			
EXTAL	Input	Connects a crystal for main clock oscillation. (When the clock is supplied externally, input it to EXTAL and input an opposite phase clock to XTAL.)		
XTAL				
$\overline{RST}$	Input	System reset. Active at "L" level.		
AV_{DD}		Positive power supply for A/D converter. (Must be the same voltage with V_{DD})		
AV_{REF}	Input	Reference voltage input for A/D converter. (Must be the same voltage with V_{DD})		
AVss		GND for A/D converter.		
V_{DD}		Positive power supply. (Connect both V_{DD} pins to positive power supply.)		
Vss		GND. (Connect all four Vss pins to GND.)		
NC		NC. (NC is used for FLASH EEPROM incorporated version.)		

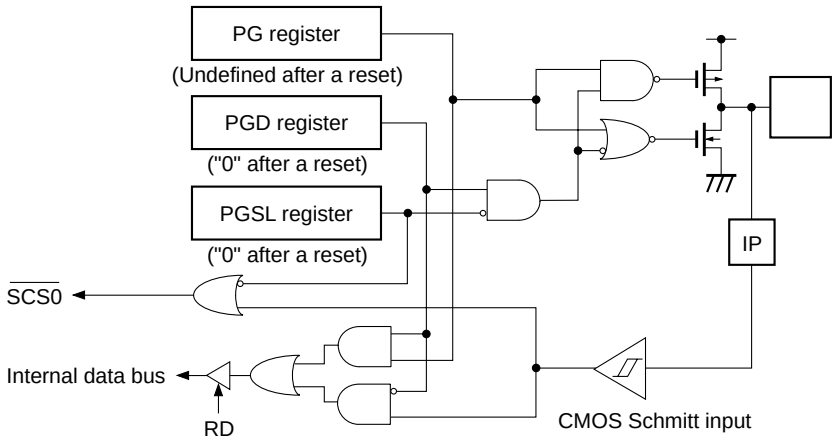
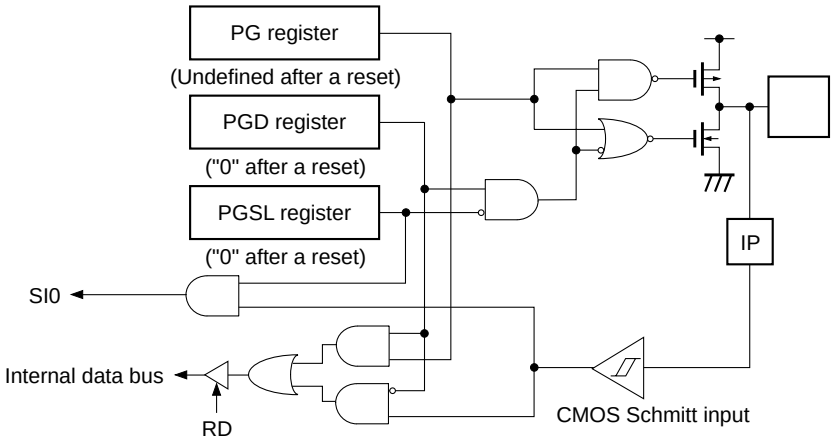
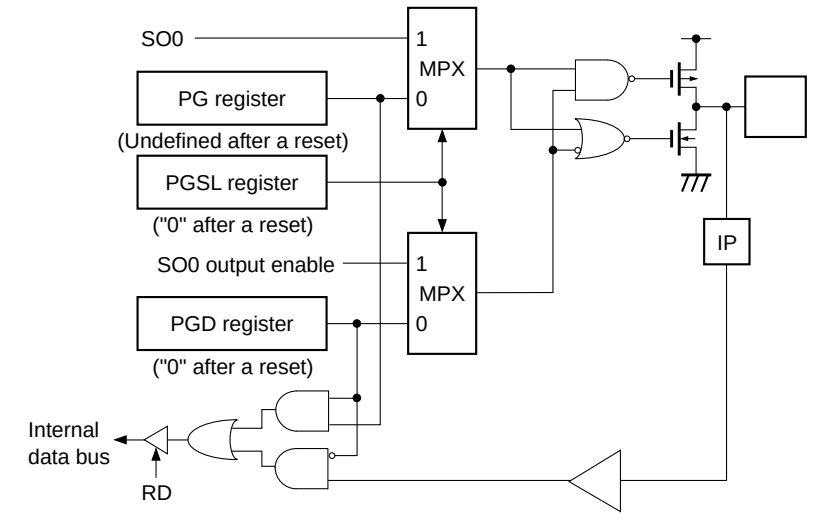
I/O Circuit Format for Pins

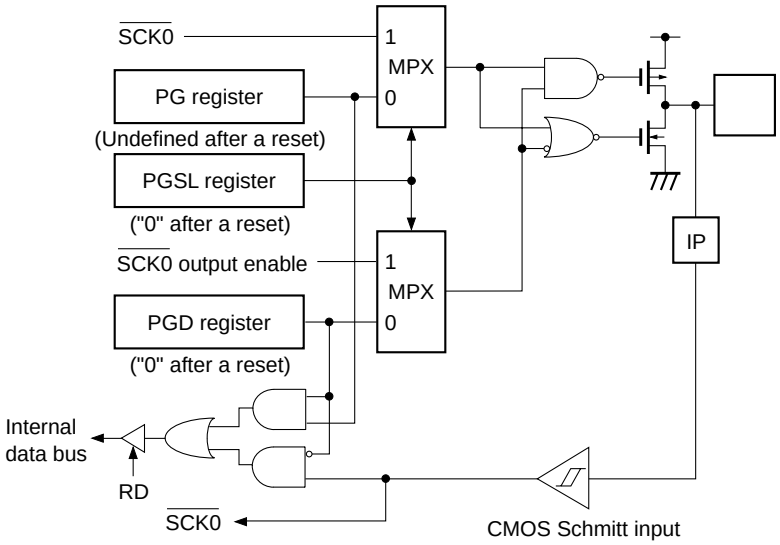
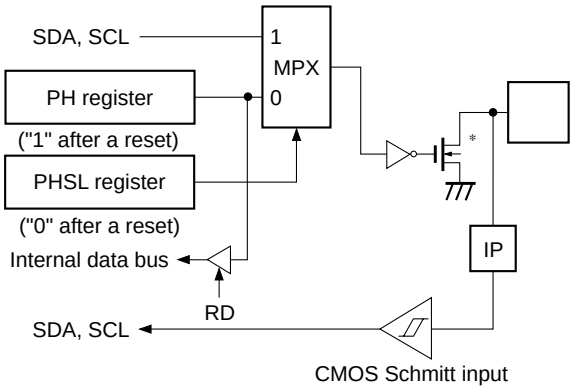
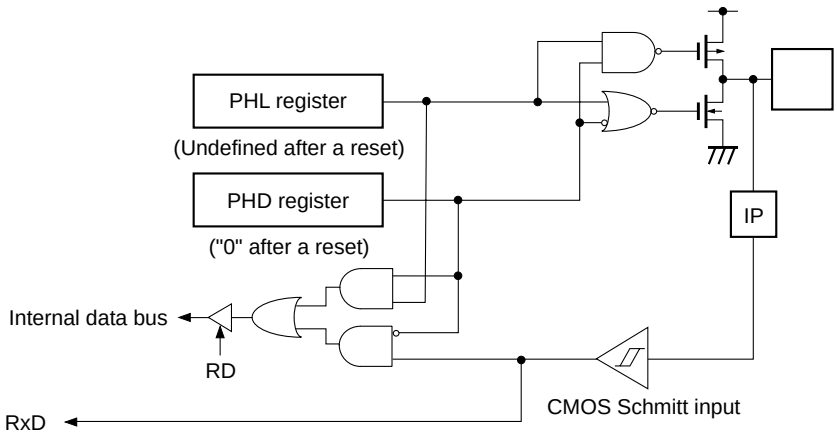
Pin	Circuit format	After a reset
PA0/A0 to PA7/A7		Hi-Z
PB0/PPO00/A8 to PB7/PPO07/A15		Hi-Z
PC0/PPO08 to PC3/PPO11		Hi-Z

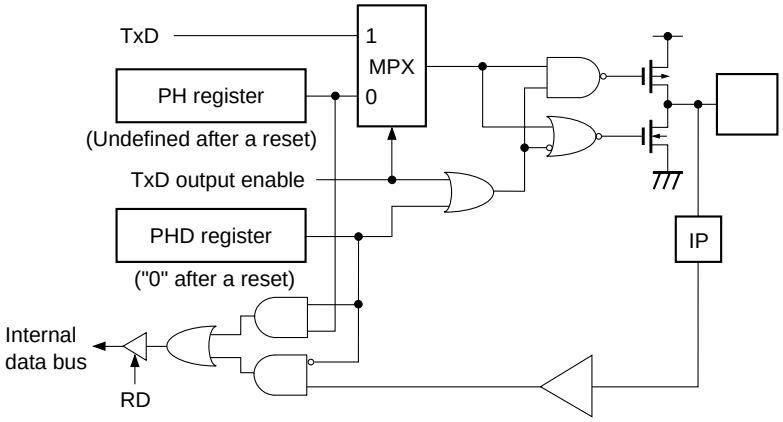
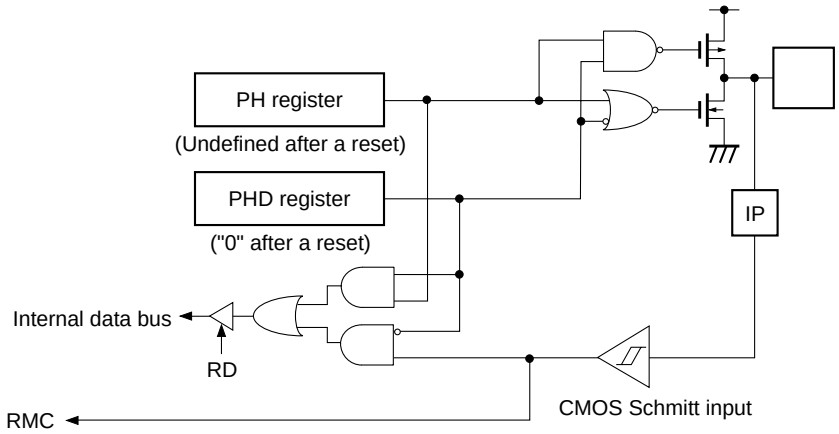
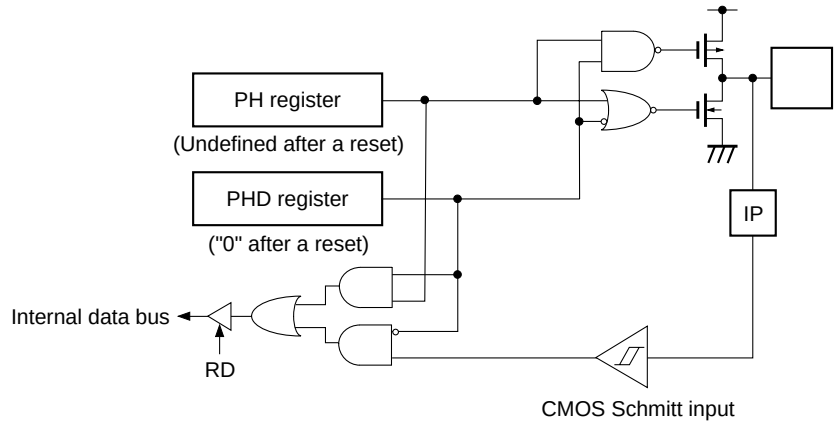
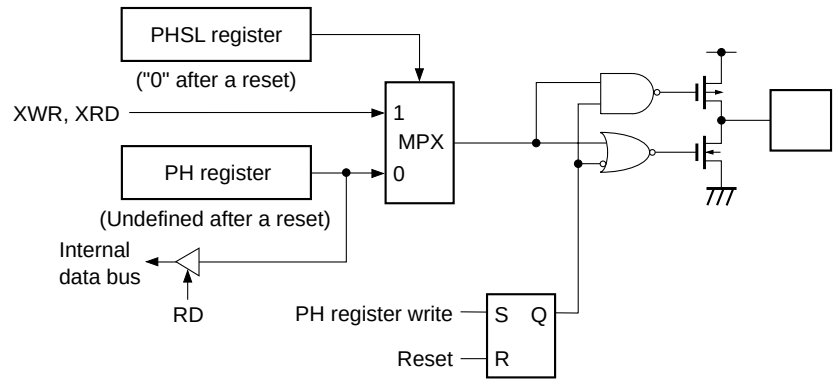
Pin	Circuit format	After a reset
PC4/PPO12/ XCS3 to PC7/PPO15/ XCS0		Hi-Z
PD0/D0/$\overline{KS12}$ to PD7/D7/ $\overline{KS19}$		Hi-Z
PE0/INT0 to PE7/INT7/ CINT		Hi-Z

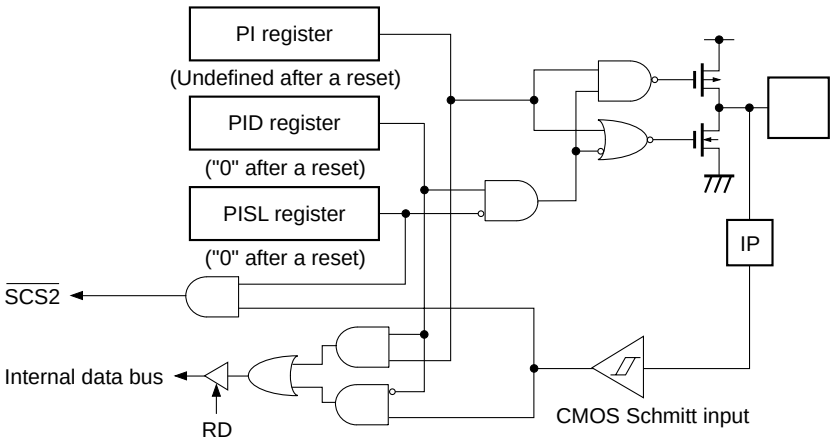
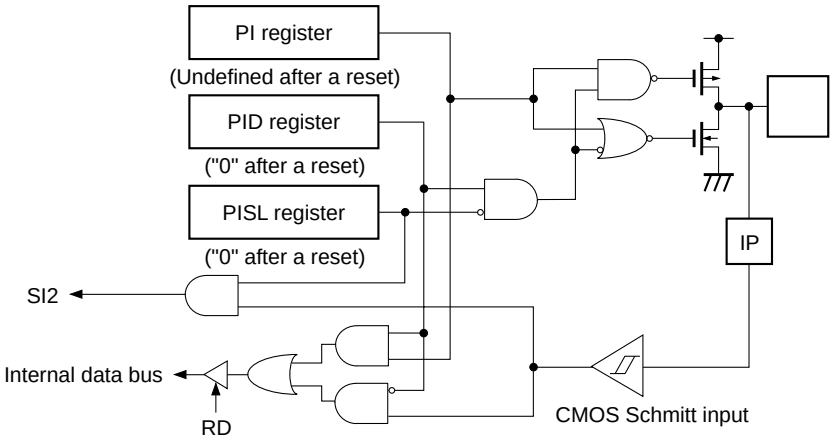
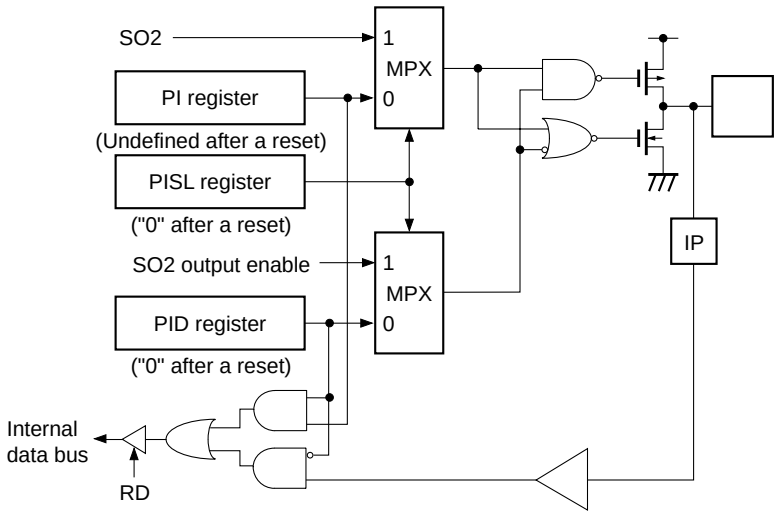
Pin	Circuit format	After a reset
PF0/$\overline{EC0}$ PF1/$\overline{EC2}$		Hi-Z
PF2/$\overline{SCS1}$/ $\overline{NMI}$		Hi-Z
PF3/SI1		Hi-Z
PF4/SO1		Hi-Z
PF5/$\overline{SCK1}$		Hi-Z

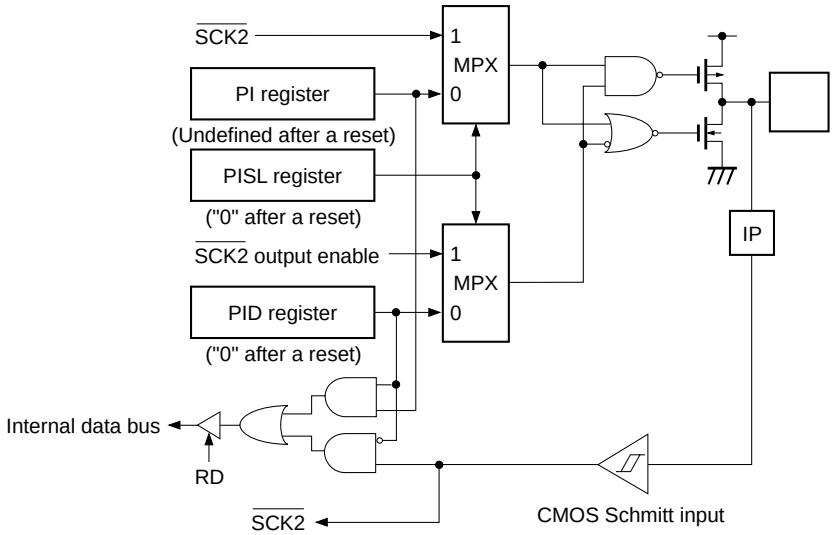
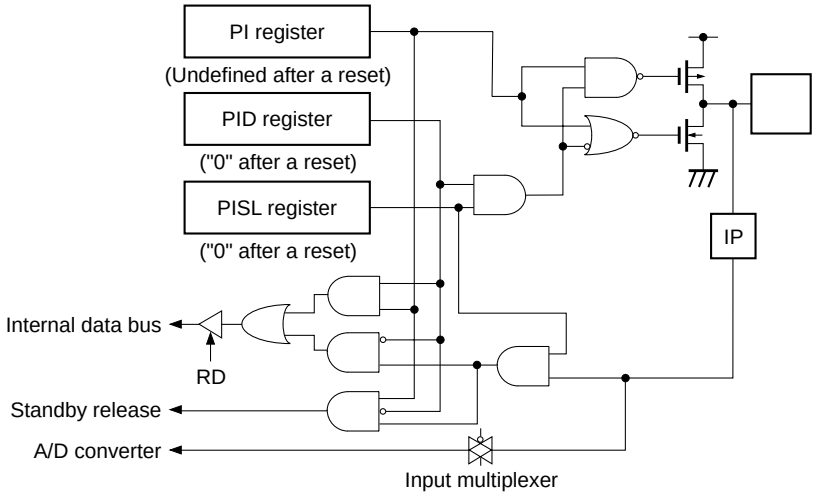
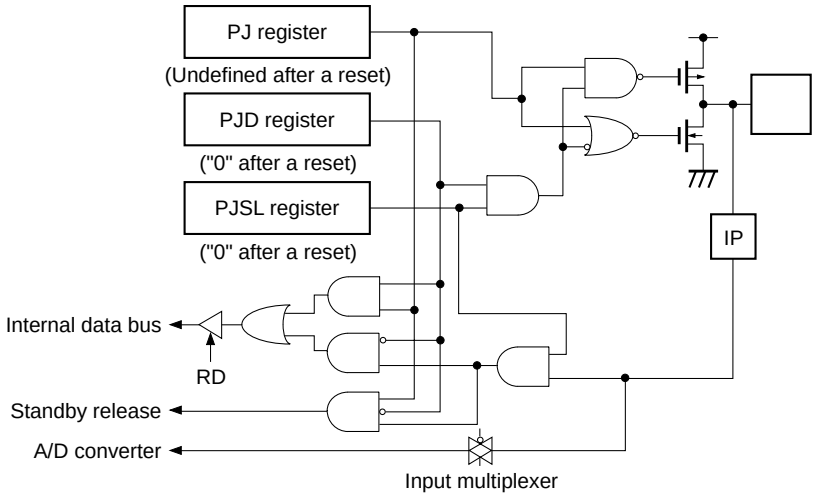
Pin	Circuit format	After a reset
PF6/T1		"H" level
PF7/T2		"H" level ("H" level at ON resistance of pull-up transistor by a reset.)
PG0/PWM0 to PG3/PWM3		Hi-Z

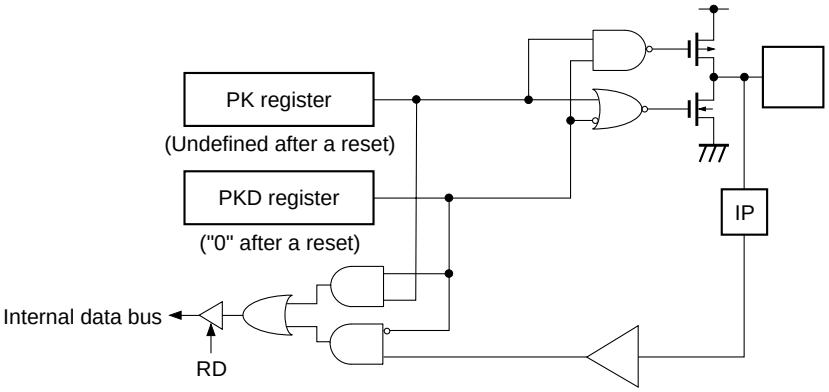
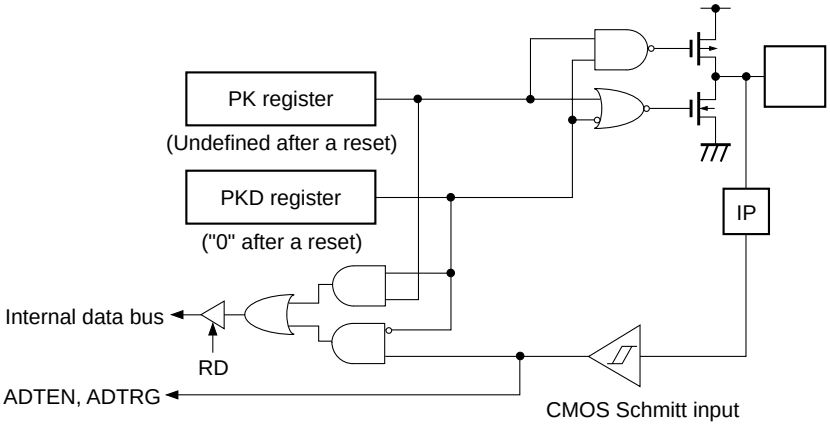
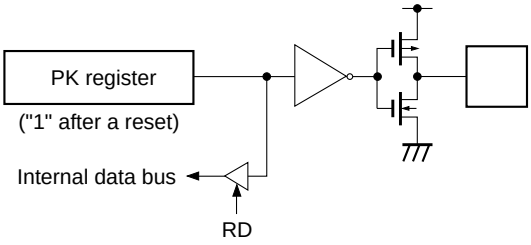
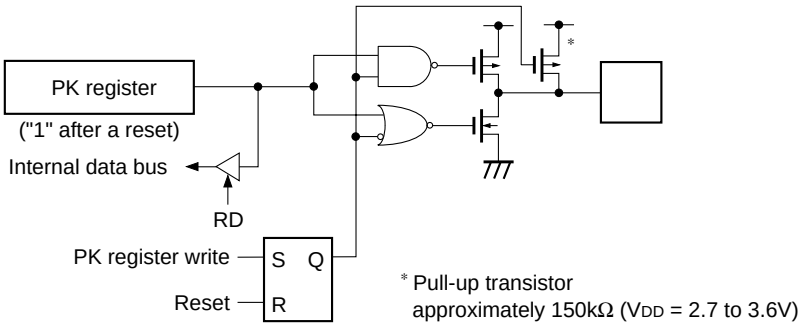
Pin	Circuit format	After a reset
PG4/$\overline{SCS0}$		Hi-Z
PG5/SI0		Hi-Z
PG6/SO0		Hi-Z

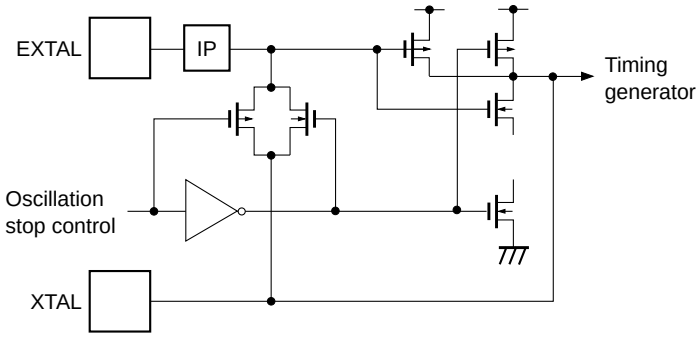
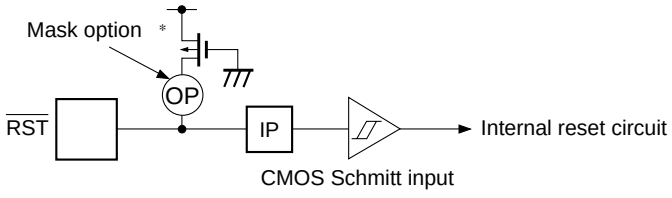
Pin	Circuit format	After a reset
PG7/$\overline{SCK0}$		Hi-Z
PH0/SDA PH1/SCL	 * Large current drive 5mA (V_{DD} = 2.7 to 3.6V)	Hi-Z
PH2/RxD		Hi-Z

Pin	Circuit format	After a reset
PH3/TxD		Hi-Z
PH4/RMC		Hi-Z
PH5		Hi-Z
PH6/XWR PH7/XRD		Hi-Z

Pin	Circuit format	After a reset
PI0/$\overline{SCS2}$		Hi-Z
PI1/SI2		Hi-Z
PI2/SO2		Hi-Z

Pin	Circuit format	After a reset
PI3/$\overline{SCK2}$		Hi-Z
PI4/AN0/$\overline{KS0}$ to PI7/AN3/ $\overline{KS3}$		Hi-Z
PJ0/AN4/$\overline{KS4}$ to PJ7/AN11/ $\overline{KS11}$		Hi-Z

Pin	Circuit format	After a reset
PK0 to PK2		Hi-Z
PK3/ADTEN PK4/ADTRG		Hi-Z
PK5		"H" level
PK6		"H" level ("H" level at ON resistance of pull-up transistor by a reset.)

Pin	Circuit format	After a reset
XTAL EXTAL	 • Diagram shows circuit configuration during oscillation. • Feedback resistor is removed during standby stop mode, and XTAL is driven at "H" level.	Oscillation
$\overline{\text{RST}}$	 * Pull-up transistor approximately 30kΩ (V_{DD} = 2.7 to 3.6V)	"L" level (during a reset)

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +4.6	V	
	AV_{DD}	AV_{SS} to +4.6*1	V	
	AV_{REF}	AV_{SS} to +4.6*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +4.6*2	V	
Output voltage	V_{OUT}	–0.3 to +4.6*2	V	
High level output current	I_{OH}	–5.0	mA	Output (value per pin)
High level total output current	ΣI_{OH}	–50	mA	Total for all output pins
Low level output current	I_{OL}	15.0	mA	All pins excluding large current output pins (value per pin)
	I_{OLC}	20.0	mA	Large current output pins*3 (value per pin)
Low level total output current	ΣI_{OL}	130	mA	Total for all output pins
Operating temperature	Topr	–30 to +85	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP-100P-L01
		380		LQFP-100P-L01

*1 AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.

*2 V_{IN} and V_{OUT} excluding PH0 and PH1 must not exceed V_{DD} + 0.3V.

*3 The large current drive transistor is N-ch transistor of PD and PH0, PH1.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	2.7	3.6	V	
		2.0	3.6		Guaranteed data hold range during stop mode
	AV_{DD}	2.7	3.6	V	*1
	AV_{REF}	2.7	3.6	V	*1
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*2
	V_{IHS}	0.8V_{DD}	V_{DD}	V	CMOS Schmitt input*3
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.2	V	EXTAL*4
Low level input voltage	V_{IL}	0	0.2V_{DD}	V	*2
	V_{ILS}	0	0.2V_{DD}	V	CMOS Schmitt input*3
	V_{ILEX}	–0.3	0.4	V	EXTAL*4
Operating temperature	Topr	–30	+85	°C	

*1 AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.

*2 PC, PD, PF4, PG6, PH3, PI2, PI4 to PI7, PJ, PK0 to PK2 for normal input port.

*3 $\overline{RST}$, PE, PF0 to PF3, PF5, PG4, PG5, PG7, PH0 to PH2, PH4, PH5, PI0, PI1,PI3, PK3 and PK4.

*4 Specified only during self-oscillation.

Electrical Characteristics

DC Characteristics 1

(Topr = –30 to +85°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PD to PE, PF6, PF7, PG0 to PG5, PH2, PH4, PH5, PI to PJ, PK0 to PK6	V_{DD} = 3.0V, I_{OH} = –0.15mA	2.70			V
			V_{DD} = 2.7V, I_{OH} = –0.15mA	2.40			
			V_{DD} = 3.0V, I_{OH} = –0.5mA	2.30			V
			V_{DD} = 2.7V, I_{OH} = –0.5mA	2.00			
		PA to PC, PF4, PF5, PG6, PG7, PH3, PH6, PH7, PI2, PI3	V_{DD} = 3.0V, I_{OH} = –1.5mA	2.30			V
			V_{DD} = 2.7V, I_{OH} = –1.5mA	2.00			
Low level output voltage	V_{OL}	PE, PF6, PF7, PG0 to PG5, PH2, PH4, PH5, PI0, PI1, PI4 to PI7, PJ, PK0 to PK6	I_{OL} = 1.2mA			0.30	V
			I_{OL} = 1.6mA			0.50	V
		PA to PC, PF4, PF5, PG6, PG7, PH3, PH6, PH7, PI2, PI3	I_{OL} = 2.0mA			0.30	V
			I_{OL} = 3.0mA			0.50	V
		PD, PH0, PH1	I_{OL} = 5.0mA			1.00	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.6V, V_{IH} = 3.6V	0.3		61	µA
	I_{ILE}		V_{DD} = 3.6V, V_{IL} = 0.3V	–0.3		–61	µA
	I_{ILR}	$\overline{RST}$*1	V_{DD} = 3.6V, V_{IL} = 0.3V	–0.9		–250	µA
I/O leakage current	I_{IZ}	PA to PJ, PK0 to PK6, $\overline{RST}$*1	V_{DD} = 3.6V, V_I = 0, 3.6V			±31	µA
Open drain output leakage current (N-ch Tr. off state)	I_{LOH}	PH0, PH1	V_{DD} = 3.6V, V_{IH} = 3.6V			31	µA

*1 $\overline{RST}$ specifies the input current when pull-up resistor has been selected; the leakage current when no resistor has been selected.

DC Characteristics 2 (Topr = –30 to +85°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Typ.	Max.	Unit
Supply current*1	I_{DD1} *2	V_{DD}, V_{SS}	V_{DD} = 3.3 ± 0.3V, f_{EX} = fsrc = 40MHz, External clock operation A/D off state, PLL off state			32	40	mA
	I_{DDS2} *2	V_{DD}, V_{SS}	V_{DD} = 3.3 ± 0.3V, f_{EX} = fsrc = 40MHz, External clock operation A/D off state, PLL off state, sleep mode			8.0	10	mA
	I_{DDS3}	V_{DD}, V_{SS}	V_{DD} = 3.6V, stop mode	85°C or less			25	µA
				75°C or less			13	
				50°C or less			5	

*1 When all output pins are open.

*2 When the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh) are set to "00" and the LSI is operated in high-speed mode (2 frequency dividing clock).

I/O Capacitance

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	PF0 to PF3, EXTAL, $\overline{RST}$	Clock 1MHz, 0V for all pins excluding measured pins		10	20	pF
Output capacitance	C_{OUT}	PA to PB, PF6, PF7, PG0 to PG3, PH6, PH7, PK5, PK6, XTAL	Clock 1MHz, 0V for all pins excluding measured pins		10	20	pF
I/O capacitance	$C_{I/O}$	PC to PE, PF4, PF5, PG4 to PG7, PH0 to PH5, PI to PJ, PK0 to PK4	Clock 1MHz, 0V for all pins excluding measured pins		10	20	pF

AC Characteristics

(1) Clock timing

(Topr = –30 to +85°C, V_{DD} = 2.7 to 3.6 V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Main clock base oscillation frequency	f_{EX}	EXTAL, XTAL	Fig.1, Fig.2 Mask option Selection less than 40MHz	4.76	33.86	40.5	MHz
			Fig.1, Fig.2 Mask option Selection less than 20MHz	4.76	20.0	20.5	MHz
Main clock base oscillation input pulse width	t_{XH}	EXTAL, XTAL	f_{EX} = 40.0MHz Fig.1, Fig.2 External clock drive	4.0			ns
	t_{XL}						
	t_{XH}		f_{EX} = 33.86MHz Fig.1, Fig.2 External clock drive	4.0			ns
	t_{XL}						
	t_{XH}		f_{EX} = 20.0MHz Fig.1, Fig.2 External clock drive	11			ns
	t_{XL}						
Main clock base oscillation input rise time, fall time	t_{XR}	EXTAL, XTAL	f_{EX} = 40.0MHz Fig.1, Fig.2 External clock drive			8.5	ns
	t_{XF}						
	t_{XR}		f_{EX} = 33.86MHz Fig.1, Fig.2 External clock drive			10.5	ns
	t_{XF}						
	t_{XR}		f_{EX} = 20.0MHz Fig.1, Fig.2 External clock drive			14	ns
	t_{XF}						
Main clock duty	duty	XTAL	Fig.1, Fig.2 1/2 V_{DD} point	40	50	60	%

Note) tsys indicates the four values below according to the upper two bits (PCK1, PCK0) of the clock control register (CLC: 0002FEh).
tsys [ns] = 2/f_{EX} (PCK1, PCK0 = 00), 4/f_{EX} (PCK1, PCK0 = 01), 8/f_{EX} (PCK1, PCK0 = 10), 16/f_{EX} (PCK1, PCK0 = 11)

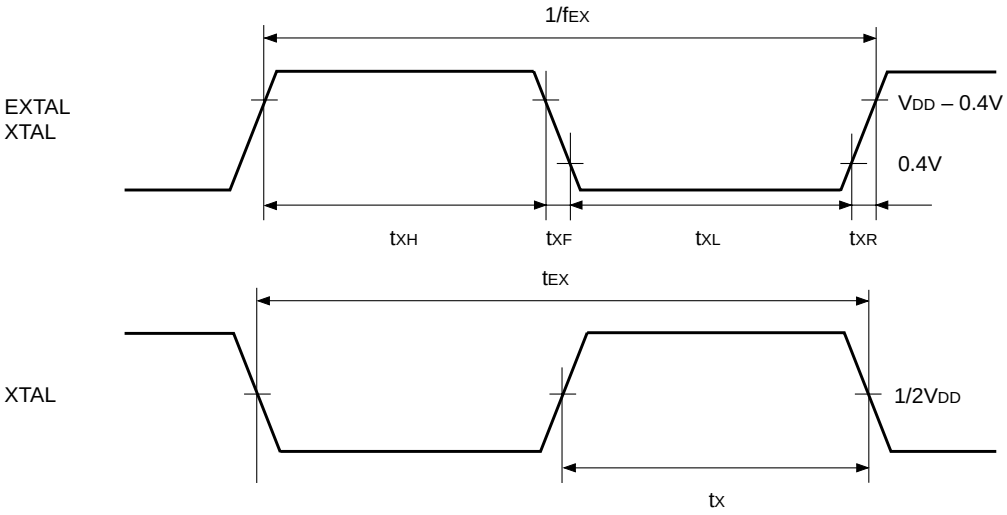
(2) Main clock multiplier circuit

(Topr = –30 to +85°C, V_{DD} = 2.7 to 3.6 V, Vss = 0V reference)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Main clock multiplier frequency	f_{SRC}	*1		22.0		40.5	MHz
			–20 to +85°C	19.9		40.5	
Lock-up time	t_{LOCK}				1	5	ms

*1 When the degree of input frequency of the main clock base oscillation frequency f_{EX} is 10.0 ± 0.1MHz, quadruple setting is 40.0 ± 0.4MHz.

Note) Main clock multiplier frequency f_{SRC} generates the value set from 1.5 times to 4 times of the main clock base oscillation frequency f_{EX} internally according to the Bits 10 to 8 (CMN2 to CMN0) of PLL setting register (PLL: 0002FCh).



duty = tx/tEX; tEX = 1/fEX

Fig. 1. Clock timing

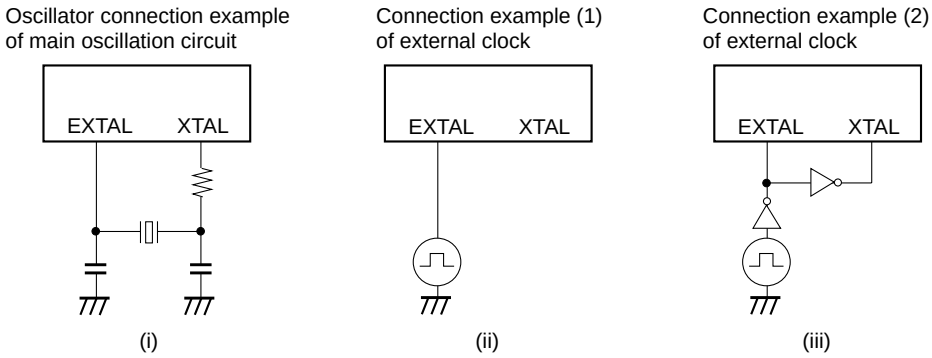


Fig. 2. Oscillator connection and clock applied conditions

(3) Event count input (Topr = –30 to +85°C, V_{DD} = 2.7 to 3.6V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC0}$, $\overline{EC2}$	Fig. 3	tsys + 100		ns

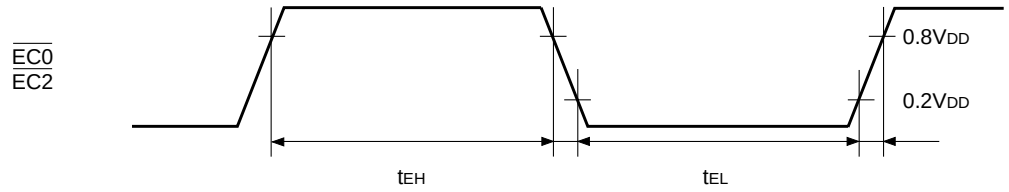


Fig. 3. Event count input timing

(4) Interruption and reset input (Topr = –30 to +85°C, V_{DD} = 2.7 to 3.6V, Vss = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Max.	Unit
External interruption high, low level width	t_{IH}, t_{IL}	$\overline{NMI}$, INT0 to INT7, $\overline{KS0}$ to $\overline{KS19}$	Main mode Sleep mode Fig. 4		tsys + 100		ns
		INT4 to INT7	Noise filter selected Fig. 4	ϕ	2tsys + 100		
				PS4	$32/f_{EX}$ + 100		
				PS6	$128/f_{EX}$ + 100		
Reset input low level width	t_{RST}	$\overline{RST}$	Fig. 5		$50/f_{EX}$		ns

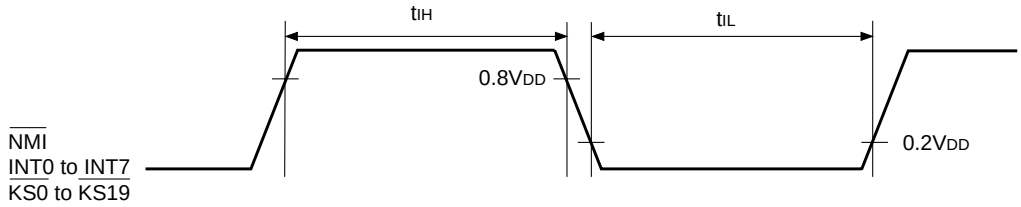


Fig. 4. Interruption input timing

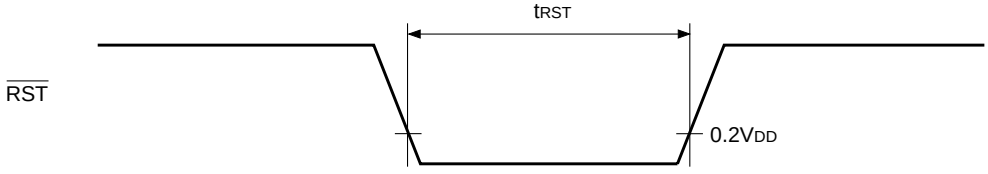


Fig. 5. Reset input timing

(5) A/D converter characteristics

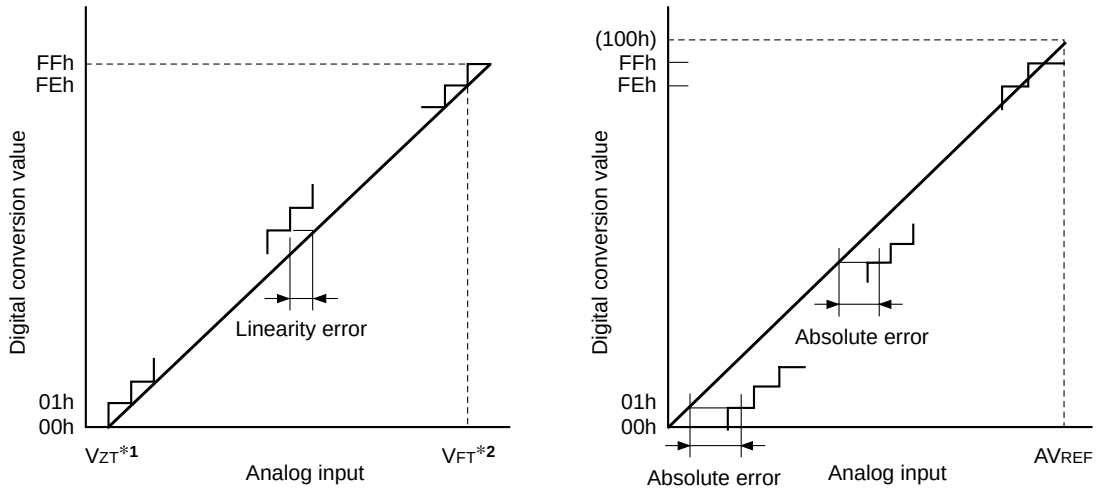
(Topr = –30 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 3.6V, Vss = AVss = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Typ.	Max.	Unit
Resolution							8	Bits
Linearity error			V_{DD} = AV_{DD} = AV_{REF} = 3.0V				±1	LSB
Absolute error							±3	LSB
Conversion time	t_{CONV}				34tsys			ns
			*1		62tsys			ns
Sampling time	t_{SAMP}				10tsys			ns
			*1		20tsys			ns
Reference input voltage	V_{REF}	AV_{REF}	V_{DD} = AV_{DD} = AV_{REF}		2.7		3.6	V
Analog input voltage		AN0 to AN11			0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Main mode	V_{DD} = 3.3 ± 0.3V f_{SRC} = 40MHz		1.5	2.1	mA
				V_{DD} = 3.3 ± 0.3V f_{SRC} = 20MHz		1.2	1.7	mA
	I_{REFS}		ADC off state*2 Stop mode				12	µA

*1 When Bit 6 (ADCK) of A/D control status register (ADCS: 000132h) is specified to "1".

*2 When Bit 5 (ADPC) of A/D control status register (ADCS: 000132h) is specified to "1".

Note) AV_{DD} and AV_{REF} must be the same voltage with V_{DD}.



*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

Fig. 6. Definition of A/D converter terms

(6) Serial transfer (CH0, CH1, CH2) (Topr = –30 to +85°C, V_{DD} = 2.7 to 3.6V, Vss = 0V reference)

Item	Symbol	Pins	Conditions		Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$	External start transfer mode ($\overline{SCK}$ = output mode)	V_{DD} = 3.3 ± 0.3V		1.5tsys + 200	ns
				V_{DD} = 3.0 ± 0.3V		1.5tsys + 210	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t_{DSKF}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$		V_{DD} = 3.3 ± 0.3V		1.5tsys + 200	ns
				V_{DD} = 3.0 ± 0.3V		1.5tsys + 210	ns
$\overline{CS} \downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0, SO1, SO2	External start transfer mode	V_{DD} = 3.3 ± 0.3V		1.5tsys + 200	ns
				V_{DD} = 3.0 ± 0.3V		1.5tsys + 210	ns
$\overline{CS} \uparrow \rightarrow$ SO float delay time	t_{DCSOF}	$\overline{SCS0}$, $\overline{SCS1}$, $\overline{SCS2}$		V_{DD} = 3.3 ± 0.3V		1.5tsys + 200	ns
				V_{DD} = 3.0 ± 0.3V		1.5tsys + 210	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{SCS0}$, $\overline{SCS1}$, $\overline{SCS2}$		V_{DD} = 3.3 ± 0.3V	tsys + 100		ns
				V_{DD} = 3.0 ± 0.3V	tsys + 110		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$	Input mode	V_{DD} = 3.3 ± 0.3V	2tsys + 200		ns
				V_{DD} = 3.0 ± 0.3V	2tsys + 210		ns
			Output mode	V_{DD} = 3.3 ± 0.3V	16/f_{EX}		ns
				V_{DD} = 3.0 ± 0.3V	16/f_{EX}		ns
$\overline{SCK}$ high, low pulse width	t_{KH}, t_{KL}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$	Input mode	V_{DD} = 3.3 ± 0.3V	tsys + 100		ns
				V_{DD} = 3.0 ± 0.3V	tsys + 110		ns
			Output mode	V_{DD} = 3.3 ± 0.3V	8/f_{EX} – 100		ns
				V_{DD} = 3.0 ± 0.3V	8/f_{EX} – 110		ns
SI input data setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0, SI1, SI2	$\overline{SCK}$ input mode	V_{DD} = 3.3 ± 0.3V	100		ns
				V_{DD} = 3.0 ± 0.3V	110		ns
			$\overline{SCK}$ output mode	V_{DD} = 3.3 ± 0.3V	200		ns
				V_{DD} = 3.0 ± 0.3V	210		ns
SI input data hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0, SI1, SI2	$\overline{SCK}$ input mode	V_{DD} = 3.3 ± 0.3V	2tsys + 100		ns
				V_{DD} = 3.0 ± 0.3V	2tsys + 110		ns
			$\overline{SCK}$ output mode	V_{DD} = 3.3 ± 0.3V	100		ns
				V_{DD} = 3.0 ± 0.3V	110		ns
$\overline{SCK} \downarrow \rightarrow$ SO delay time	t_{KSO}	SO0, SO1, SO2	$\overline{SCK}$ input mode	V_{DD} = 3.3 ± 0.3V		2tsys + 150	ns
				V_{DD} = 3.0 ± 0.3V		2tsys + 160	ns
			$\overline{SCK}$ output mode	V_{DD} = 3.3 ± 0.3V		100	ns
				V_{DD} = 3.0 ± 0.3V		110	ns
Minimum interval time	t_{INT}	$\overline{SCK0}$, $\overline{SCK1}$, $\overline{SCK2}$	$\overline{SCK}$ input mode	V_{DD} = 3.3 ± 0.3V	3tsys + 100		ns
				V_{DD} = 3.0 ± 0.3V	3tsys + 110		ns
			$\overline{SCK}$ output mode	V_{DD} = 3.3 ± 0.3V	8/f_{EX} – 100		ns
				V_{DD} = 3.0 ± 0.3V	8/f_{EX} – 110		ns

Note) The load condition for the $\overline{SCK}$ output mode and SO output delay time is 100pF.

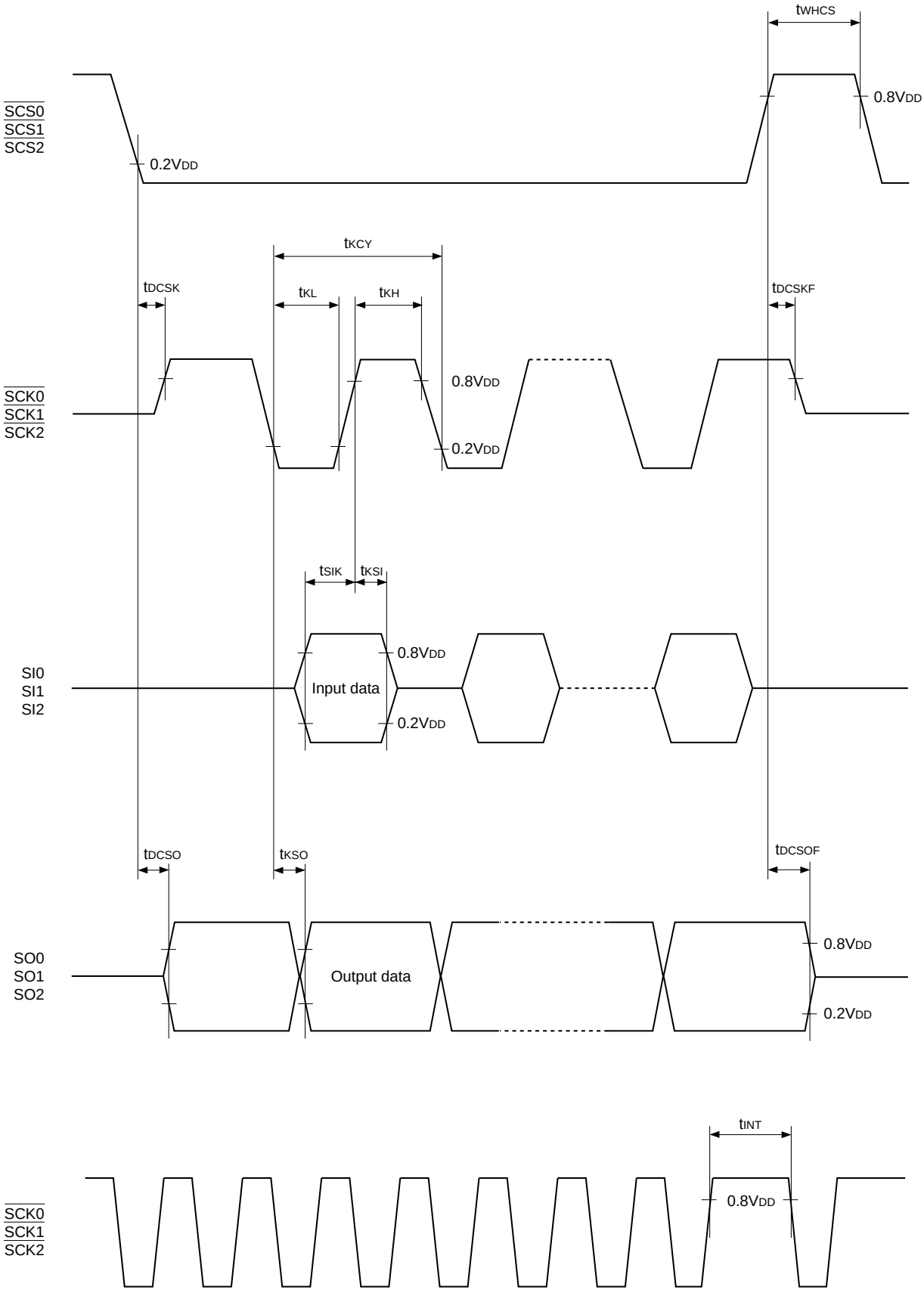


Fig. 7. Serial transfer CH0, CH1, CH2 timing

(7) I²C bus (Topr = –30 to +85°C, V_{DD} = 2.7 to 3.6V, Vss = 0V reference)

Item	Symbol	Pins	Standard mode		High-speed mode		Unit
			Min.	Max.	Min.	Max.	
SCK clock frequency	t_{SCL}	SCL		100		400	kHz
Bus free time between stop and start conditions	t_{BUF}	SDA	4.7		1.3		µs
Hold time under (resend) start condition	$t_{HD;STA}$	SDA, SCL	4.0		0.6		µs
Hold time in SCL clock low state	t_{Low}	SCL	4.7		1.3		µs
Hold time in SCL clock high state	t_{High}	SCL	4.0		0.6		µs
Setup time under (resend) start condition	$t_{SU;STA}$	SDA, SCL	4.7		0.6		µs
Data hold time	$t_{HD;DAT}$	SDA, SCL	0		0	0.9	µs
Data setup time	$t_{SU;DAT}$	SDA, SCL	250		100		ns
SCL, SDA signal output rise time	t_{Rd}, t_{Rc}	SDA, SCL		1000	20 + α*1	300	ns
SCL, SDA signal output fall time	t_{Fd}, t_{Fc}	SDA, SCL		300	20 + α*1	300	ns
Setup time under stop condition	$t_{SU;STO}$	SDA, SCL	4.0		0.6		µs

*1 Due to the total capacitance of the bus.

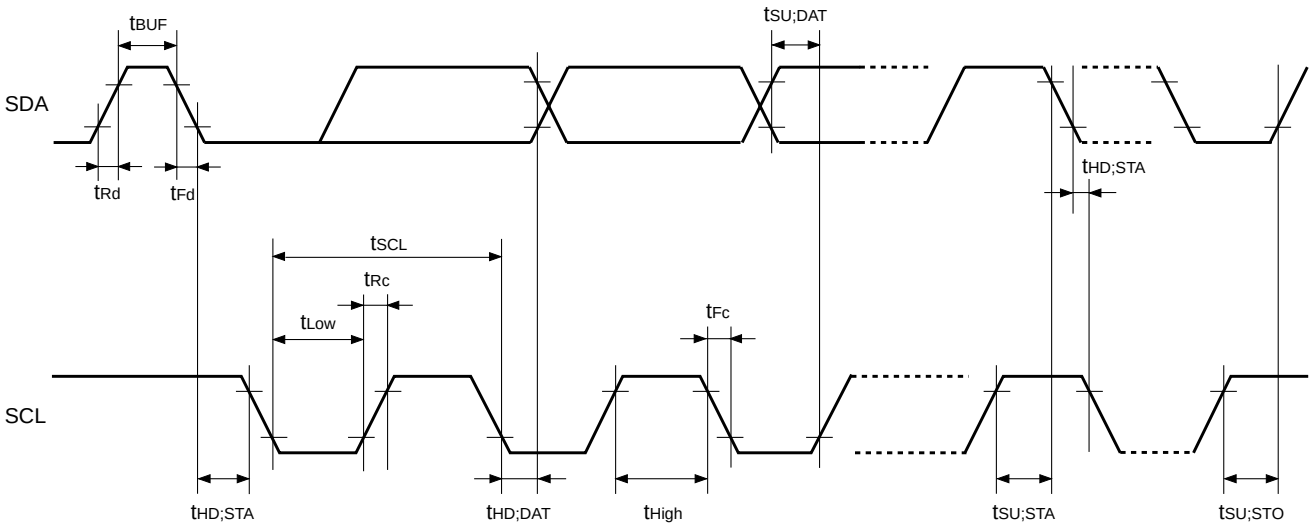


Fig. 8. I²C bus timing

(8) Remote control reception (Topr = –30 to +85°C, V_{DD} = 2.7 to 3.6V, Vss = 0V reference)

Item	Symbol	Pins	Conditions		Typ.	Max.	Unit
Remote control receive high, low level width	t_{RMC}	RMC	Main mode	PS5 selected	$128/f_{EX}$ + 100		ns
				PS7 selected	$512/f_{EX}$ + 100		
				PS9 selected	$2048/f_{EX}$ + 100		

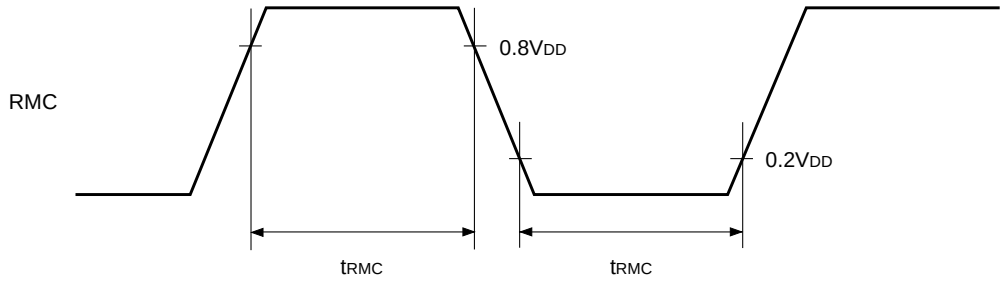


Fig. 9. Remote control signal input timing

(9) External register interface (Vss = 0V reference)

Item	Symbol	3.3 ± 0.3V Topr = –20 to +75°C		3.3 ± 0.3V Topr = –30 to +85°C		3.0 ± 0.3V Topr = –30 to +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Chip select pulse width 1	t_{CS1}	1.5tsys –20	1.5tsys	1.5tsys –20	1.5tsys	1.5tsys –30	1.5tsys	ns
Chip select pulse width 2	t_{CS2}	2.5tsys –20	16.5tsys	2.5tsys –20	16.5tsys	2.5tsys –30	16.5tsys	ns
Chip select pulse width 3	t_{CS3}	2.5tsys –20	32.5tsys	2.5tsys –20	32.5tsys	2.5tsys –30	32.5tsys	ns
Chip select pulse width 4	t_{CS4}	3.5tsys –20	33.5tsys	3.5tsys –20	33.5tsys	3.5tsys –30	33.5tsys	ns
Chip select pulse width 5	t_{CS5}	2.5tsys –20	17.5tsys	2.5tsys –20	17.5tsys	2.5tsys –30	17.5tsys	ns
Chip select pulse width 6	t_{CS6}	3.5tsys –20	18.5tsys	3.5tsys –20	18.5tsys	3.5tsys –30	18.5tsys	ns
Chip select pulse width 7	t_{CS7}	4.5tsys –20	34.5tsys	4.5tsys –20	34.5tsys	4.5tsys –30	34.5tsys	ns
Read/write strobe pulse width 1	t_{RW1}	tsys – 25	tsys	tsys – 25	tsys	tsys – 35	tsys	ns
Read/write strobe pulse width 2	t_{RW2}	2tsys – 25	16tsys	2tsys – 25	16tsys	2tsys – 35	16tsys	ns
Read/write strobe pulse width 3	t_{RW3}	2tsys – 25	32tsys	2tsys – 25	32tsys	2tsys – 35	32tsys	ns
Address setting time 1	t_{AS1}	tsys/2 –25	tsys/2	tsys/2 –25	tsys/2	tsys/2 –35	tsys/2	ns
Address setting time 2	t_{AS2}	1.5tsys –25	1.5tsys	1.5tsys –25	1.5tsys	1.5tsys –35	1.5tsys	ns
Address hold time	t_{AH}	tsys/2 –25	—	tsys/2 –25	—	tsys/2 –35	—	ns
Read data setting request time	t_{DS1}	15	—	15	—	20	—	ns
Read data hold request time	t_{DH1}	0	—	0	—	0	—	ns
Write data setting time 1	t_{DS2}	1.5tsys –25	1.5tsys	1.5tsys –25	1.5tsys	1.5tsys –35	1.5tsys	ns
Write data setting time 2	t_{DS3}	2.5tsys –25	16.5tsys	2.5tsys –25	16.5tsys	2.5tsys –35	16.5tsys	ns
Write data hold time	t_{DH2}	tsys/2 –25	tsys/2 +30	tsys/2 –25	tsys/2 +30	tsys/2 –35	tsys/2 +30	ns

Read Timing

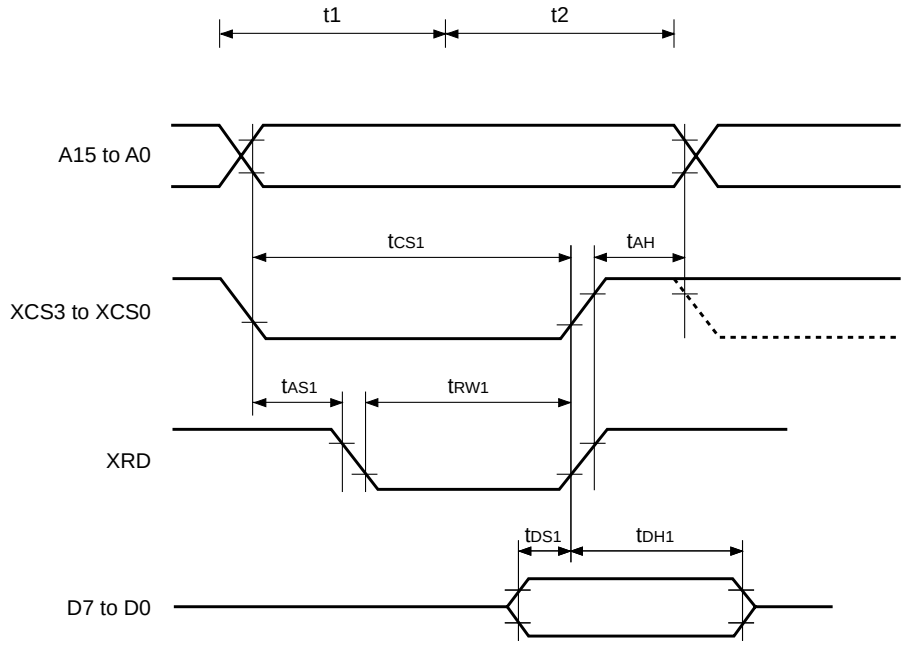


Fig. 10. Byte read (without programmable wait)

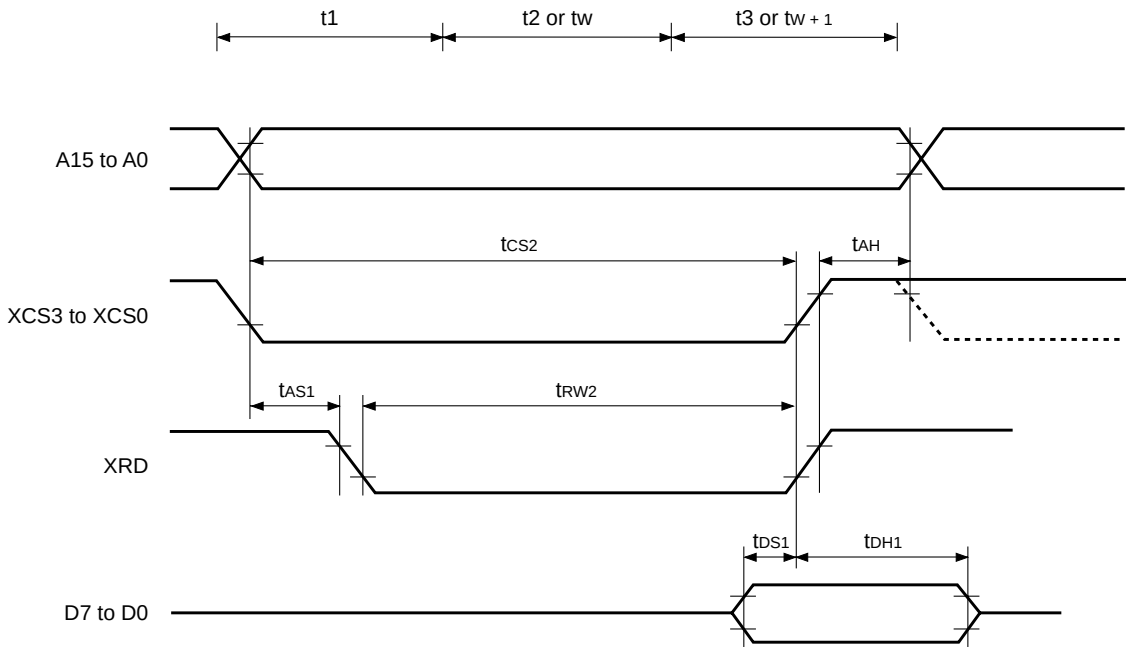


Fig. 11. Byte read (with programmable wait)

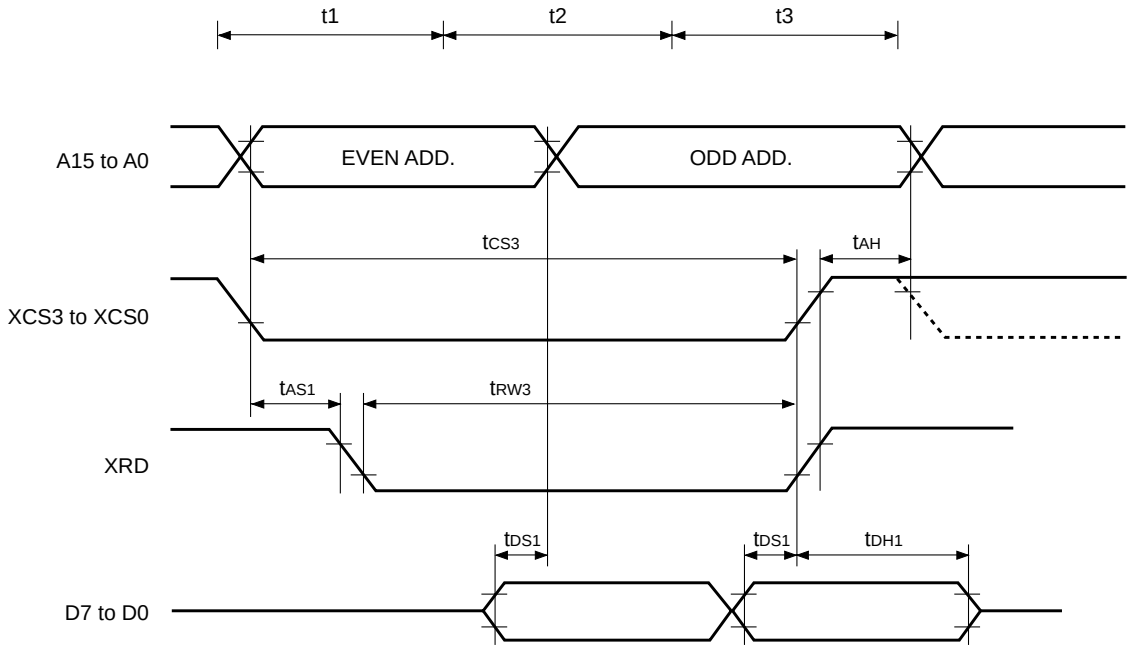


Fig. 12. Word read (no strobe mode, without programmable wait)

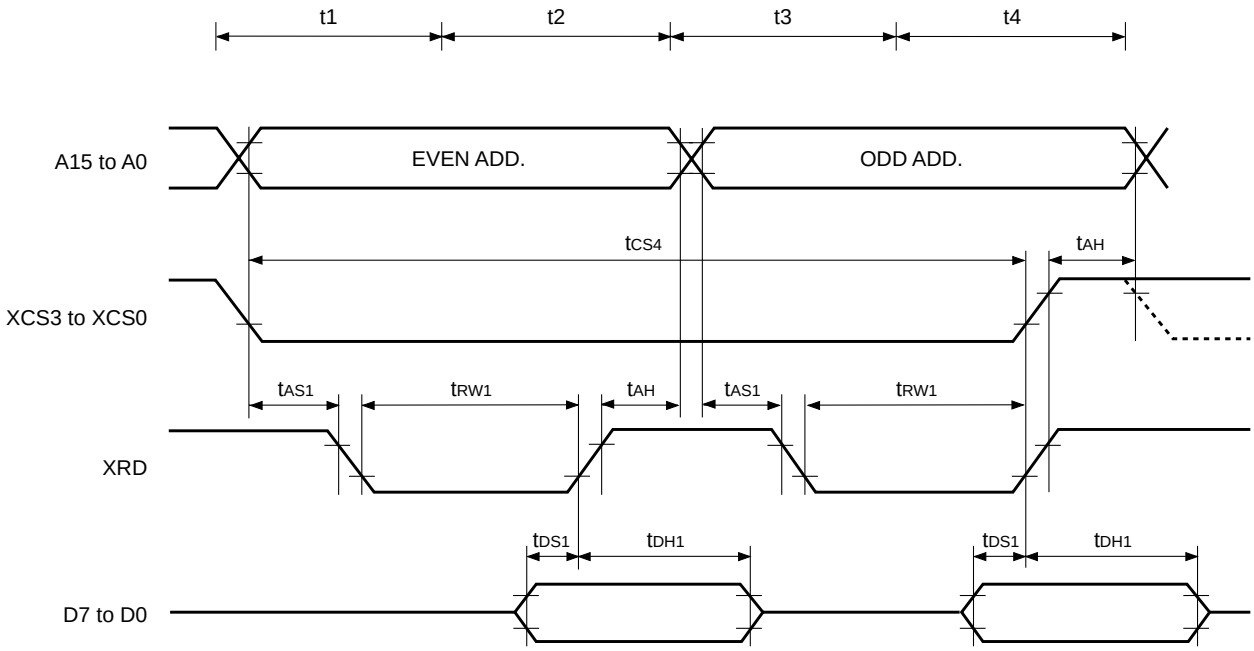


Fig. 13. Word read (strobe mode, without programmable wait)

Write Timing

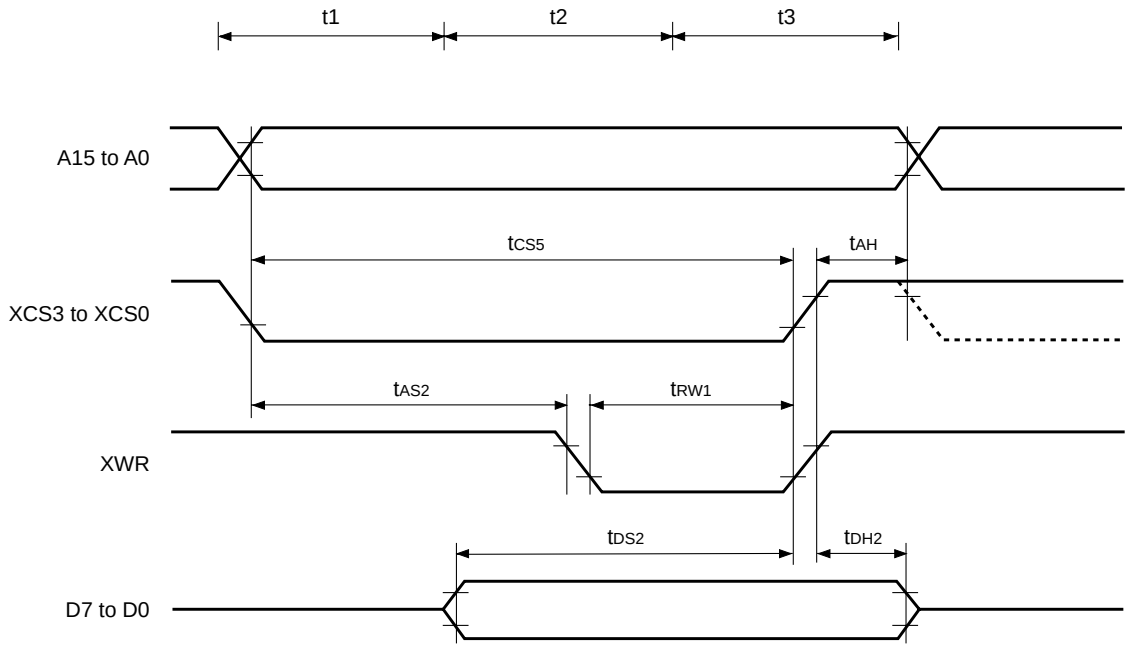


Fig. 14. Byte write (without programmable wait)

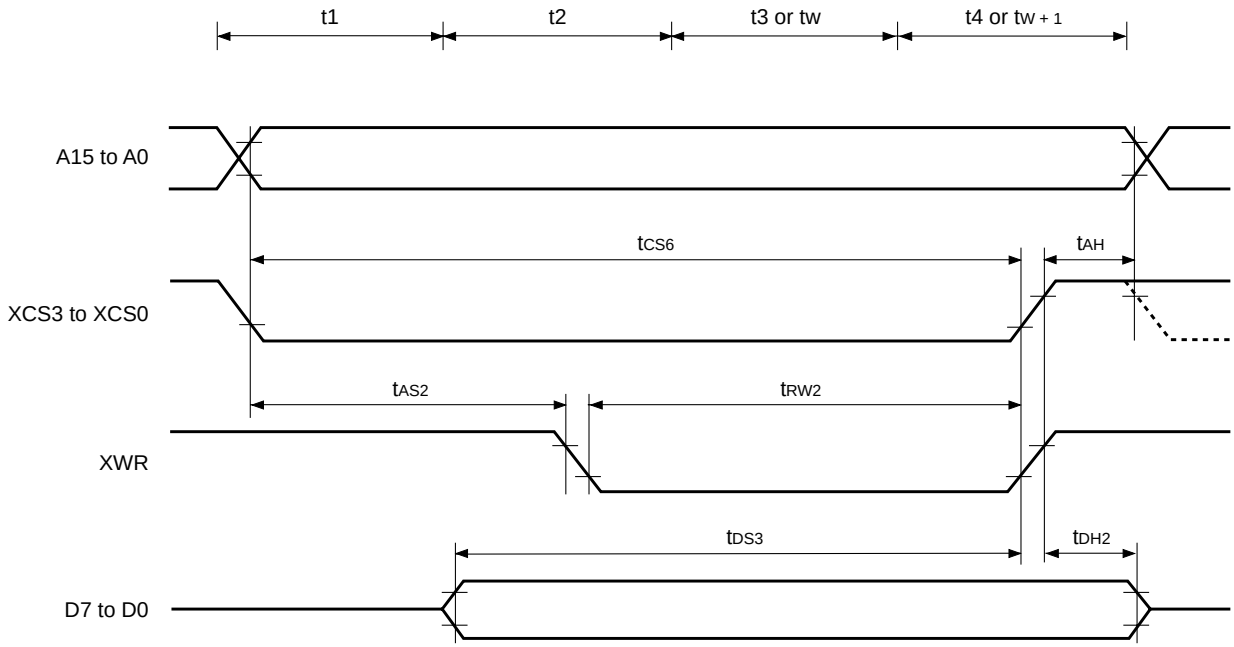


Fig. 15. Byte write (with programmable wait)

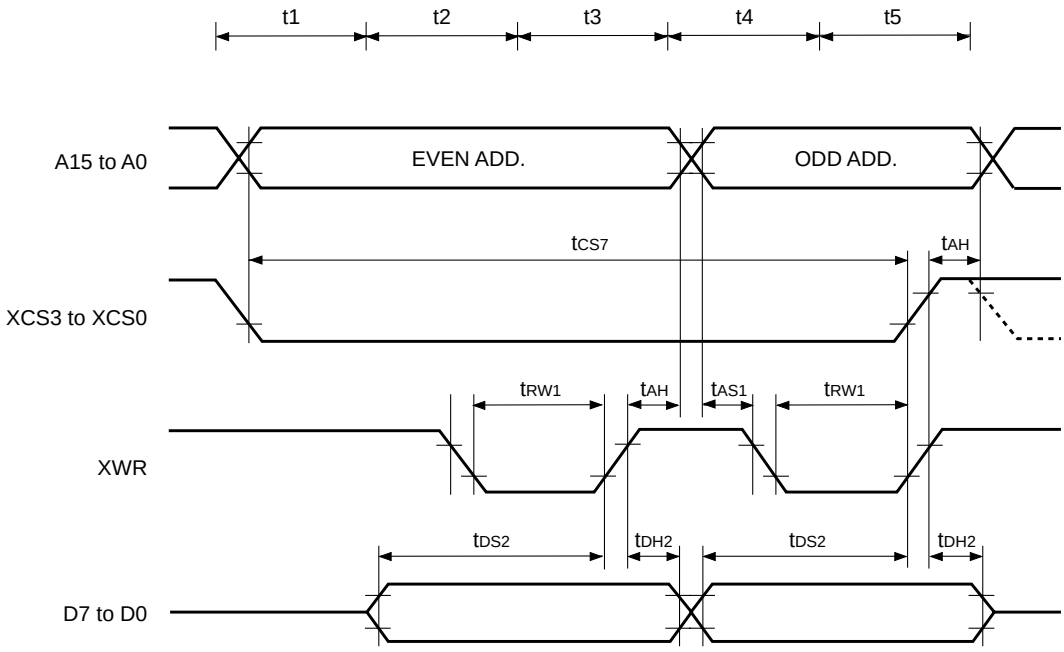


Fig. 16. Word write (without programmable wait)

Appendix

SPC970 Series recommended oscillation circuit and oscillator

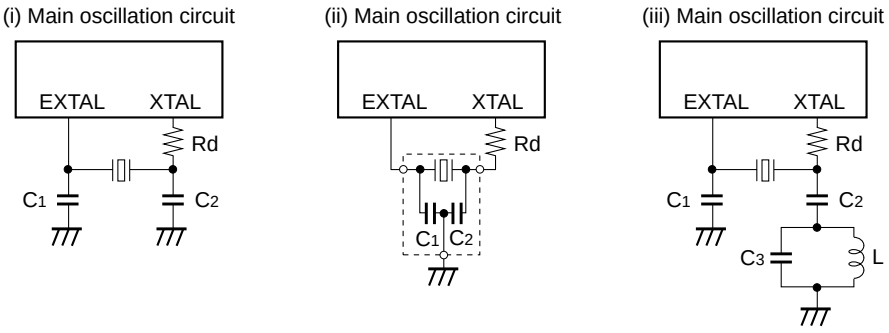


Fig. 17. Recommended oscillation circuit

Manufacturer	Model	f_{EX} (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA6.00MG040	6.0	100	100	0	(i)	
	CSA8.00MTZ	8.0	30	30	0		
	CSA10.0MTZ	10.0	30	30	0		
	CSA12.0MTZ	12.0	30	30	0		
	CSA16.00MXZ040	16.0	15	15	0		
	CSA20.00MXZ040	20.0	10	10	0		
	CSA24.00MXZ040	24.0	7	7	0		
	CST6.00MGW040*	6.0	100	100	0	(ii)	
	CST8.00MTW*	8.0	30	30	0		
	CST10.0MTW*	10.0	30	30	0		
	CST12.0MTW*	12.0	30	30	0		
	CST16.00MXW0C3*	16.0	15	15	0		
RIVER ELETEC CO., LTD.	HC-49/U03	6.0	18	18	560	(i)	CL = 13.5pF
		8.0	15	15	330		CL = 12pF
		10.0	10	10	330		CL = 9.5pF
		12.0	10	10	220		CL = 10pF

* Indicates types with on-chip grounding capacitor (C_1, C_2). CL: Load capacitor

Manufacturer	Model	f_{EX} (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example	Remarks
KINSEKI LTD.	HC-49/U-S	6.0	15	15	5.6k	(i)	CL = 16pF
		8.0	15	15	3.0k		
		10.0	10	10	1.8k		CL = 12pF
		12.0	12	12	1.0k		
		16.0	12	12	470		
		20.0	12	12	390		
		24.0	12	12	200		
		28.0	1	1	100		
	HC-49/U	32.0	3	0.01µF	0	(iii)	C3 = 10pF, L = 2.7µH
		36.0	3	0.01µF	0		C3 = 5pF, L = 2.7µH
		40.0	1	0.01µF	0		C3 = 3pF, L = 3.3µH
TDK Corporation	CCR6.0MC5*	6.0	36 (±20%)	36 (±20%)	0	(ii)	
	CCR12.0MSC5*	12.0	20 (±20%)	20 (±20%)	0		
	CCR16.0MSC6*	16.0	10 (±20%)	10 (±20%)	0		
	CCR28.0MSC6*	28.0	10 (±20%)	10 (±20%)	0		
	CCR40.0MS6	40.0	5	5	0	(i)	

* Indicates types with on-chip grounding capacitor (C_1, C_2).

CCR***: Surface mounted type ceramic oscillator

CL: Load capacitor

Product List

Type	Mask ROM
Product name	CXP974096
ROM capacitance	384K bytes
RAM capacitance	23.5K bytes
Package	100-pin plastic QFP, 100-pin plastic LQFP
Main clock base oscillation frequency*1	Less than 40MHz, Less than 20MHz
Reset pin pull-up resistor	Existent/Non-existent

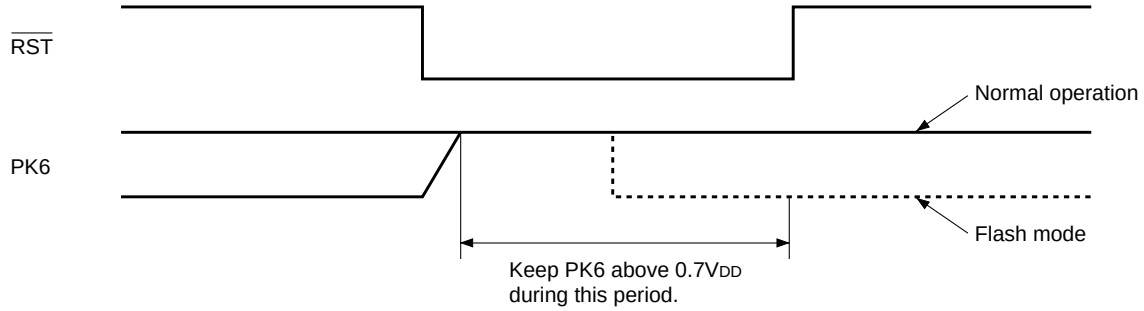
*1 When the main clock base oscillation frequency is specified below 20MHz, operation is not performed even though higher external oscillation and higher external input frequency than the upper limit of clock timing specification are applied.

Notes on PK6 Usage

FLASH EEPROM incorporated PK6 is also used as flash mode setting function. Note the followings:

1. "H" is output to PK6 during a reset. That is driven at comparatively high impedance (approximately 150kΩ), and take care that V_{OH} should not fall under $0.7V_{DD}$ by the partial pressure with external circuit load impedance.

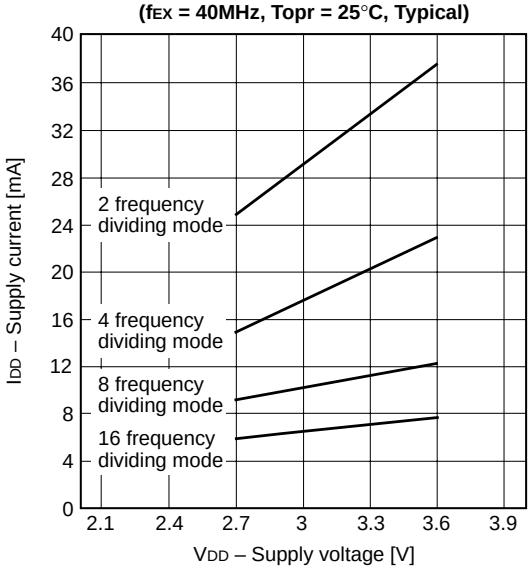
2. When using software reset functions, PK6 may not rise enough during a reset. Switching PK6 to "H" output prior to software reset execution or connecting pull-up resistor is recommended.



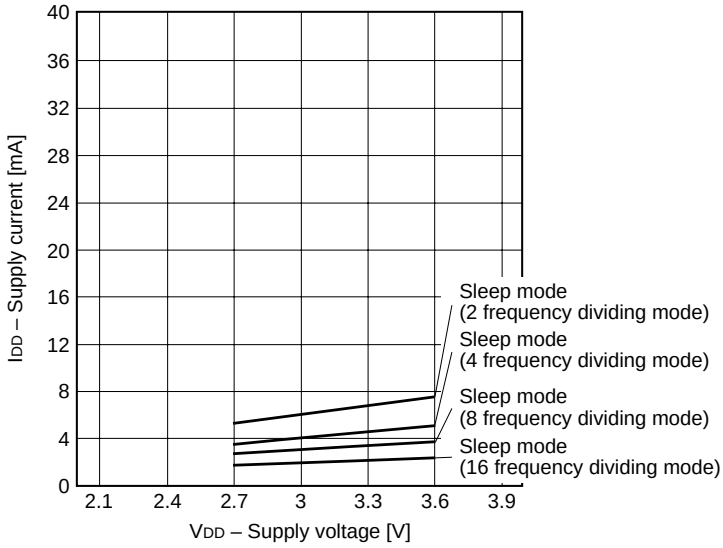
Mask ROM and piggy/evaluation chip do not have flash mode setting function. Considering that FLASH EEPROM incorporated version is used, above countermeasure should be performed.

Characteristics Curve

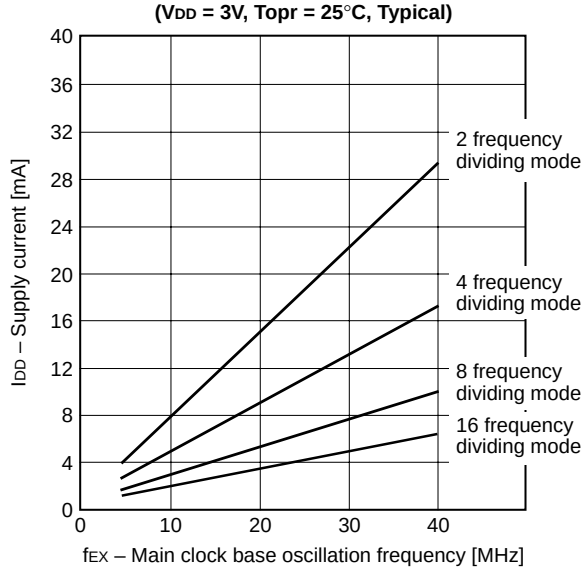
IDD vs. VDD
(fEX = 40MHz, Topr = 25°C, Typical)



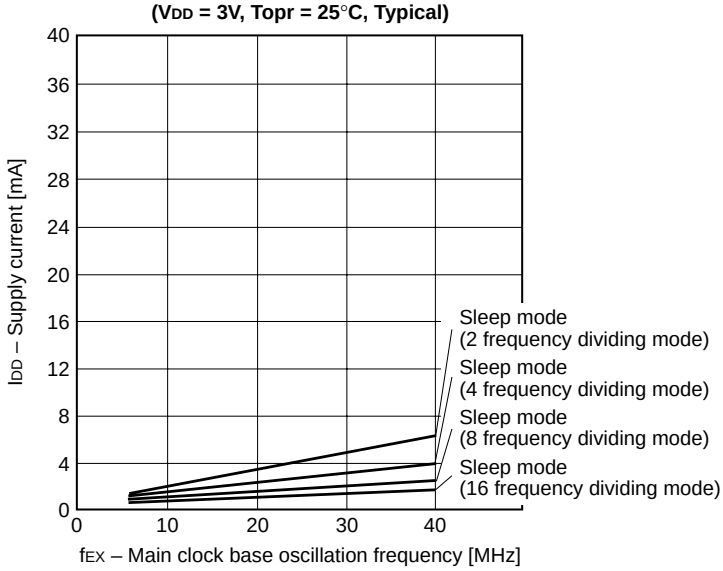
IDD vs. VDD
(fEX = 40MHz, Topr = 25°C, Typical)



IDD vs. fEX
(VDD = 3V, Topr = 25°C, Typical)

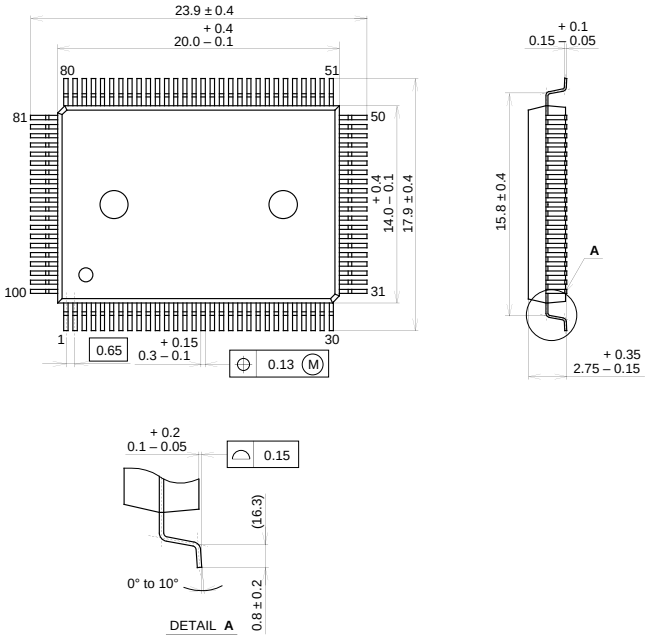


IDD vs. fEX
(VDD = 3V, Topr = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)



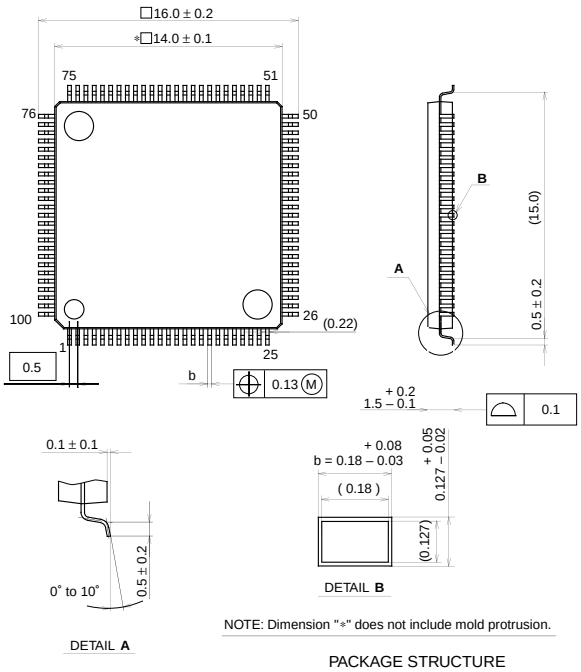
SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

Package Outline Unit: mm

100PIN LQFP (PLASTIC)



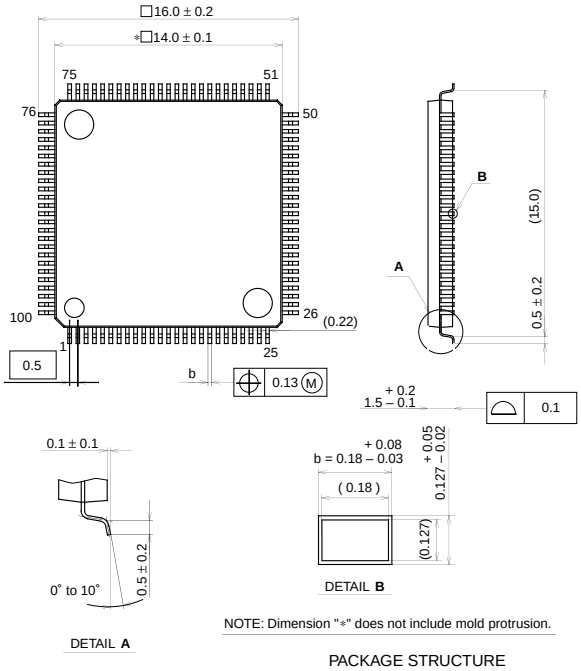
NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

100PIN LQFP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	P-LQFP100-14x14-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.7g

LEAD SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	ALLOY 42
LEAD TREATMENT	Sn-Bi 2.5%
LEAD TREATMENT THICKNESS	5-18µm