M62383FP

5 V Composite Type D-A Converter

REJ03F0076-0100Z
Rev.1.0
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Description

The M62383FP is a 5 V composite D-A converter incorporating two modules, with two 8-bit buffer amp output D-A converters and an 8-bit D-A converter for reference voltage adjustment as one module.

The D-A outputs can be set simultaneously for each module without address setting. The data configurations comprise 16-bit serial data for the two main D-A circuits and 8-bit serial data for the reference voltage setting D-A. The D-A output buffer amps have full-swing output capability, from power supply voltage to GND.

Features

- Simultaneous dual-output data setting by means of 16-bit serial data (TTL level)
- Data transfer clock frequency: 10 MHz (max.)
- D-A converter output settling time: 5 µs (typ.)
- Power-on reset and external reset (L reset) functions
  (D-A output = 0 V, MON output = VREF × 255/256)

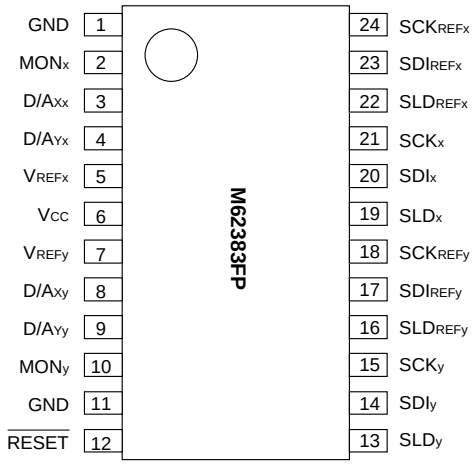
Application

Automatic adjustment of electronic devices

Recommended Operating Conditions

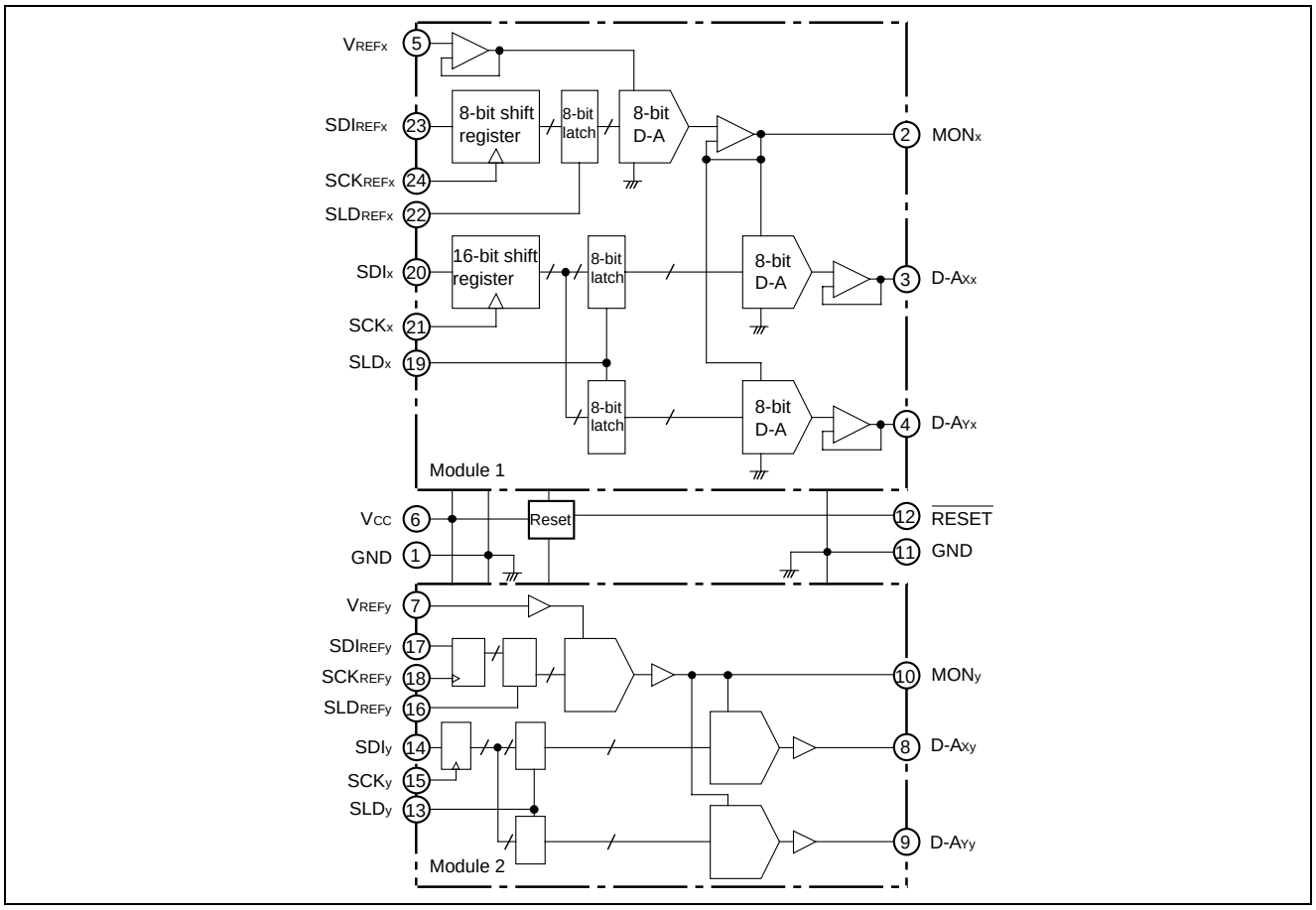
Power supply voltage: 5 V ±10%

Pin Connection Diagram (Top View)



Package: 24P2Q-A

Block Diagram



Pin Description

Pin No.	Symbol	Function	
1, 11	GND	Ground (GND) pin	
2	MONx	Module 1: Reference voltage D-A output pin	
10	MONy	Module 2: Reference voltage D-A output pin	
3	D/Axx	Module 1: 8-bit D-A output pin (x side)	
4	D/Axy	Module 1: 8-bit D-A output pin (y side)	
8	D/Ayx	Module 2: 8-bit D-A output pin (x side)	
9	D/Ayy	Module 2: 8-bit D-A output pin (y side)	
5	VREFx	Module 1: Reference voltage input pin	
7	VREFy	Module 2: Reference voltage input pin	
6	Vcc	Power supply (VCC) pin	
12	$\overline{\text{RESET}}$	Reset pin	When input level is changed from “H” to “L”, D-A output becomes 0 V (D-A data: 00h), and MON output becomes VREF × 255/256 (MON data: FFh). Even if input level is restored from “L” to “H”, output is maintained until next data setting. TTL-based.
19	SLDx	Module 1: Load signal input pin	At rising edge of input signal from “L” to “H”, data in 16-bit shift register is loaded into D/A data register. TTL-based.
13	SLDy	Module 2: Load signal input pin	
22	SLDREFx	Module 1: Reference voltage load signal input pin	At rising edge of input signal from “L” to “H”, data in 8-bit shift register is loaded into D/A data register. TTL-based.
16	SLDREFy	Module 2: Reference voltage load signal input pin	
20	SDIx	Module 1: Serial data input pin	TTL-based 16-bit-length serial data
14	SDIy	Module 2: Serial data input pin	
23	SDIREFx	Module 1: Reference voltage serial data input pin	TTL-based 8-bit-length serial data
17	SDIREFy	Module 2: Reference voltage serial data input pin	
21	SCKx	Module 1: Shift clock signal input pin	TLL Schmitt trigger based serial clock input SDI serial data is sent to 16-bit shift register one bit at a time at each rise.
15	SCKy	Module 2: Shift clock signal input pin	
18	SCKREFx	Module 1: Reference voltage shift clock signal input pin	TLL Schmitt trigger based serial clock input SDIREF serial data is sent to 8-bit shift register one bit at a time at each rise.
24	SCKREFy	Module 2: Reference voltage shift clock signal input pin	

Absolute Maximum Ratings

(Unless specified otherwise, Ta = 25ºC)

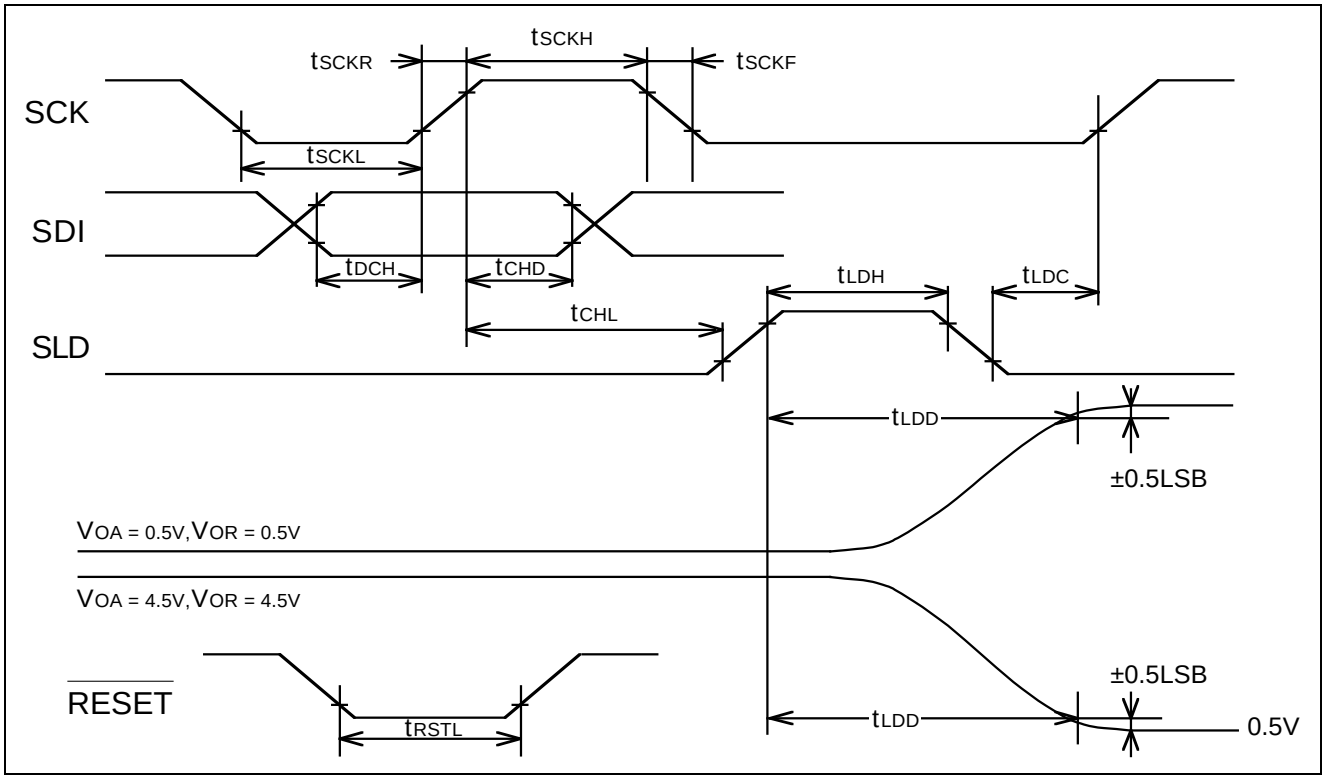
Item	Symbol	Rated Value	Unit	Conditions
Power supply voltage	VCC	-0.3 to 7.0	V	
Digital input voltage	VDIN	-0.3 to Vcc+0.3 (≤ 7.0)	V	DC voltage (“H” level voltage)
Reference voltage input voltage	VREF	-0.3 to Vcc+0.3 (≤ 7.0)	V	
Output voltage	VDAout	-0.3 to Vcc+0.3 (≤ 7.0)	V	
Internal permissible loss	Pd	500	mW	
Operating ambient temperature	Topr	-20 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

Recommended Operating Conditions

(Unless specified otherwise, VCC = 5 V ±10%, VREF = VCC, fSCK = 5 MHz, VIH = VCC, VIL = GND, Ta = 25ºC)

		Specification Values				
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Power supply voltage	Vcc	4.5	5.0	5.5	V	
Reference power supply voltage	VREF	GND		Vcc	V	VCC voltage or below
Clock frequency	fSCK			10	MHz	
“H” level input voltage	VIH	2		Vcc	V	TTL “H” input level
“L” level input voltage	VIL	GND		0.8	V	TTL “L” input level
Clock input hysteresis voltage	VΔ	0.4	0.6	1.0	V	TTL Schmitt trigger
Clock “L” pulse width	tSCKL	30		450	ns	See timing chart
Clock “H” pulse width	tSCKH	30		450	ns	See timing chart
Clock rise time	tSCKR	10		100	ns	See timing chart
Clock fall time	tSCKF	10		100	ns	See timing chart
Data setup time	tDCH	10		100	ns	See timing chart
Data hold time	tCHD	20		200	ns	See timing chart
Load setup time	tCHL	40		800	ns	See timing chart
Load hold time	tLDC	20		400	ns	See timing chart
Load “H” pulse time	tLDH	20		400	ns	See timing chart
Reset “H” pulse time	tRSTL	50			ns	See timing chart

Timing Chart



Electrical Characteristics

(Unless specified otherwise, VCC = 5 V ±10%, VREF = VCC, fSCK = 5 MHz, VIH = VCC, VIL = GND, Ta = -20ºC to 85ºC)

(a) Common to analog and digital blocks

		Specification Values				
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Circuit current	Icc		6.0	10	mA	

(b) Digital block

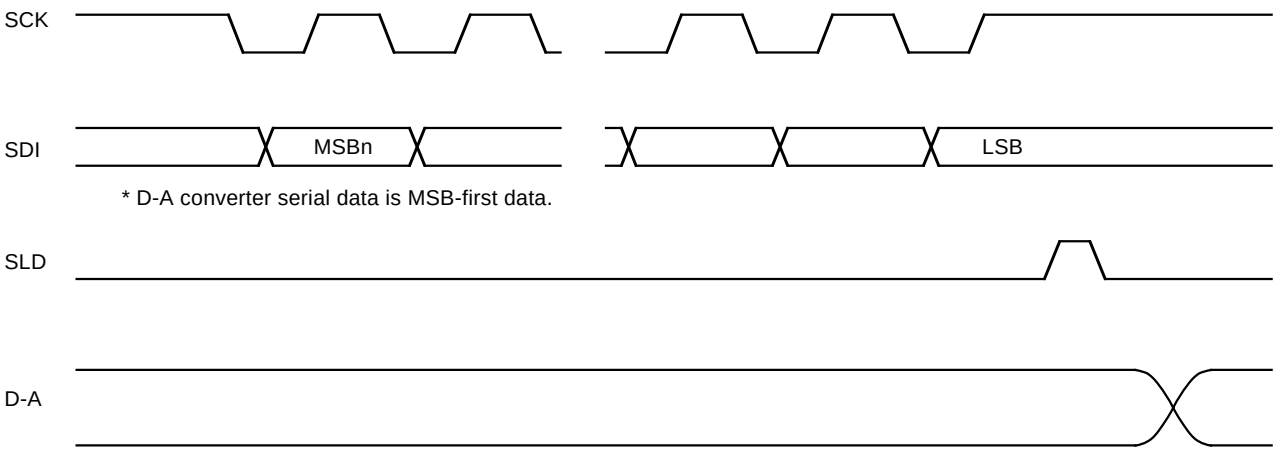
		Specification Values				
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Test Conditions**
Input leakage current	IILK	–10		10	µA	VIN = 0V to 5V

(c) Analog block

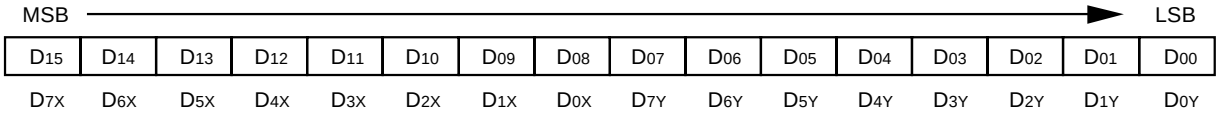
Item	Symbol	Specification Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Reference voltage input voltage	VREF	GND		Vcc	V	When SDIREF is set to (FF)h, VREF = MON
Reference voltage input current	IREF	–1		+1	µA	GND≤VREF≤Vcc
Upper reference voltage output voltage (*1)	VORU	4.88	4.98	Vcc	V	SDIREF = (FF)h, SDI = (FFFF)h, MON output value
Lower reference voltage output voltage (*1)	VORL	GND		0.10	V	SDIREF = (00)h, SDI = (FFFF)h, MON output value
Reference voltage output offset voltage (*1)	ΔVOR	–100		100	mV	VREF = 2 to 5V, SDI = (FFFF)h, 255/256VREF-VOR (MON output value)
Upper buffer amp D-A output voltage	VOAU	4.5			V	IOA = ±0.5mA, SDIREF = (FF)h, SDI = (FFFF)h
Lower buffer amp D-A output voltage	VOAL			0.05	V	IOA = ±0.5mA, SDIREF = (FF)h, SDI = (0000)h
Accuracy: Differential nonlinearity error	SDL	–1.0		+1.0	LSB	(Monotone increasing capability)
Accuracy: Nonlinearity error	SNL	–1.0		+1.0	LSB	
Accuracy: Zero scale error	SZERO	–2.0		+2.0	LSB	VREF = 2 to 5 V: Buffer output offset (*2)
Accuracy: Full-scale error	SFULL	–2.0		+2.0	LSB	VREF = 2 to 5 V: Buffer output offset (*2)
Reference voltage input pin capacitance	CREF			10	pF	
D-A converter output settling time	tLDDA		5	10	µS	VOA = 0.5↔4.5V, IOA = 0.1mA, Co = 50pF, SDIREF = (FF)h, Time for output to be absorbed within ±0.5 LSB
Reference voltage output settling time	tLDDR		10	20	µS	VOA = 0.5↔4.5V, no external load Time for output to be absorbed within ±0.5 LSB
Power-on reset voltage (*3)	$V\overline{RESET}$	0.8	1.5	3	V	Vcc = 0→5V, VOA = 0V, VOR = VREF×255/256 set

Notes: 1. MON output specification. Equivalent to ±5 LSB.
2. D-A output (D-Axx, D-Axy, D-Ayx, D-Ayy) specification. MON output is stipulated by 3 items in *1 above (VORU, VORL, ΔVOR).
3. Reference values

Digital Data Format



SDIx, SDIy

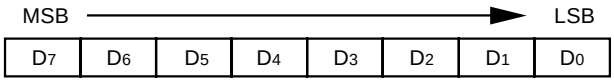


$$V_{OA} = V_{OR} \times \frac{2^7 \times D_7 * + 2^6 \times D_6 * + 2^5 \times D_5 * + 2^4 \times D_4 * + 2^3 \times D_3 * + 2^2 \times D_2 * + 2^1 \times D_1 * + 2^0 \times D_0 *}{256}$$

V_{OA}: D-A output voltage
V_{OR}: MON output voltage

Dn*: D-A data
n = 0 to 7, * = x, y

SDIREFx, SDIREF



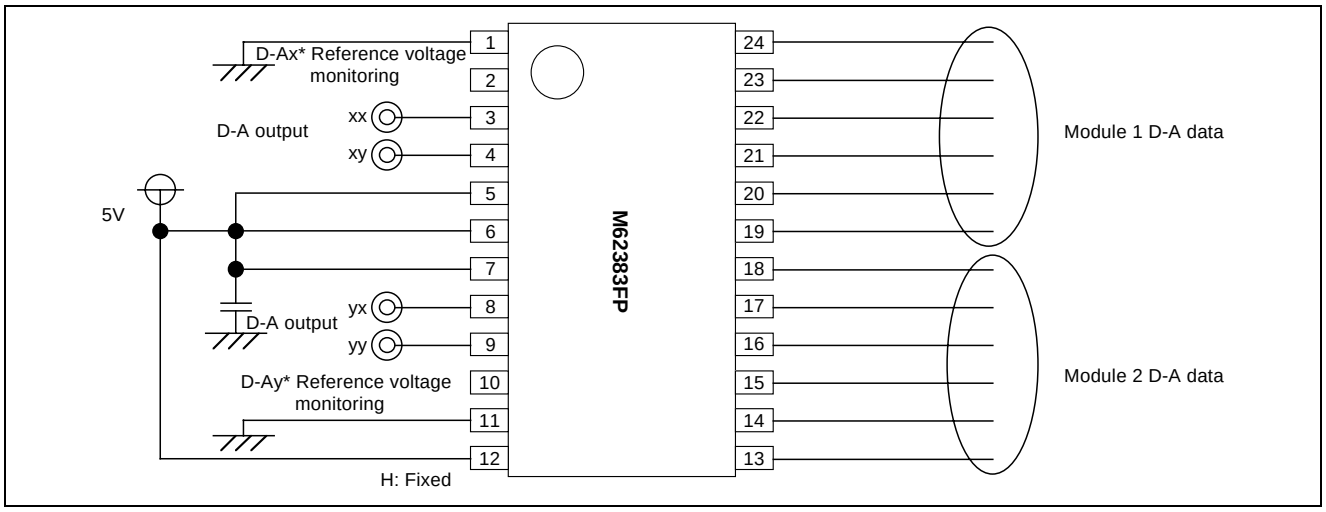
$$V_{OA} = V_{REF} \times \frac{2^7 \times D_7 + 2^6 \times D_6 + 2^5 \times D_5 + 2^4 \times D_4 + 2^3 \times D_3 + 2^2 \times D_2 + 2^1 \times D_1 + 2^0 \times D_0}{256}$$

V_{OR}: MON output voltage
V_{REF}: Reference voltage

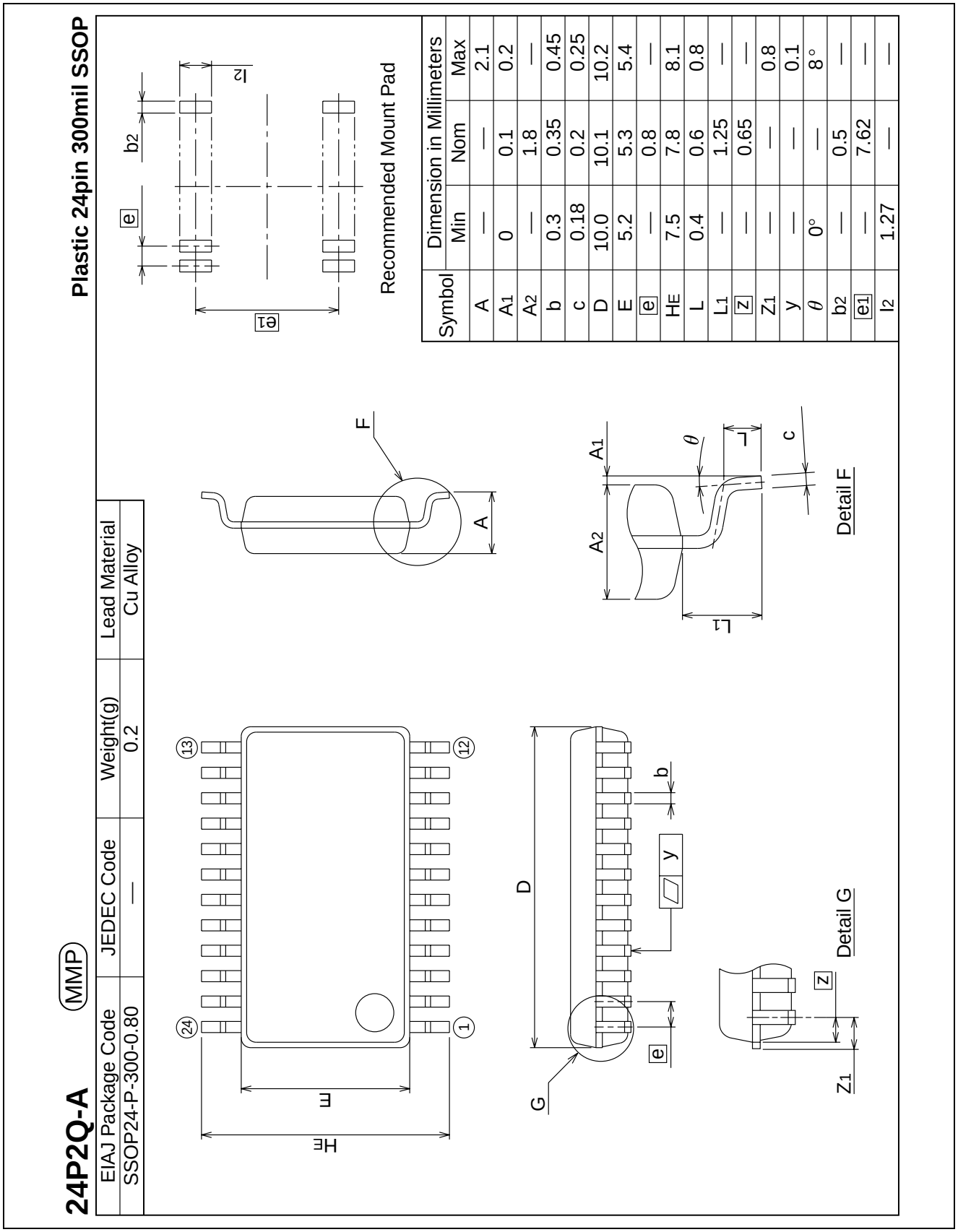
Usage Notes

1. This IC has three pins to which a constant voltage is applied during use (constant-voltage input pins: VCC, VREFx, VREFy). If ripples or spikes are imposed on these pins, D-A conversion accuracy may fall. When using this IC, a capacitor (1 µF or higher recommended) must be inserted between the constant-voltage input pins and ground (GND) in order to ensure stable D-A conversion.
2. With regard to the reset function (power-on reset), when the power supply voltage passes the vicinity of 1.5 V at power-on, the D-A output voltage (VOA) becomes 0 V (D-A data: 00h), and the MON output voltage (VOR) becomes VREF × 255/256 (MON data: FFh), and output is maintained until the next data is set. In the event of repeated power supply on/off operations at short intervals, a reset may not be effected because of the simplicity of the circuit.

Sample Standard Application Circuit



Package Dimensions



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