YAMAHA

YDA144

D-4N

STEREO 2.1W Non-Clip DIGITAL AUDIO POWER AMPLIFIER

■Overview

YDA144 (D-4N) is a digital audio power amplifier IC with maximum output of 2.1W (R_L=4Ω)×2ch.
YDA144 has a "Pure Pulse Direct Speaker Drive Circuit" which directly drives speakers while reducing distortion of pulse output signal and reducing noise on the signal, and realizes the highest standard low distortion rate characteristics and low noise characteristics among digital amplifier ICs for mobile use.
In addition, circuit design with fewer external parts can be made depend on the condition of use because corresponds to filter less.
The YDA144 features Yamaha original non-clip output control function which detects output signal clip due to the over level input signal and suppress the output signal clip automatically. Also the non-clip output control function can adapt the output clip caused by power supply voltage down with battery. This is the difference from the traditional AGC (Auto Gain Control) or ALC (Auto Level Control) circuit. Attack time and release time can be freely set by external resistances or capacitances.
The independent power-down function for L channel and R channel minimizes consumption current at standby. As for protection function, overcurrent protection function for speaker output terminal, overtemperatue protection function for inside of the device, and low supply voltage malfunction preventing function are prepared.

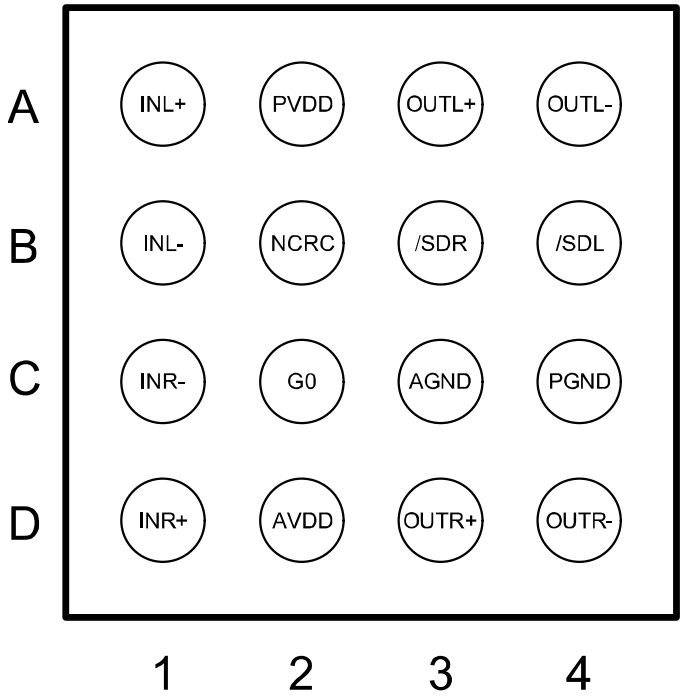
■Features

- Maximum output
  2.1 W×2ch (V_{DDP}=V_{DDA}=5.0V, R_L=4Ω, THD+N=10%)
  0.75 W×2ch (V_{DDP}=V_{DDA}=3.6V, R_L=8Ω, THD+N=10%)
- Distortion Rate (THD+N)
  0.03 % (V_{DDP}=V_{DDA}=3.6V, R_L=8Ω, Po=0.4W, 1kHz)
- Residual Noise
  40μVrms (V_{DDP}=V_{DDA}=3.6V, Av=12dB)
- Efficiency
  84 % (V_{DDP}=V_{DDA}=3.6V, R_L=8Ω, Po=600mW)
  78 % (V_{DDP}=V_{DDA}=3.6V, R_L=8Ω, Po=100mW)
- S/N Ratio
  95dB (V_{DDP}=V_{DDA}=3.6V, Av=12dB)
- Channel separation
  95dB (V_{DDP}=V_{DDA}=3.6V, R_L=8Ω, Av=18dB, 1kHz)
- Over-current Protection function
- Thermal Protection function
- Low voltage Malfunction Prevention function
- 2ch independent power-down control function
- Power-down High speed Recovery function
- Package
  Lead-free 16-ball WLCSP (YDA144-WZ)
  Lead-free 20-pin QFN (YDA144-QZ)

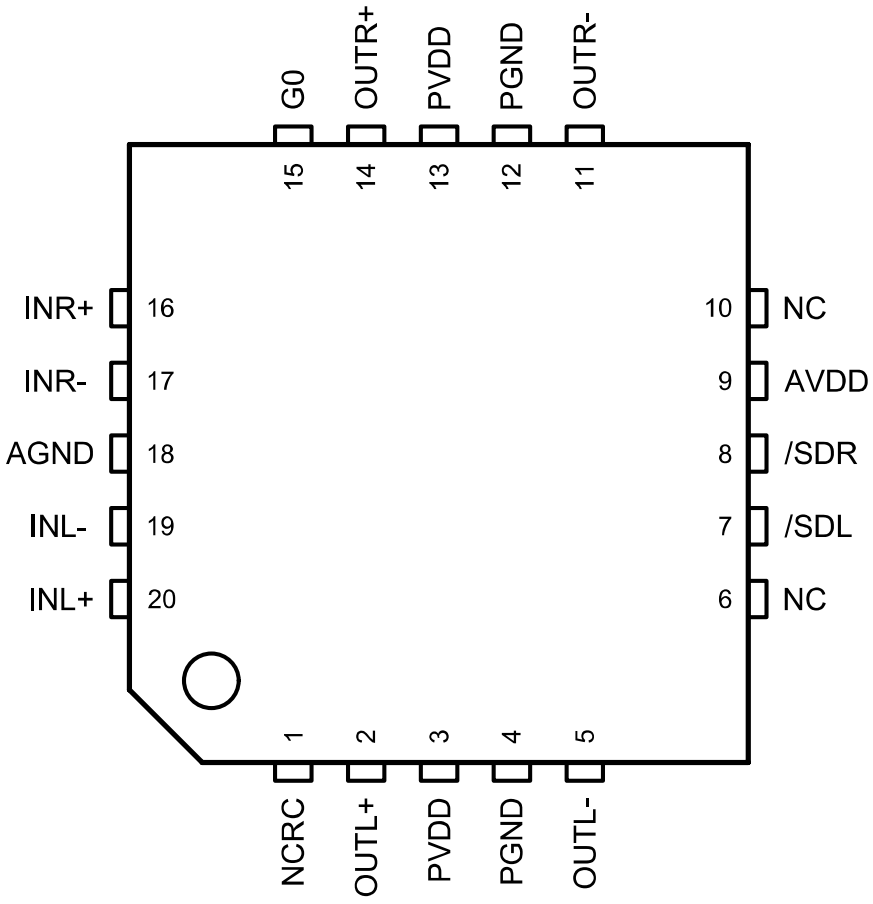
YAMAHA CORPORATION

YDA144 CATALOG
CATALOG No.:LSI-4DA144A30
2006.11

■Terminal configuration



<16-ball WLCSP Top View>



<20-pin QFN Top View>

■Terminal function

・WLCSP16

No.	Name	I/O	Protection circuit composition	Function
A1	INL+	A	PN	Positive input terminal (differential +) Lch
A2	PVDD	Power	-	Power supply for output
A3	OUTL+	O	-	Positive output terminal (differential +) Lch
A4	OUTL-	O	-	Negative output terminal (differential -) Lch
B1	INL-	A	PN	Negative input terminal (differential -) Lch
B2	NCRC	I/O	PN	Non-Clip control terminal
B3	/SDR	I	N	Shut-down terminal for Rch
B4	/SDL	I	N	Shut-down terminal for Lch
C1	INR-	A	PN	Negative input terminal (differential -) Rch
C2	G0	I	N	Gain setting terminal
C3	AGND	GND	-	GND for analog circuits
C4	PGND	GND	-	GND for output
D1	INR+	A	PN	Positive input terminal (differential +) Rch
D2	AVDD	Power	-	Power supply for analog circuits
D3	OUTR+	O	-	Positive output terminal (differential +) Rch
D4	OUTR-	O	-	Negative output terminal (differential -) Rch

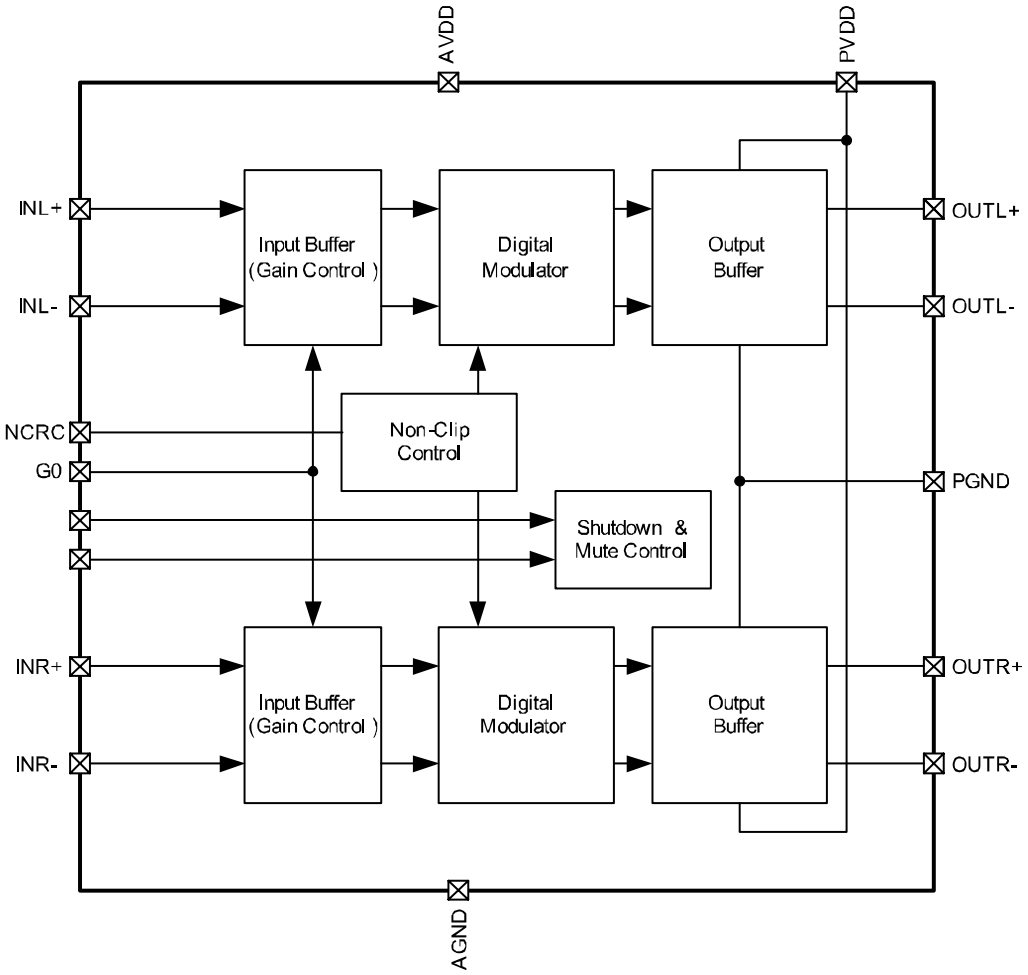
(Note) I: Input terminal O: Output terminal A: Analog terminal
When a voltage that is bigger than the AVDD potential is impressed to the terminal of PN (protection circuit is composed of PMOS and NMOS), the leakage current flows through the protection circuit of PMOS.

・QFN20

No.	Name	I/O	Protection circuit composition	Function
1	NCRC	I/O	PN	Non-Clip control terminal
2	OUTL+	O	-	Positive output terminal (differential +) Lch
3	PVDD	Power	-	Power supply for output
4	PGND	GND	-	GND for output
5	OUTL-	O	-	Negative output terminal (differential -) Lch
6	NC	-	-	Non connection or connect to AGND
7	/SDL	I	N	Shut-down terminal for Lch
8	/SDR	I	N	Shut-down terminal for Rch
9	AVDD	Power	-	Power supply for analog circuits
10	NC	-	-	Non connection or connect to AGND
11	OUTR-	O	-	Negative output terminal (differential -) Rch
12	PGND	GND	-	GND for output
13	PVDD	Power	-	Power supply for output
14	OUTR+	O	-	Positive output terminal (differential +) Rch
15	G0	I	N	Gain setting terminal
16	INR+	A	PN	Positive input terminal (differential +) Rch
17	INR-	A	PN	Negative output terminal (differential -) Rch
18	AGND	GND	-	GND for analog circuits
19	INL-	A	PN	Negative input terminal (differential -) Lch
20	INL+	A	PN	Positive input terminal (differential +) Lch

(Note) I: Input terminal O: Output terminal A: Analog terminal
When a voltage that is bigger than the AVDD potential is impressed to the terminal of PN (protection circuit is composed of PMOS and NMOS), the leakage current flows through the protection circuit of PMOS.

■Block diagram



■Description of operating functions

●Digital Amplifier Function

YDA144 has digital amplifiers with analog and digital input, PWM pulse output, Maximum output of 2.1W(R_L=4Ω)×2ch. Distortion of PWM pulse output signal and noise of the signal is reduced by adopting "Pure Pulse Direct Speaker Drive Circuit"
In addition, YDA144 has been designed so that high-efficiency can be maintained within an average power range (100mW or so) that is used for mobile terminal.

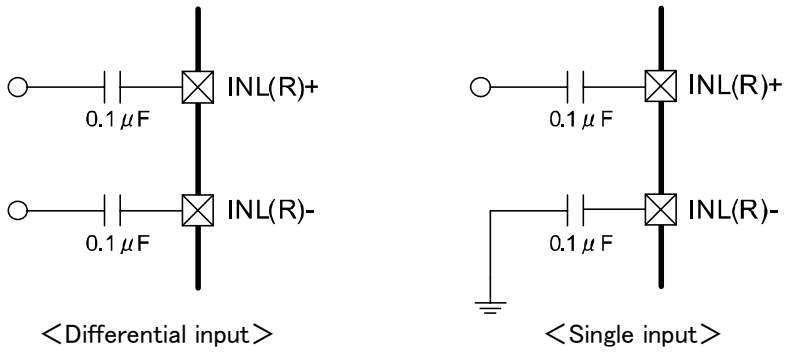
First Stage Amplifier Gain Setting Function
G0 terminal can set the Gain of YDA144. When Non-Clip function is disabled, the relation between G0 terminal setting and Gain is as follows.

Digital Amplifier Gain Setting

G0	Gain	Input Impedance(Z_{IN})
L	12dB	44kΩ
H	18dB	28kΩ

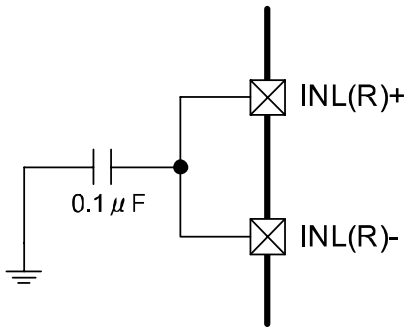
Note） H and L indicates logic High and logic Low, respectively.

Input Lch differential input signals to INL+ terminal and INL- terminal through DC-cut capacitors (C_{IN}). For single ended operation, input the signal to INL+ pin through the DC-cut capacitor (C_{IN}). At this time, INL- pin must be connected to AVSS pin through a capacitor (C_{REF}: same value as C_{IN}). As with Lch, connect input signals to Rch.



＜Differential input＞ ＜Single input＞

In addition, positive (+) and negative (-) sides of differential input pins (INL+ and INL-, or INR+ and INR-), input pins of the unused channel side, should be connected to each other and connected to AVSS through a capacitor.
Use a capacitor with the same capacitance (0.1μF) as that of a DC-cut capacitor in the channel side being used.



＜Input terminal processing of unused channel side＞

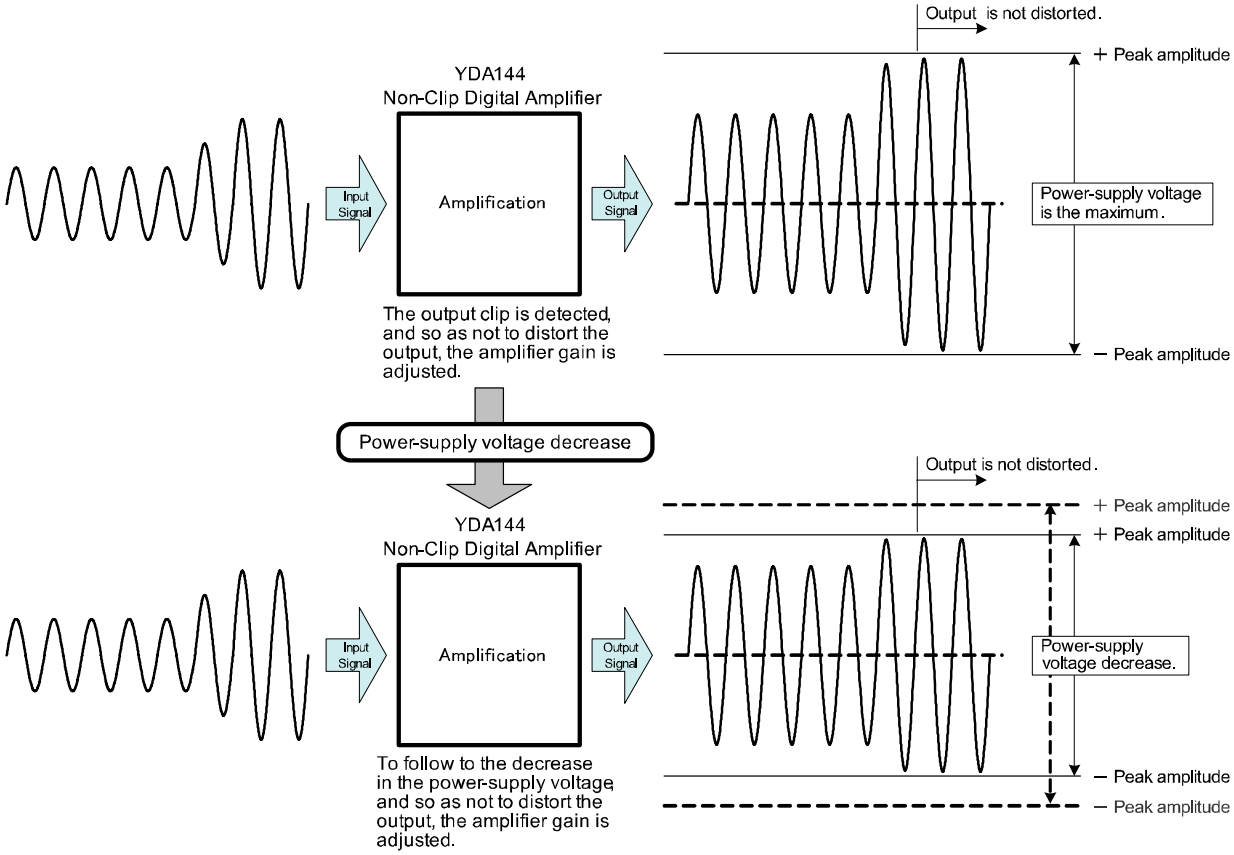
The lower cut-off frequency (fc) can be found from DC-cut capacitor (C_{IN}) and input impedance (Z_{IN}) as shown below.

$$fc=1/(2*\pi*Z_{IN}*C_{IN})$$

In order to reduce pop-noise, impedance in the differential input signal source is arranged. And, DC-cut capacitor (C_{IN}) should be 0.1μF or less.

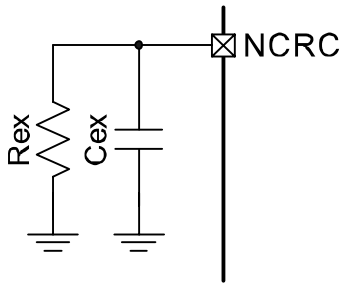
●Non-Clip control Function

This is the function to control the output in order to obtain a maximum output level without distortion when an excessive input which causes clipping at the differential signal output is applied. That is, with the Non-Clip function, YDA144 lowers the Gain of the digital amplifier to an appropriate value so as not to cause the clipping at the differential signal output.
And, YDA144 follows also to the clip of the output wave form due to the decrease in the power-supply voltage.



<Operation outline of Non-Clip control function>

Connecting a resistor (Rex) and a capacitor (Cex) to NCRC terminal can set Attack Time and Release Time of the Non-Clip control. A temperature compensation type ceramic capacitor is recommended as capacitor (Cex).



The Attack time is a time interval until gain falls to target attenuation gain -3dB with a big signal input enough.
And, the Release Time is a time from target attenuation gain to not working of Non-Clip.
With the target attenuation gain of 10dB, the Attack Time and Release Time is as can above Table.

Resistor(Rex), Capacitor(Cex) and Attack Time, Release Time

Rex(MΩ)	1	4.7	1	1
Cex(μF)	1	1	0.47	4.7
Attack Time(ms)	10	10	4.7	47
Release Time(s)	0.8	3.8	0.38	3.8

Non-Clip control function can be invalidated by the NCRC terminal assumption H level fixation (AVDD potential) or L level fixation (GND). In that case, the following differences exist by the state of the NCRC terminal.

Difference of operation by state of NCRC terminal when Non-Clip control function is OFF.

NCRC terminal	Current increase [mA]	Start up wait time [sec]	Non-Clip function ON/OFF change in state of signal input.
L level (GND)	0.2 (Maximum)	0	Change is possible.
H level (AVDD potential)	0	3*Rex*Cex	Change is prohibited.

Start up wait time: It means time until the signal input is permitted from Non-Clip function ON.

●Protection Function

YDA144 has the following protection functions for the digital amplifier: Over-current Protection function, Thermal Protection function, and Low voltage Malfunction Prevention function.

Over-current Protection function

This is the function to establish the over-current protection mode when detecting a short circuit between YDA144 differential output pin and VSS, VDD, or another differential output. The function works independently for Lch and Rch. In the over current protection mode, the differential output pin becomes a high impedance state.
Setting /SDR pin to a logic Low state can cancel the Rch over current protection mode. Likewise, when setting /SDL pin to a logic Low level, the over current protection mode applied to Lch can be cancelled. In addition, turning on the power again can cancel the over current protection mode applied to Lch and Rch.

Thermal Protection function

This is the function to establish the thermal protection mode when detecting excessive high temperature of YDA144 itself. In the thermal protection mode, the differential output pin becomes Weak Low state (a state grounded through high resistivity). And, when YDA144 gets out of such condition, the protection mode is cancelled.

Low voltage Malfunction Prevention function

This is the function to establish the low voltage protection mode when AVDD pin voltage becomes lower than the detection voltage (V_{UVLL}) for the low voltage malfunction prevention and to cancel the protection mode when AVDD pin voltage becomes higher than the threshold voltage (V_{UVLH}) for its deactivation. In the low voltage protection mode, the differential output pin becomes Weak Low state (a state grounded through high resistivity). YDA144 will start up within the start-up time (T_{STUP}) when the low voltage protection mode is cancelled.

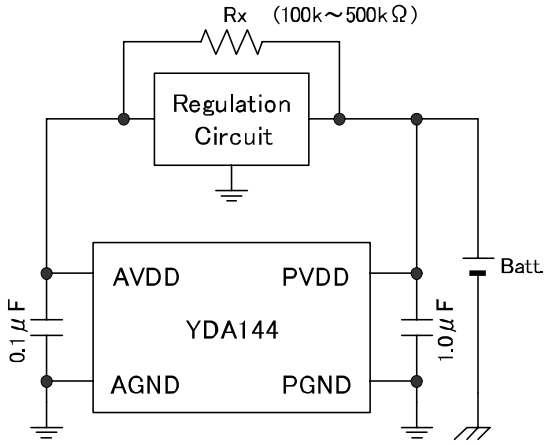
●Power-down Function

This is the function to turn Rch into the power-down mode when setting /SDR terminal to a logic Low level and to turn Lch into the power-down mode when setting /SDL terminal to a logic Low level. The power-down mode stops all the functions and minimizes current consumption. At this time, the differential output signal becomes Weak Low state (a state grounded through high resistivity).
YDA144 will start up within the start-up time (Tstup) when setting /SDR and /SDL terminals to a logic High state.

Caution:

When using a device while Non-Clip function is ON, power down state of both channels is released and used.
Please do not adjust the AVDD power supply voltage to less than 2V, when set to power down with the voltage impressed to the PVDD power supply terminal.

- Power up the PVDD supply voltage in conjunction with the AVDD regulation circuit when AVDD is generated by regulating PVDD.
- AVDD voltage should be within the range of 2V≦AVDD≦PVDD as shown in the following figure when the AVDD regulation circuit needs to be stopped by power supply management.



＜Example of measures for AVDD regulation circuit stop option＞

Notes in example of the above-mentioned measures

- When a voltage is supplied to PVDD pin, decide a value of Rx so that the voltage at AVDD pin becomes a value within the range of 2V≦AVDD≦PVDD.
  A value of Rx is about 100kΩ to 500kΩ, because the power-down leakage current (AVDD current) of YDA144 is 0.1μA typ. (2μA max.@125°C).
  And, when an LSI other than YDA144 is connected to the same regulator, decide a value of Rx in consideration of all leakage currents.
- The regulator output may increase up to the supply voltage level (=PVDD voltage) such as a battery when load current is zero. Please carefully check if any problem such as LSI's withstand voltage would occur when an LSI other than YDA144 is connected to the same regulator.
- This measure is effective only when a regulator whose output during a stop state becomes the high impedance state is used.

●Pop noise reduction function

The Pop Noise Reduction Function works in the cases of Power-on, Power-off, Power-down on, and Power-down off.
And, the pop-noise can be suppressed according to control the power down by the following procedure.

- /SDR and /SDL terminal are assumed to be H, after power-on.
- /SDR and /SDL terminal are assumed to be L, before Power-off.

●Snubber Circuit and schottky barrier diode

It is necessary to connect the snubber circuit and schottky barrier diode with the output terminal to prevent IC destruction by the output short-circuit when using it on the following conditions. The constant and the circuit are as follows.

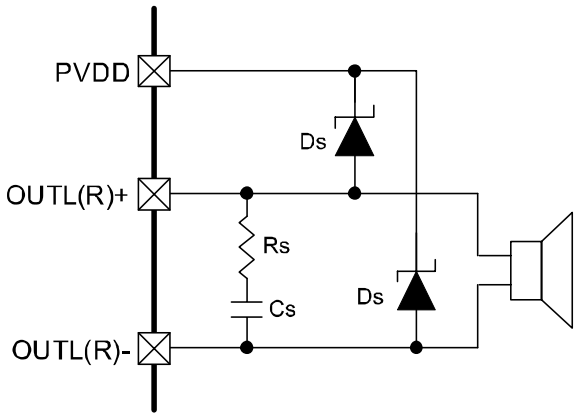
Power supply voltage range	Load conditions	Snubber Circuit	Schottky barrier diode
2.7V≦PVDD≦4.5V	R_L=8Ω Wiring inductance＞4μH	Between OUT*+ and OUT*- Rs=1.5Ω, Cs=330pF	Need less
4.5V＜PVDD≦5.25V	R_L=4Ω or 8Ω	Between OUT*+ and OUT*- Rs=1.5Ω, Cs=680pF	Between OUT** and PVDD

Recommended parts

Schottky barrier diode: ROHM, RB161VA-20

Forward current surge peak = 5A or more, Average forward current = 1A or more,

Forward voltage (I_F=1A) = 0.38V or less

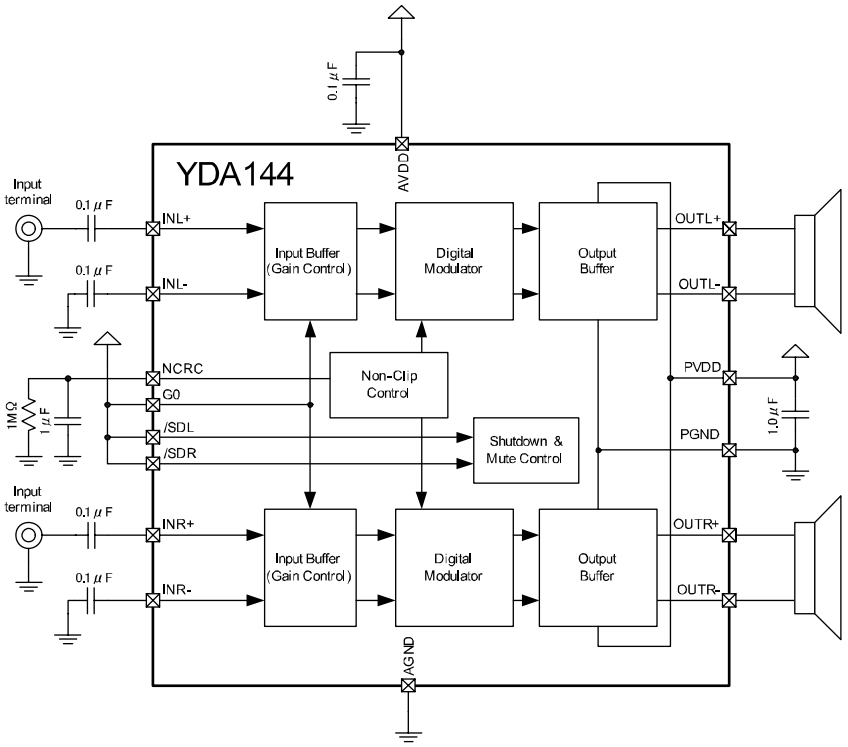


＜Snubber circuit and Schottky barrier diode＞

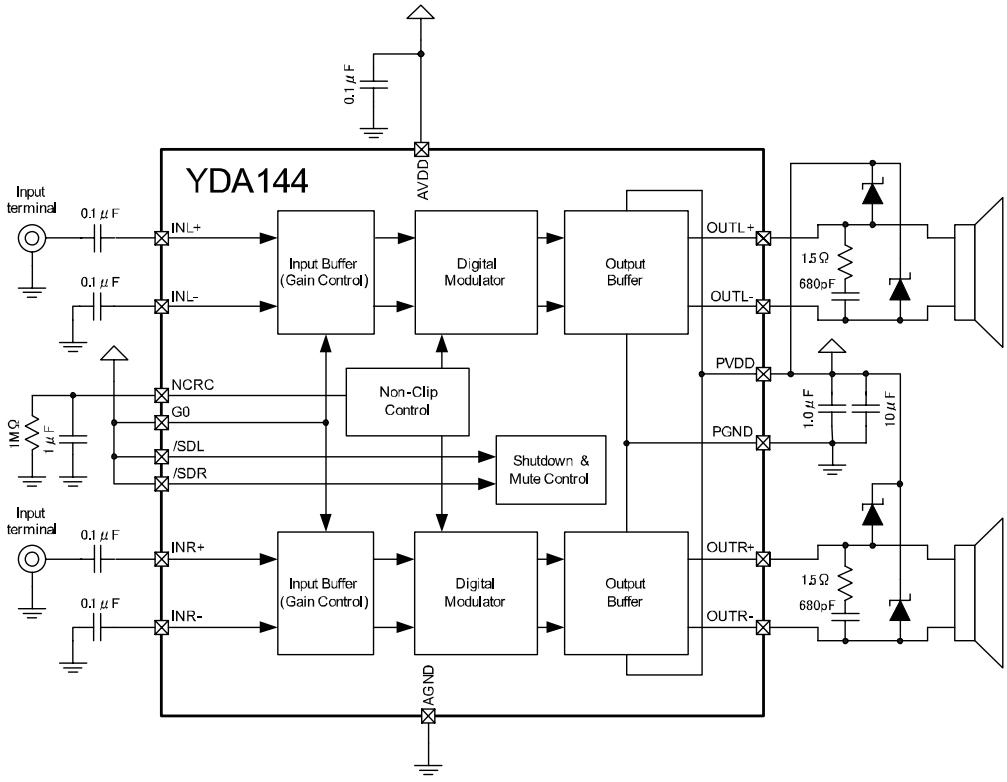
■Application circuit examples

●WLCSP16

・Snubber circuit and schottky barrier diode are unnecessary (2.7V≦PVDD≦4.5V)



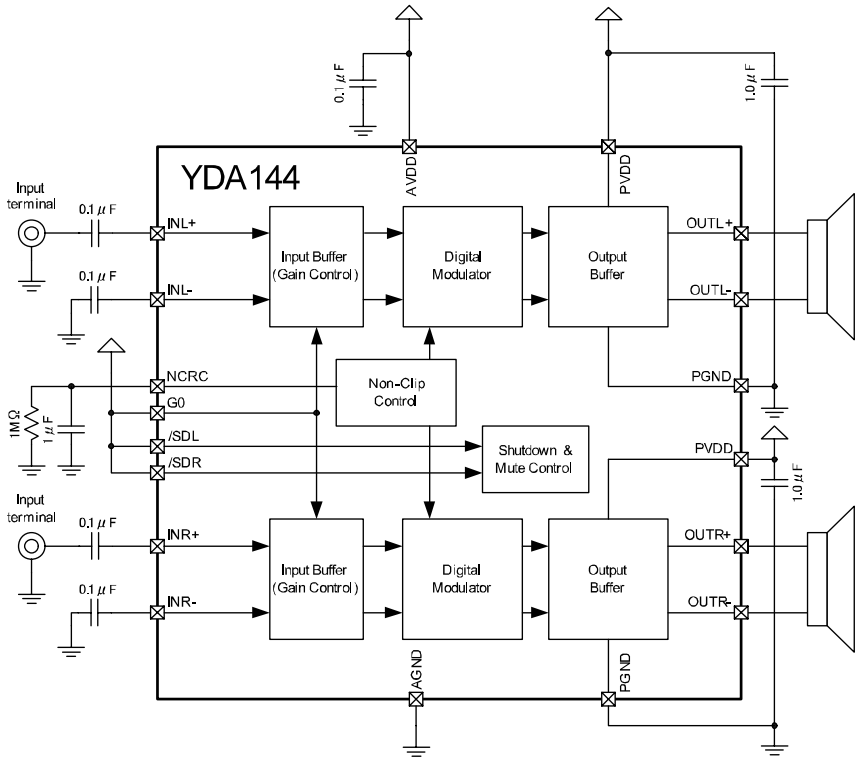
・Snubber circuit and schottky barrier diode are necessary (4.5V＜PVDD)



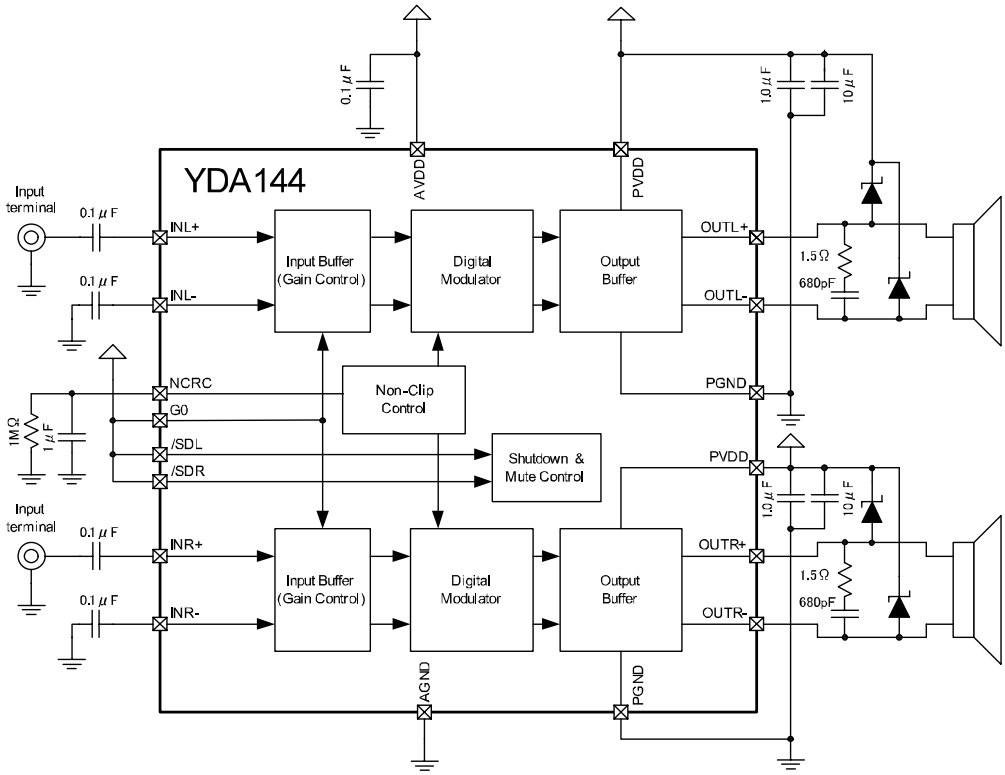
When the IC is used at more than 4.5V power supply, use it with an additional capacitor of 10μF or over between PVDD and GND. Place a bypass capacitor as close as possible to each power supply pin of the IC.

●QFN20

・Snubber circuit and schottky barrier diode are unnecessary (2.7V≦PVDD≦4.5V)



・Snubber circuit and schottky barrier diode are necessary (4.5V＜PVDD)



When the IC is used at more than 4.5V power supply, use it with an additional capacitor of 10μF or over between PVDD and GND. Place a bypass capacitor as close as possible to each power supply pin of the IC.

■Cautions for Safety

Please observe the following restrictions to use YDA144 safely.

・The snubber circuit should be laid out within 3mm from the IC on the component side.

・The schottky barrier diode should be laid out within 3mm from the IC.

・Place a bypass capacitor, which is connected between PVDD and GND, together with a schottky barrier diode. And, when no schottky barrier diode is required, place it within 3mm from the IC.

・When a LC filter is used, consider the following.

With a system of which an input signal in excess of a resonance frequency of a LC filter could be input, be sure to place a snubber circuit (insert 13Ω+330ns at the LC filter output) after the LC filter to prevent an over-current condition. The purpose is to prevent an over-current from flowing because an impedance of the speaker increases at the resonance frequency.

・With a system of which a voltage at an input pin might exceed a supply voltage of V_{DDA}/GND, use an external diode etc. to assure that the voltage does not exceed the absolute maximum rating.

■Electrical Characteristic

●Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Power supply terminal (PVDD) Voltage Range	V_{DDP}	−0.3	6.0	V
Power supply terminal (AVDD) Voltage Range	V_{DDP}	−0.3	6.0	V
Input terminal Voltage Range (Analog input terminals: INL+,INL-,INR+,INR-)	V_{IN}	V_{SS}−0.6	V_{DDA}+0.6	V
Input terminal Voltage Range (Input terminals except the above-mentioned)	V_{IN}	V_{SS}−0.3	V_{DDA}+0.3	V
Allowable dissipation (16WLCSP,Ta=25℃)	P_{D25}		2.0	W
Allowable dissipation (16WLCSP,Ta=85℃)	P_{D85}		0.80	W
Allowable dissipation (20QFN,Ta=25℃)	P_{D25}		1.56	W
Allowable dissipation (20QFN,Ta=85℃)	P_{D85}		0.62	W
Allowable dissipation (20QFN,Ta=25℃)	P_{D25}		3.63	W
Allowable dissipation (20QFN,Ta=85℃)	P_{D85}		1.45	W
Junction Temperature	T_{JMAX}		125	℃
Storage Temperature	T_{STG}	−50	125	℃

Note) Absolute Maximum Ratings is values which must not be exceeded to guarantee device reliability and life, and when using a device in excess even a moment, it may immediately cause damage to device or may significantly deteriorate its reliability With a system of which a voltage at an input pin might exceed a supply voltage of V_{DDA}/GND, use an external diode to assure that the voltage does not exceed the absolute maximum rating.
*1: θja=50.0℃/W, conditions: YDA144 evaluation board (4 layers), dead calm
*2: θja=64.0℃/W, conditions: YDA144 evaluation board (2 layers, without through-hole), dead calm
*3: θja=27.5℃/W, conditions: 4 layers, through-hole, copper foil 65μm, dead calm

●Recommended Operating Condition

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage(PVDD)	V_{DDP}	2.7	3.6	5.25	V
Power Supply Voltage(AVDD)	V_{DDA}	2.7	3.6	5.25	V
Operating Ambient Temperature	T_a	−40	25	85	℃
Speaker Impedance (4.5V ＜ PVDD)	R_L	4			Ω
Speaker Impedance (2.7V ≦ PVDD ≦ 4.5V)	R_L	8			Ω

Note) Do not use under a condition other than the recommended operating conditions.
PVDD ≧ AVDD (contain power supply start up) must be met.
The rising time of PVDD and AVDD should be more than 1μs.

●DC Characteristics (V_{SS}=0V, V_{DDP}= V_{DDA} =2.7V to 5.25V, Ta=−40ºC to 85ºC, unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
AVDD power supply start-up threshold voltage	V_{UVLH}			2.2		V
AVDD power supply shut-down threshold voltage	V_{UVLL}			2.0		V
/SDL, /SDR, G0 terminal H level input voltage	V_{IH}		1.35			V
/SDL, /SDR, G0 terminal L level input voltage	V_{IL}				0.35	V
AVDD consumption current	I_{DD}	V_{DDA}=3.6V, no load		6.0		mA
PVDD consumption current	I_{DD}	V_{DDP}=3.6V, no load, no signal input		2.0		mA
Consumption current in power-down mode AVDD + PVDD	I_{PD}	/SDL=/SDR=V_{ss}, Ta=25℃		0.1		μA

●AC characteristics (V_{SS}=0V, V_{DDP}= V_{DDA} =2.7V to 5.25V, Ta=−40ºC to 85ºC, unless otherwise specified)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Start-up time	T_{STUP}			3.5		ms
Input cut-off frequency	fc	C_{IN} =0.1μF, Av=18dB		57		Hz
Attack time	T_{AT}	V_{DDA}=3.6V, g=10dB, Cex=1μF, Rex=1MΩ		10		ms
Release time	T_{RL}	V_{DDA}=3.6V, g=10dB, Cex=1μF, Rex=1MΩ		0.8		s
Carrier clock frequency	f_{PWM}			1.0		MHz

●Analog Characteristics

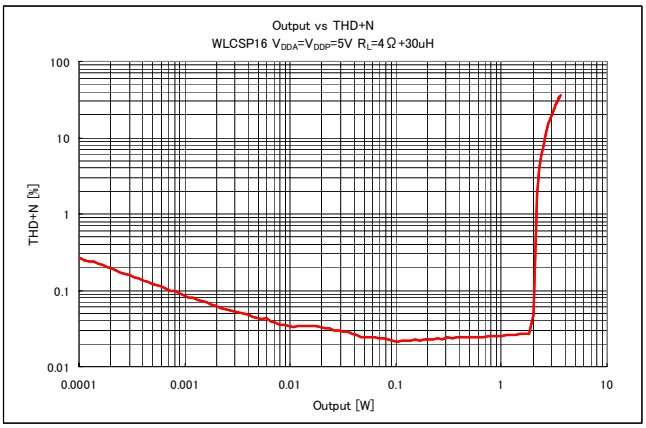
(V_{SS}=0V, V_{DDP}= V_{DDA} =3.6V, R_L=8Ω, Ta=25ºC, Non-Clip function=OFF, no snubber circuit, no schottky barrier diode, unless otherwise specified)

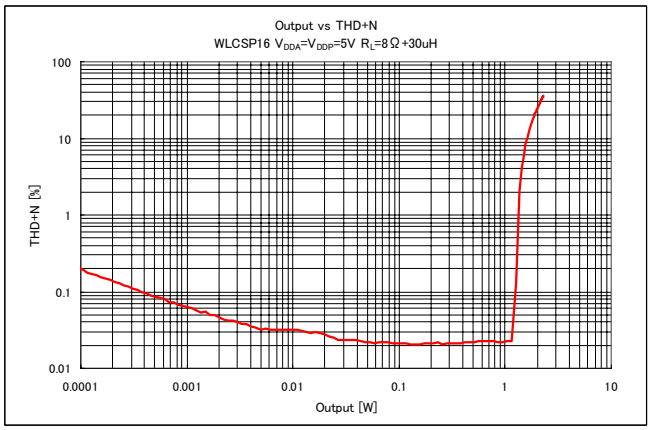
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum output	P_O	R_L=4Ω, f=1kHz,THD+N=10%, V_{DDP}=V_{DDA}=5V		2.1		W
		R_L=8Ω, f=1kHz,THD+N=10%		0.75		W
Voltage Gain	A_V	G0=L		12		dB
		G0=H		18		dB
Total Harmonic Distortion Rate (BW:20kHz)	THD+N	R_L=8Ω, P_o=0.4W, f=1kHz		0.03		%
Residual Noise (A-Filter)	N	Av=12dB		40		μVrms
Signal /Noise Ratio (BW:20kHz A-Filter)	SNR	Av=12dB		95		dB
Channel Separation Ratio	CS	1kHz		95		dB
Power supply rejection ratio	PSRR	217Hz (to PVDD)		−85		dB
Maximum Efficiency	η	R_L=8Ω, P_o=600mW		84		%
		R_L=8Ω, P_o=100mW		78		%
Output offset voltage	Vo			±20		mV
Frequency characteristics	f_{RES}	C_{IN} =0.1μF, f=100Hz to 20kHz	−3	-	1	dB
Non-Clip maximum attenuation gain	Aa			−10		dB

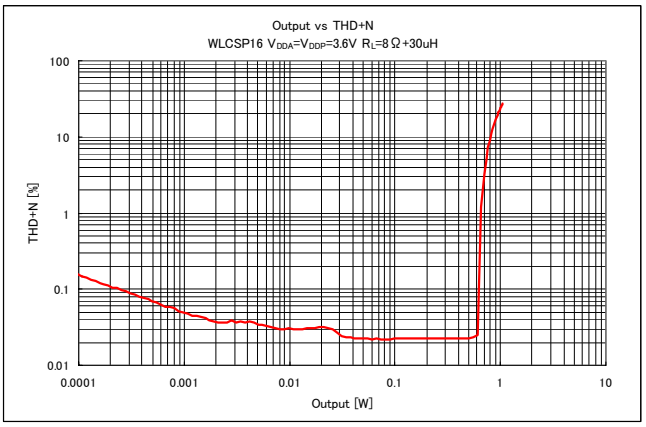
Note) All the values of analog characteristics were obtained by using our evaluation circumstance.
Depending upon parts and pattern layout to use, characteristics may be changed.
8Ω or 4Ω resistor and 30μH coil are used as an output load in order to obtain various digital amplifier characteristics.

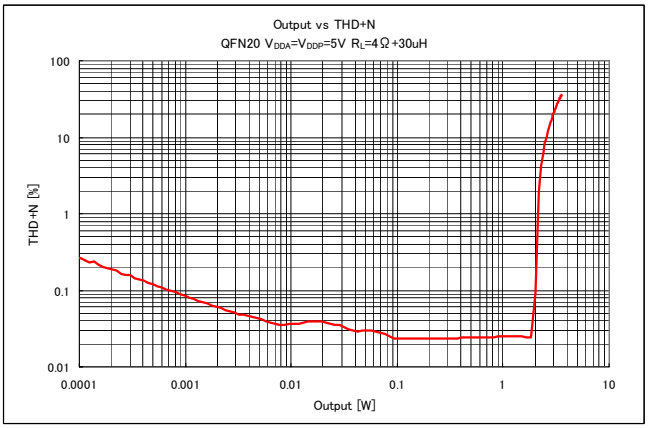
●Typical characteristics examples

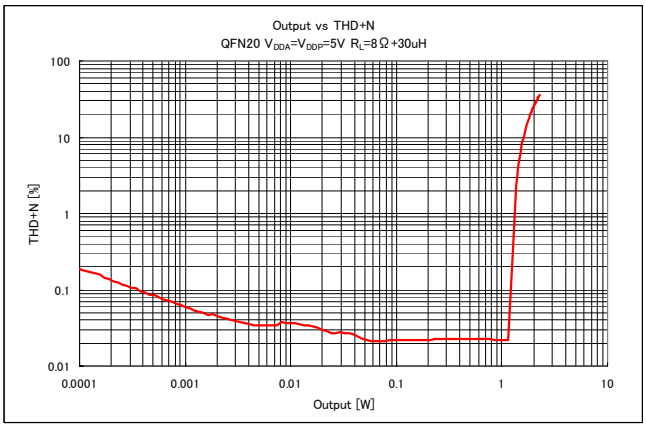
V_{DDA}=V_{DDP}=5V: Gain=18dB, Snubber circuit and schottky barrier diode are added.
V_{DDA}=V_{DDP}=3.6V: Gain=12dB, no Snubber circuit, no schottky barrier diode.
(VSS=0V, Ta=25ºC, Non-Clip=OFF, unless otherwise specified)

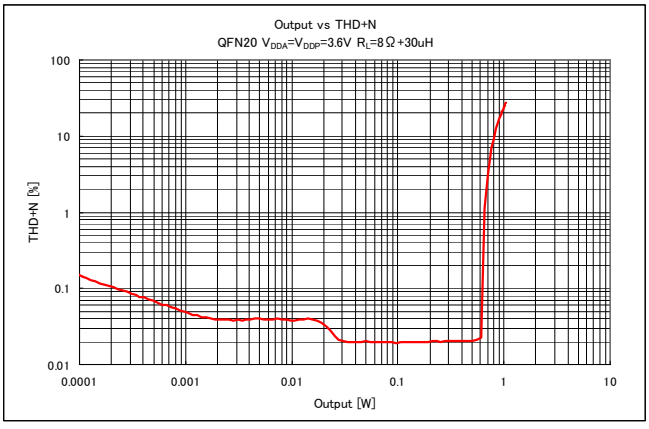


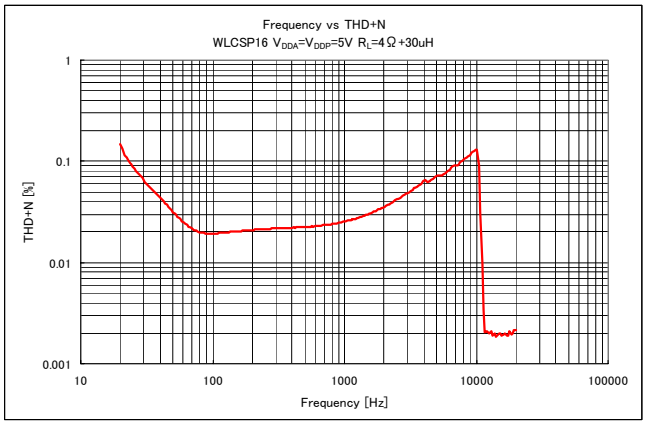


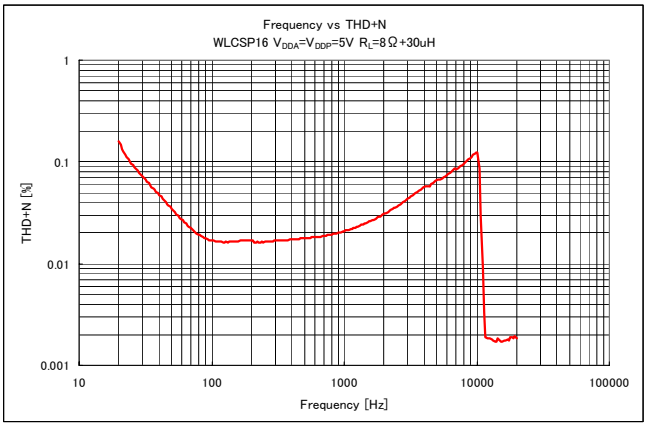


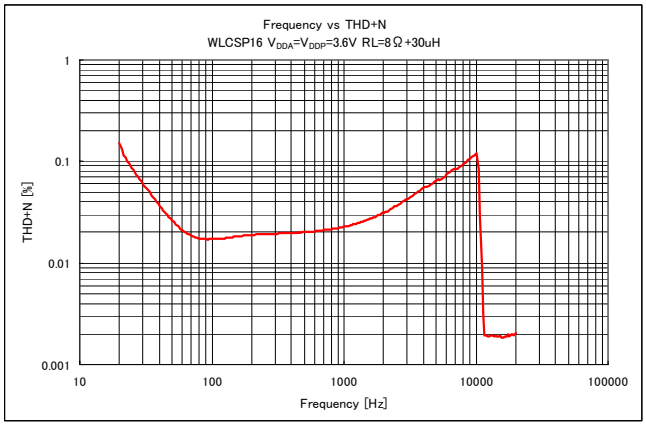


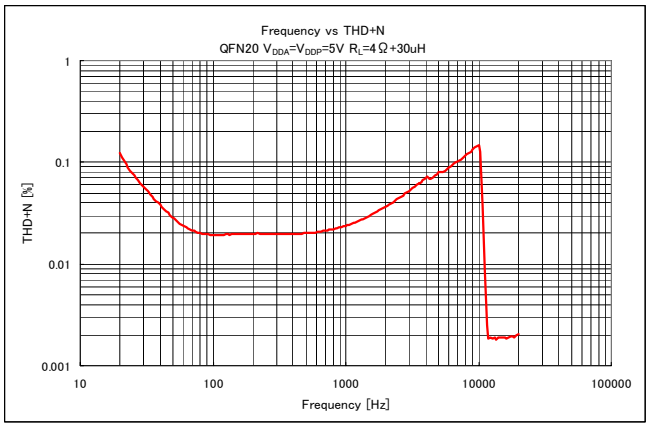


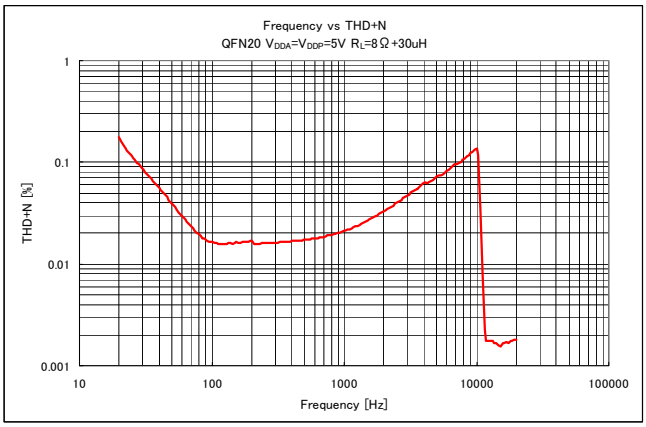


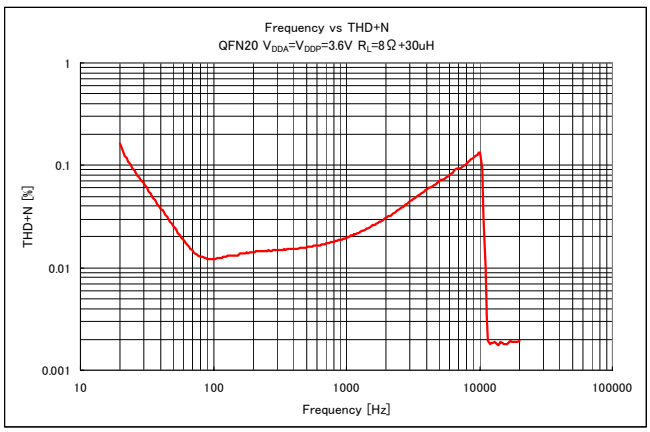

Frequency vs THD+N
WLCSP16 V_{DDA}=V_{DDP}=5V R_L=4Ω+30uH
THD+N [%]
1
0.1
0.01
0.001
10
100
1000
10000
100000
Frequency [Hz]

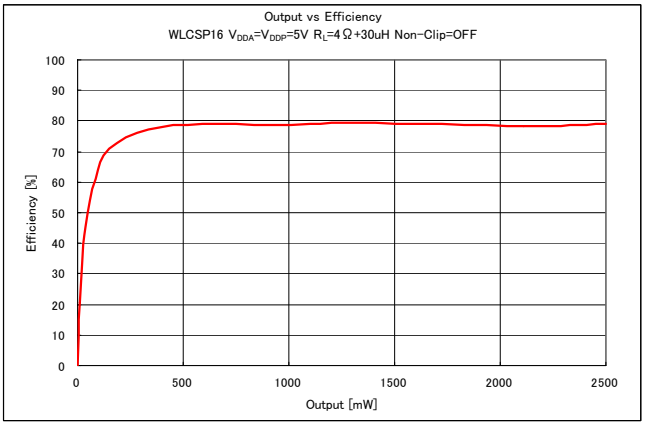

Frequency vs THD+N
WLCSP16 V_{DDA}=V_{DDP}=5V R_L=8Ω+30uH
THD+N [%]
1
0.1
0.01
0.001
10
100
1000
10000
100000
Frequency [Hz]

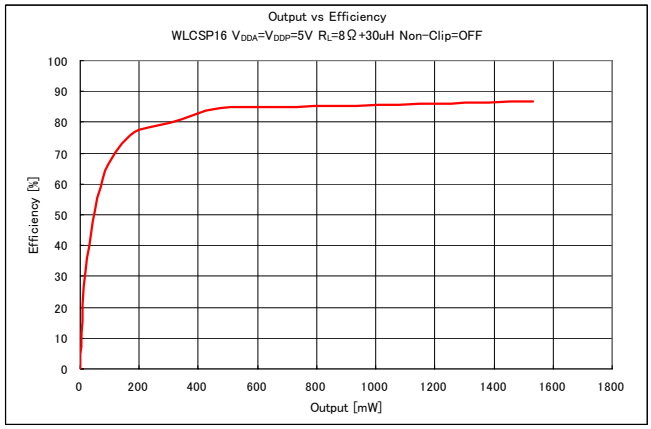

Frequency vs THD+N
WLCSP16 V_{DDA}=V_{DDP}=3.6V RL=8Ω+30uH
THD+N [%]
1
0.1
0.01
0.001
10
100
1000
10000
100000
Frequency [Hz]

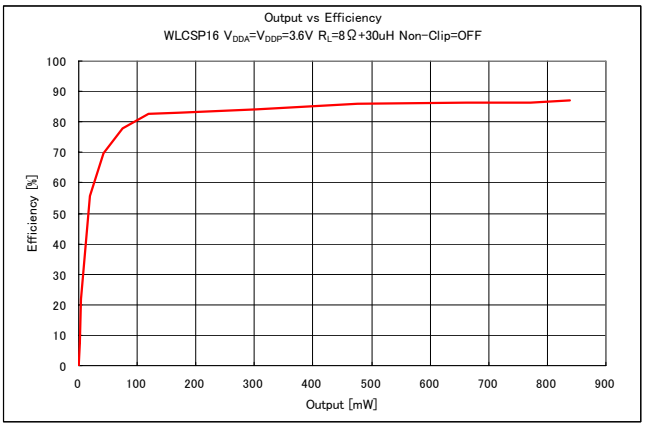

Frequency vs THD+N
QFN20 V_{DDA}=V_{DDP}=5V R_L=4Ω+30uH
THD+N [%]
1
0.1
0.01
0.001
10
100
1000
10000
100000
Frequency [Hz]

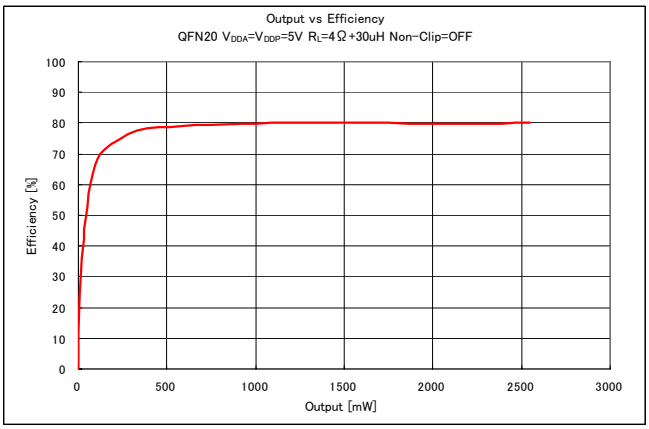

Frequency vs THD+N
QFN20 V_{DDA}=V_{DDP}=5V R_L=8Ω+30uH
THD+N [%]
1
0.1
0.01
0.001
10
100
1000
10000
100000
Frequency [Hz]

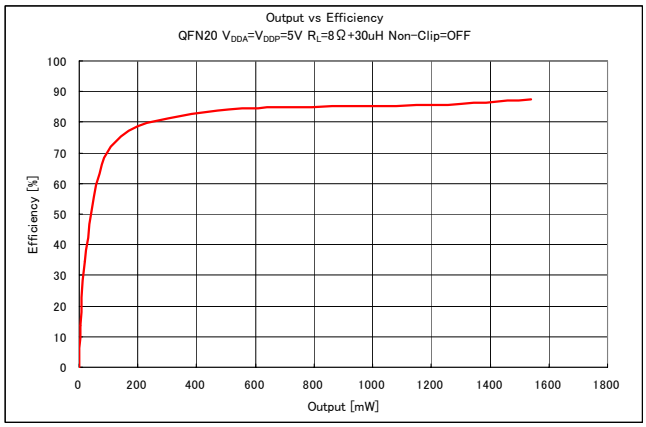

Frequency vs THD+N
QFN20 V_{DDA}=V_{DDP}=3.6V R_L=8Ω+30uH
THD+N [%]
1
0.1
0.01
0.001
10
100
1000
10000
100000
Frequency [Hz]

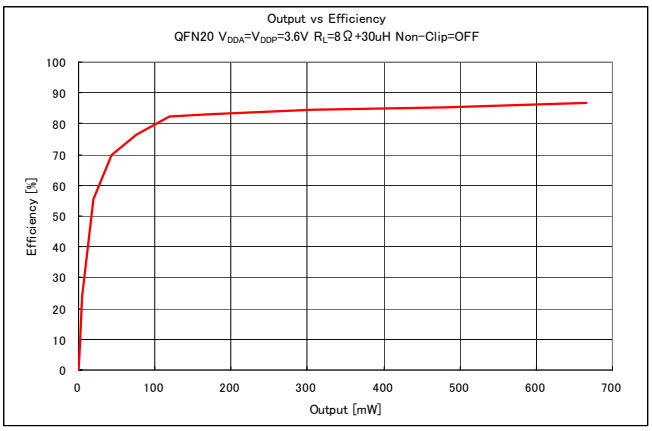

Output vs Efficiency
WLCSP16 V_{DDA}=V_{DDP}=5V R_L=4Ω+30uH Non-Clip=OFF
Efficiency [%]
Output [mW]

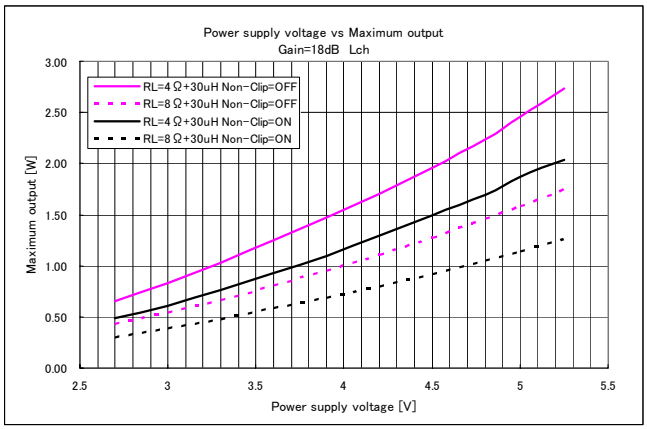

Output vs Efficiency
WLCSP16 V_{DDA}=V_{DDP}=5V R_L=8Ω+30uH Non-Clip=OFF
Efficiency [%]
Output [mW]

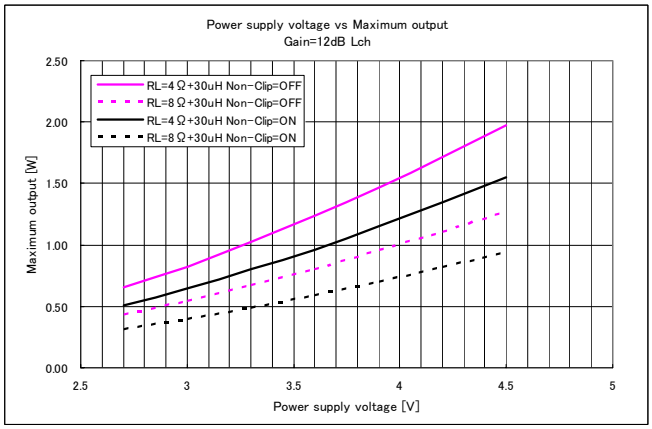

Output vs Efficiency
WLCSP16 V_{DDA}=V_{DDP}=3.6V R_L=8Ω+30uH Non-Clip=OFF
Efficiency [%]
Output [mW]

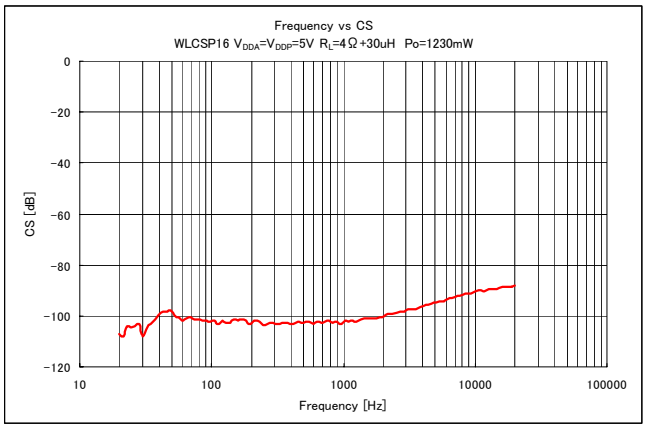

Output vs Efficiency
QFN20 V_{DDA}=V_{DDP}=5V R_L=4Ω+30uH Non-Clip=OFF
Efficiency [%]
Output [mW]

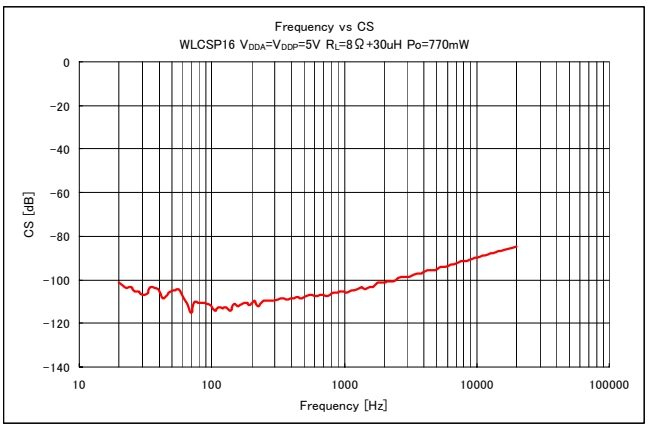

Output vs Efficiency
QFN20 V_{DDA}=V_{DDP}=5V R_L=8Ω+30uH Non-Clip=OFF
Efficiency [%]
Output [mW]

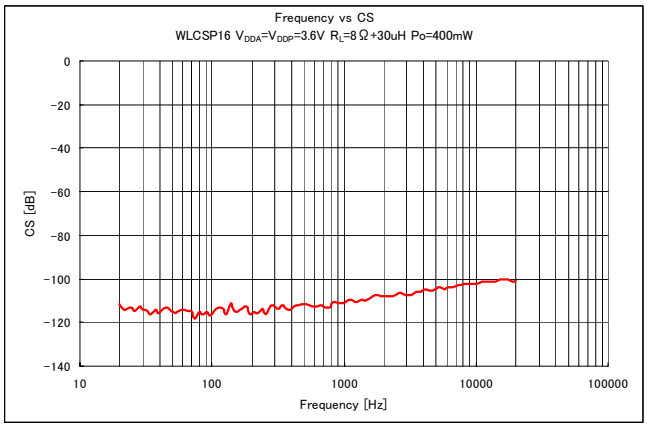

Output vs Efficiency
QFN20 V_{DDA}=V_{DDP}=3.6V R_L=8Ω+30uH Non-Clip=OFF
Efficiency [%]
Output [mW]

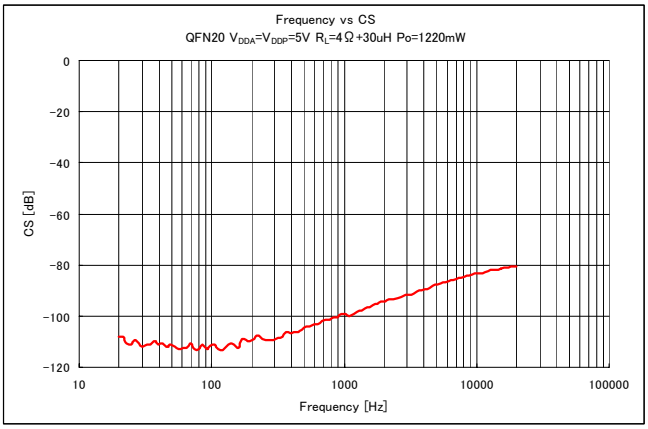

Power supply voltage vs Maximum output
Gain=18dB Lch
RL=4Ω+30uH Non-Clip=OFF
RL=8Ω+30uH Non-Clip=OFF
RL=4Ω+30uH Non-Clip=ON
RL=8Ω+30uH Non-Clip=ON
Maximum output [W]
Power supply voltage [V]

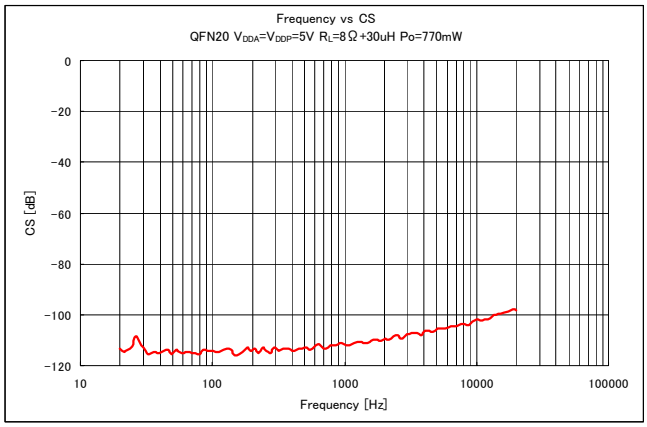

Power supply voltage vs Maximum output
Gain=12dB Lch
RL=4Ω+30uH Non-Clip=OFF
RL=8Ω+30uH Non-Clip=OFF
RL=4Ω+30uH Non-Clip=ON
RL=8Ω+30uH Non-Clip=ON
Maximum output [W]
Power supply voltage [V]

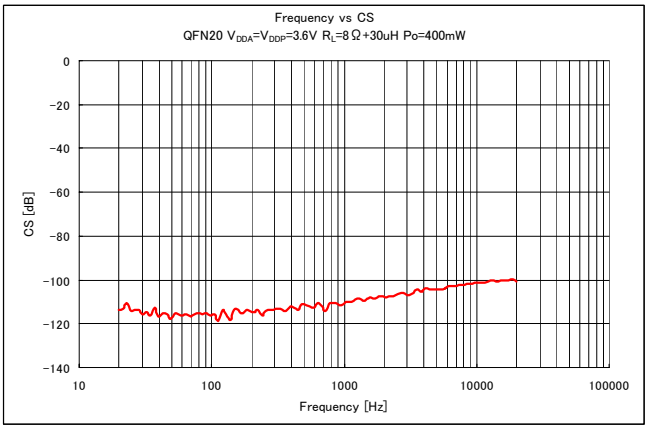

Frequency vs CS
WLCSP16 VDDA=VDDP=5V RL=4Ω+30uH Po=1230mW
CS [dB]
Frequency [Hz]

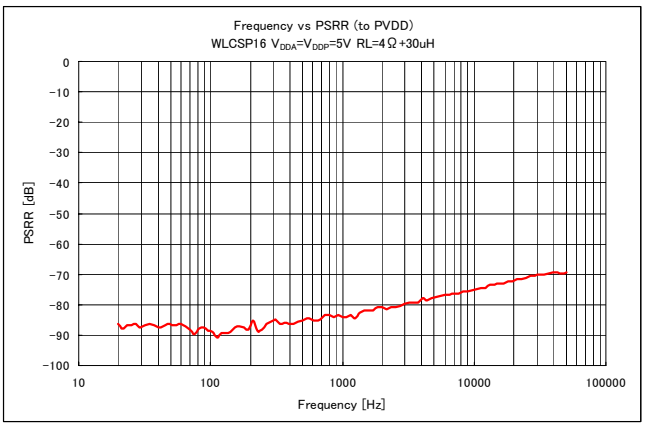

Frequency vs CS
WLCSP16 VDDA=VDDP=5V RL=8Ω+30uH Po=770mW
CS [dB]
Frequency [Hz]

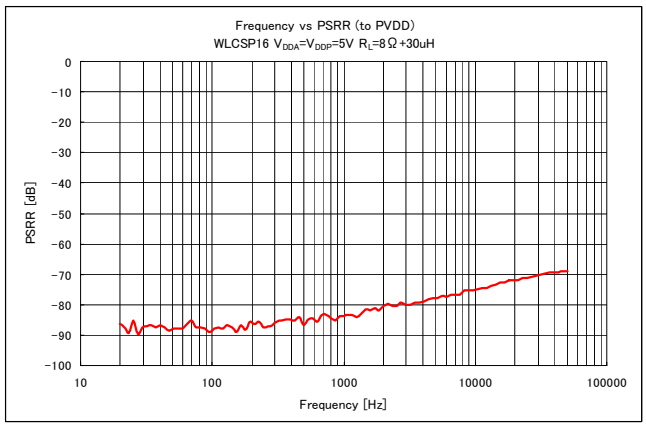

Frequency vs CS
WLCSP16 VDDA=VDDP=3.6V RL=8Ω+30uH Po=400mW
CS [dB]
Frequency [Hz]

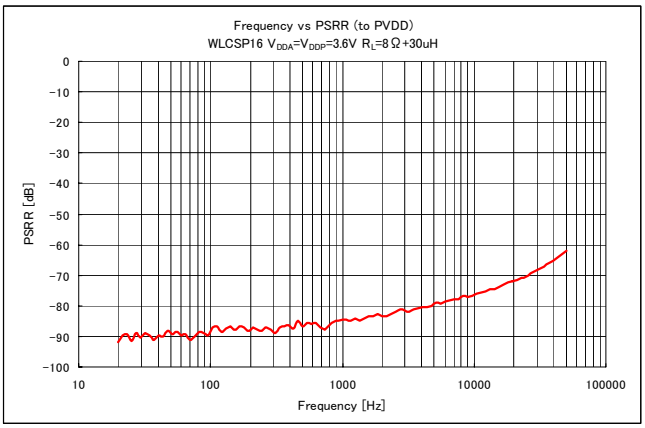

Frequency vs CS
QFN20 VDDA=VDDP=5V RL=4Ω+30uH Po=1220mW
CS [dB]
0
-20
-40
-60
-80
-100
-120
10
100
1000
10000
100000
Frequency [Hz]

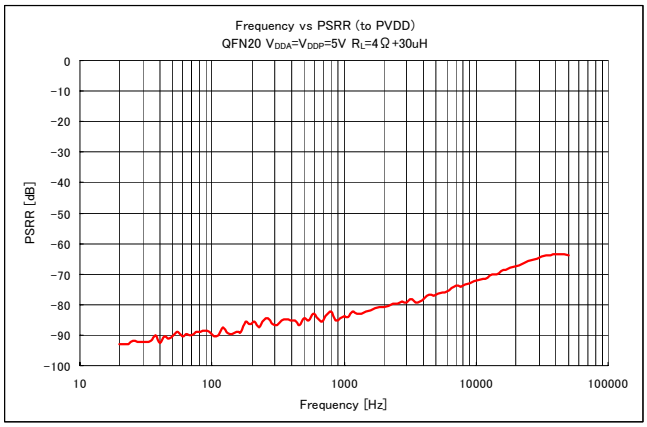

Frequency vs CS
QFN20 VDDA=VDDP=5V RL=8Ω+30uH Po=770mW
CS [dB]
0
-20
-40
-60
-80
-100
-120
10
100
1000
10000
100000
Frequency [Hz]

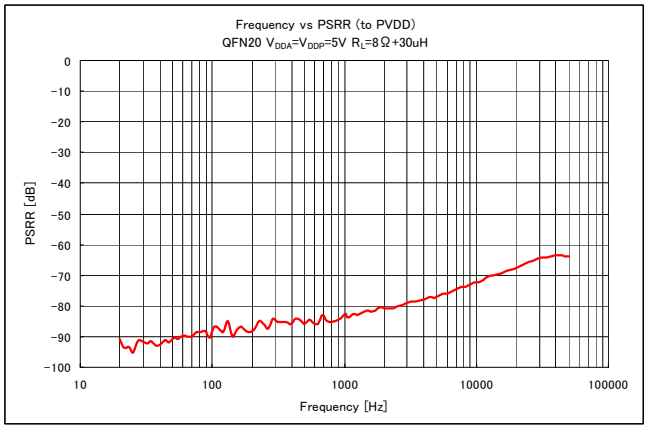

Frequency vs CS
QFN20 VDDA=VDDP=3.6V RL=8Ω+30uH Po=400mW
CS [dB]
0
-20
-40
-60
-80
-100
-120
-140
10
100
1000
10000
100000
Frequency [Hz]

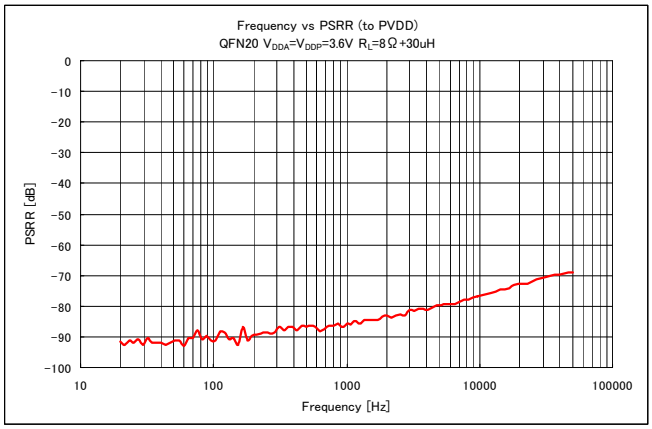

Frequency vs PSRR (to PVDD)
WLCSP16 VDDA=VDDP=5V RL=4Ω+30uH
PSRR [dB]
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
10
100
1000
10000
100000
Frequency [Hz]

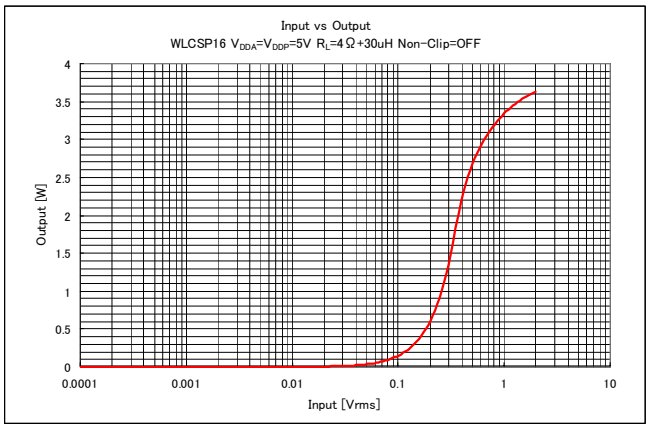

Frequency vs PSRR (to PVDD)
WLCSP16 VDDA=VDDP=5V RL=8Ω+30uH
PSRR [dB]
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
10
100
1000
10000
100000
Frequency [Hz]

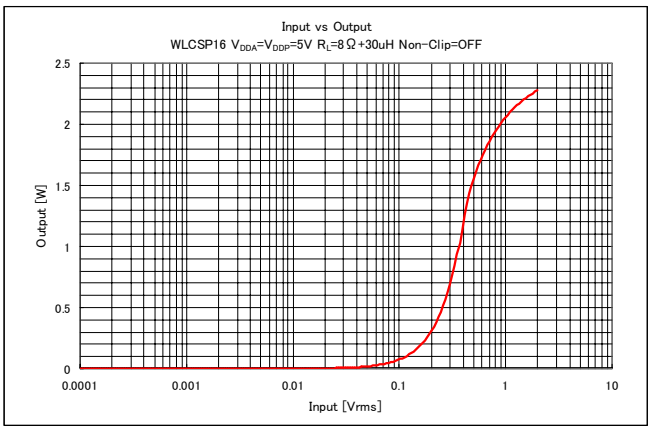

Frequency vs PSRR (to PVDD)
WLCSP16 VDDA=VDDP=3.6V RL=8Ω+30uH
PSRR [dB]
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
10
100
1000
10000
100000
Frequency [Hz]

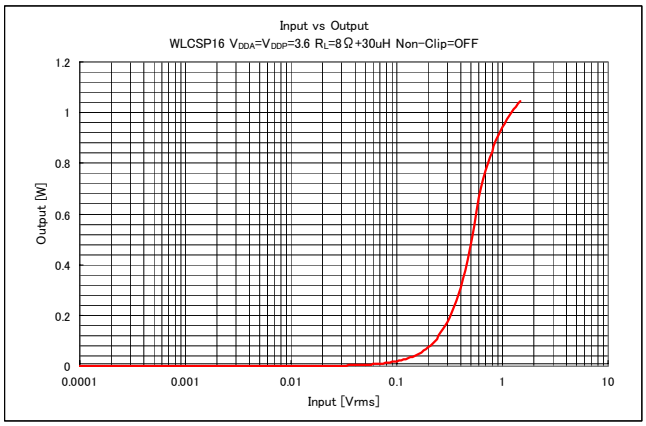

Frequency vs PSRR (to PVDD)
QFN20 V_{DDA}=V_{DDP}=5V R_L=4Ω+30uH
PSRR [dB]
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
10
100
1000
10000
100000
Frequency [Hz]

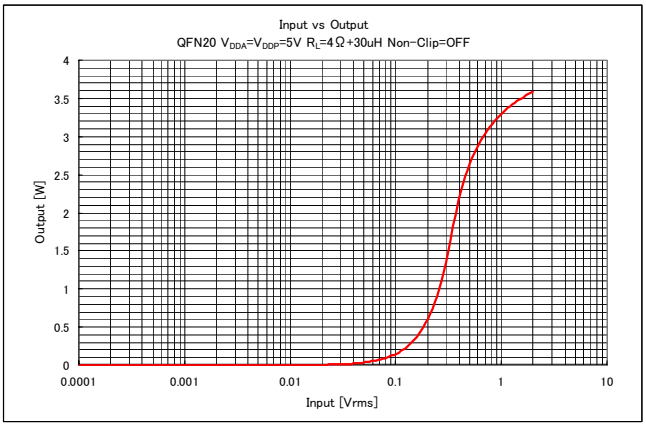

Frequency vs PSRR (to PVDD)
QFN20 V_{DDA}=V_{DDP}=5V R_L=8Ω+30uH
PSRR [dB]
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
10
100
1000
10000
100000
Frequency [Hz]

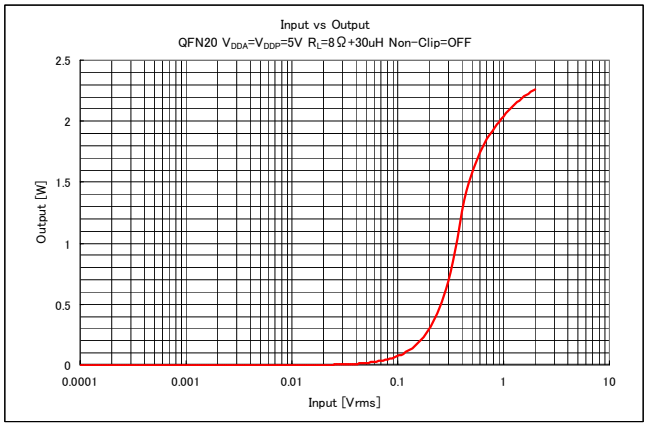

Frequency vs PSRR (to PVDD)
QFN20 V_{DDA}=V_{DDP}=3.6V R_L=8Ω+30uH
PSRR [dB]
0
−10
−20
−30
−40
−50
−60
−70
−80
−90
−100
10
100
1000
10000
100000
Frequency [Hz]

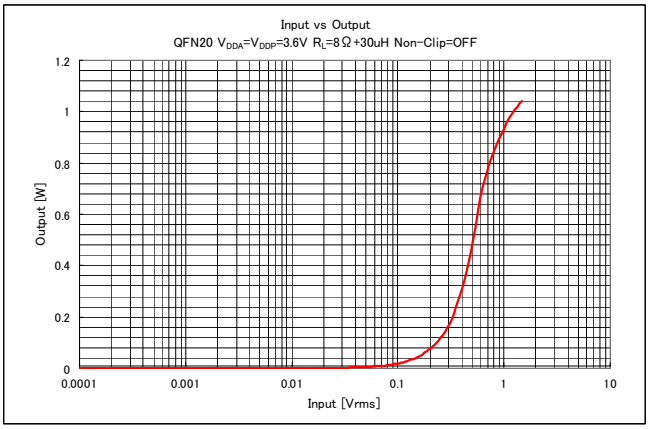

Input vs Output
WLCSP16 V_{DDA}=V_{DDP}=5V R_L=4Ω+30uH Non-Clip=OFF
Output [W]
4
3.5
3
2.5
2
1.5
1
0.5
0
0.0001
0.001
0.01
0.1
1
10
Input [Vrms]

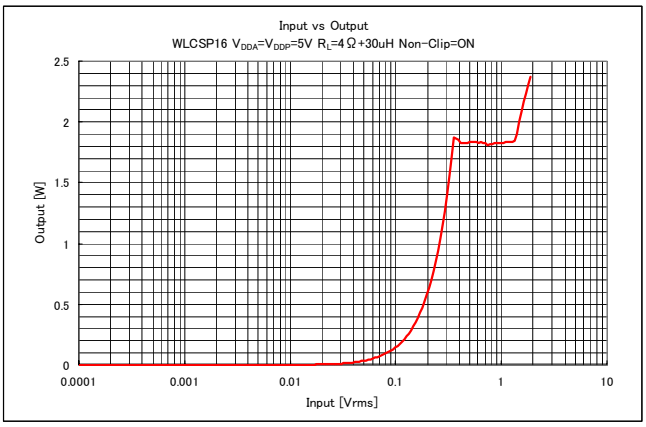

Input vs Output
WLCSP16 V_{DDA}=V_{DDP}=5V R_L=8Ω+30uH Non-Clip=OFF
Output [W]
2.5
2
1.5
1
0.5
0
0.0001
0.001
0.01
0.1
1
10
Input [Vrms]

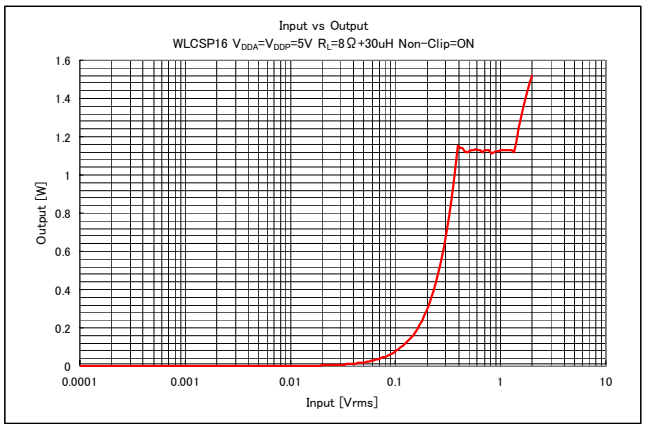

Input vs Output
WLCSP16 V_{DDA}=V_{DDP}=3.6 R_L=8Ω+30uH Non-Clip=OFF
Output [W]
1.2
1
0.8
0.6
0.4
0.2
0
0.0001
0.001
0.01
0.1
1
10
Input [Vrms]

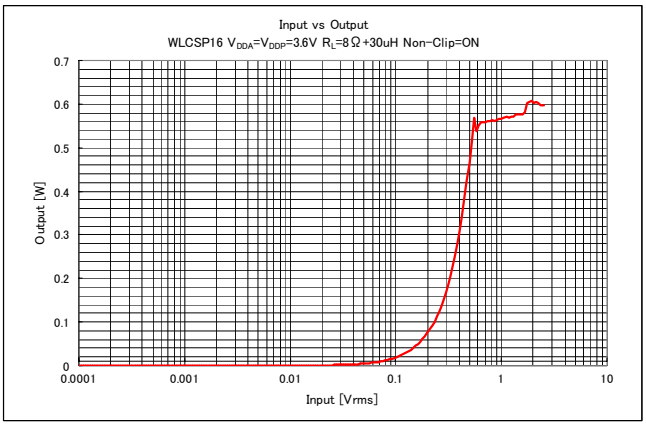

Input vs Output
QFN20 V_{DDA}=V_{DDP}=5V R_L=4Ω+30uH Non-Clip=OFF
Output [W]
Input [Vrms]
0
0.5
1
1.5
2
2.5
3
3.5
4
0.0001
0.001
0.01
0.1
1
10

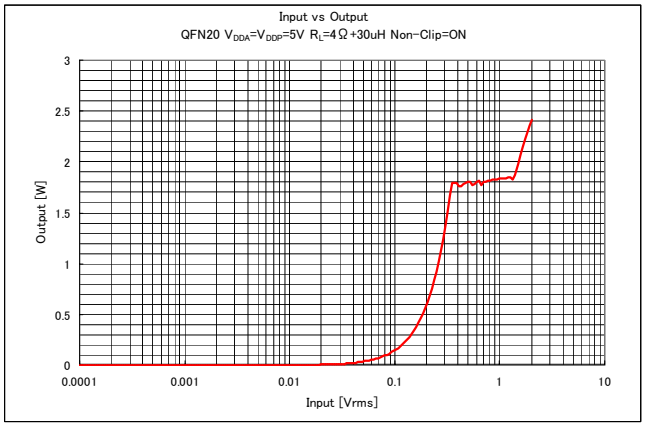

Input vs Output
QFN20 V_{DDA}=V_{DDP}=5V R_L=8Ω+30uH Non-Clip=OFF
Output [W]
Input [Vrms]
0
0.5
1
1.5
2
2.5
0.0001
0.001
0.01
0.1
1
10

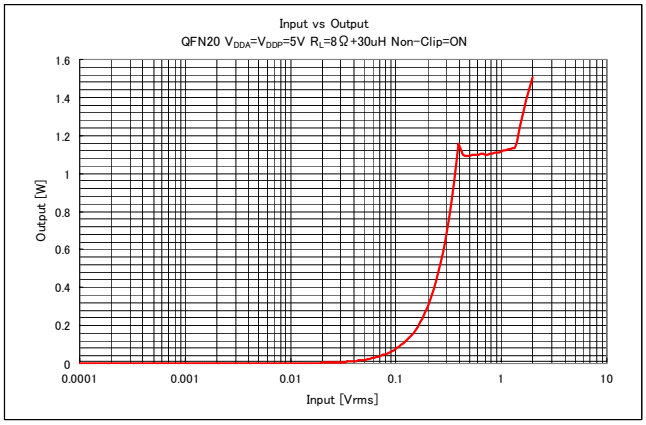

Input vs Output
QFN20 V_{DDA}=V_{DDP}=3.6V R_L=8Ω+30uH Non-Clip=OFF
Output [W]
Input [Vrms]
0
0.2
0.4
0.6
0.8
1
1.2
0.0001
0.001
0.01
0.1
1
10

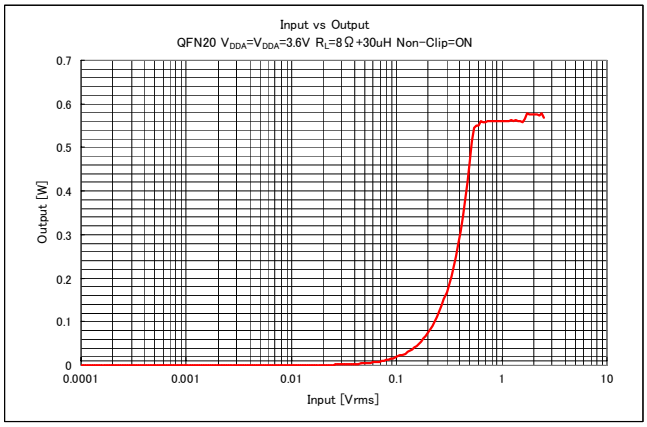

Input vs Output
WLCSP16 V_{DDA}=V_{DDP}=5V R_L=4Ω+30uH Non-Clip=ON
Output [W]
Input [Vrms]
0
0.5
1
1.5
2
2.5
0.0001
0.001
0.01
0.1
1
10


Input vs Output
WLCSP16 V_{DDA}=V_{DDP}=5V R_L=8Ω+30uH Non-Clip=ON
Output [W]
Input [Vrms]
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
0.0001
0.001
0.01
0.1
1
10


Input vs Output
WLCSP16 V_{DDA}=V_{DDP}=3.6V R_L=8Ω+30uH Non-Clip=ON
Output [W]
Input [Vrms]
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.0001
0.001
0.01
0.1
1
10

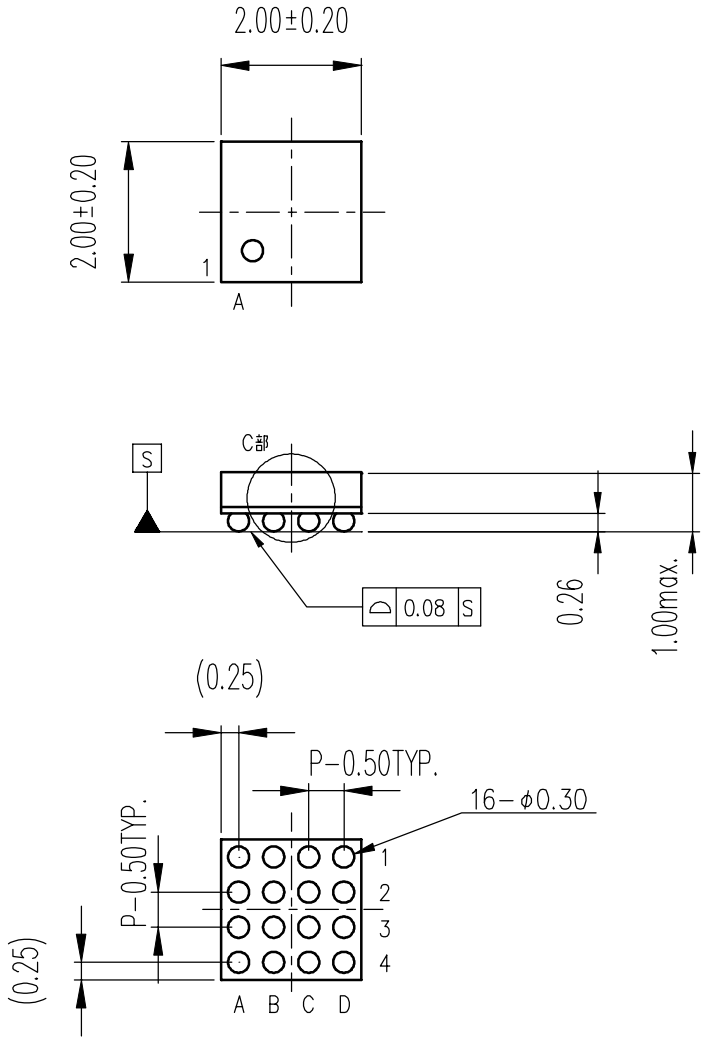

Input vs Output
QFN20 V_{DDA}=V_{DDP}=5V R_L=4Ω+30uH Non-Clip=ON
Output [W]
Input [Vrms]
3
2.5
2
1.5
1
0.5
0
0.0001
0.001
0.01
0.1
1
10


Input vs Output
QFN20 V_{DDA}=V_{DDP}=5V R_L=8Ω+30uH Non-Clip=ON
Output [W]
Input [Vrms]
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0.0001
0.001
0.01
0.1
1
10


Input vs Output
QFN20 V_{DDA}=V_{DDA}=3.6V R_L=8Ω+30uH Non-Clip=ON
Output [W]
Input [Vrms]
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0.0001
0.001
0.01
0.1
1
10

■Package Outline

C-PK16WP-1



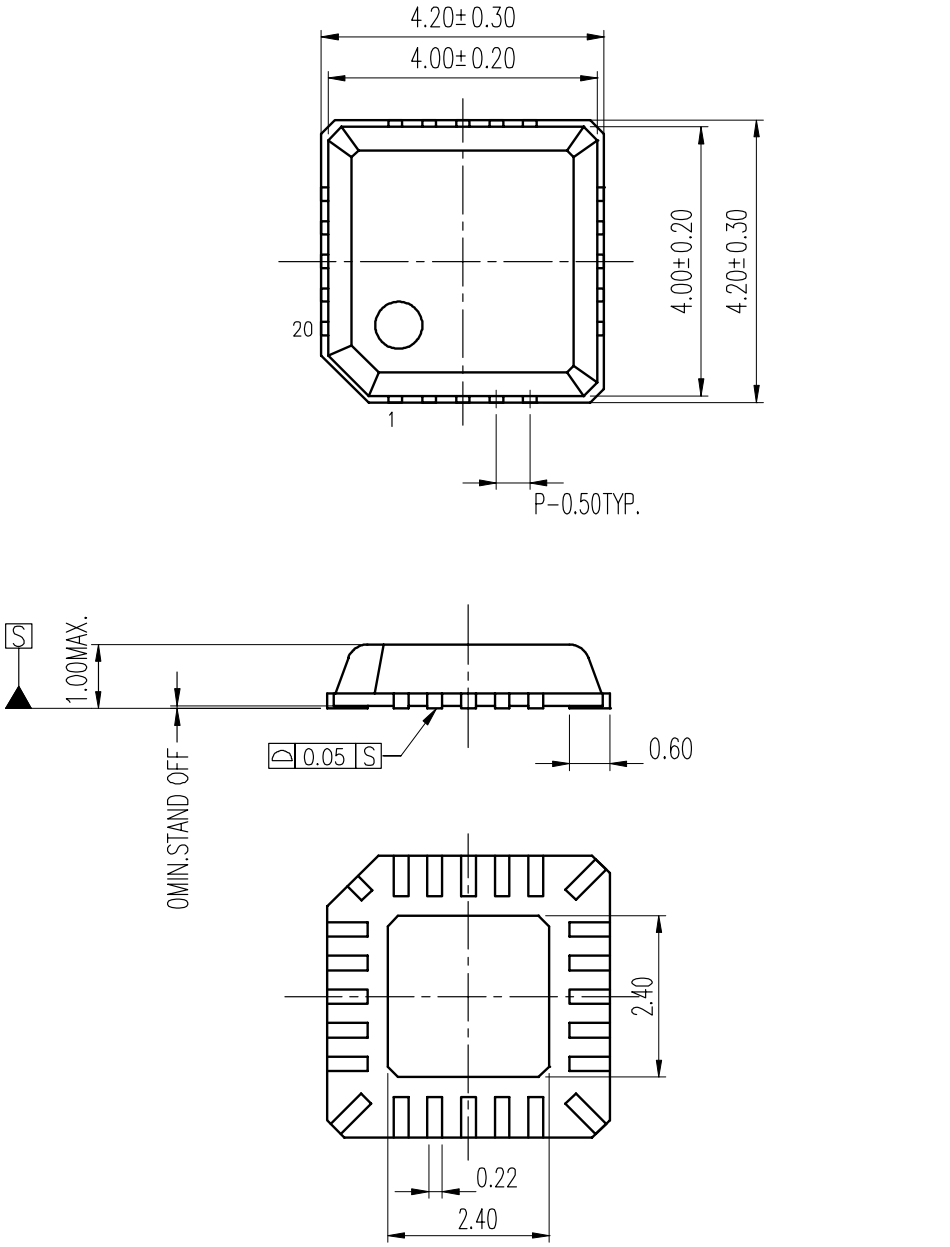
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みます。
単位： mm

The figure in the parentheses ( ) should be used as a reference.
The dimensions include burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

C-PK20QP-5



端子厚さ/Lead Thickness：0.22

カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
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