21555 Non-Transparent PCI-to-PCI Bridge

Revolutionary Bridge Technology for Intelligent I/O and Embedded Applications

developer.intel.com

Product Highlights

- Non-Transparent PCI-to-PCI bridge technology for high-performance embedded and intelligent I/O applications
- Independent address spaces and asynchronous clocks deliver unparalleled application flexibility
- 64-bit primary and secondary bus interfaces deliver high performance for data-intensive applications
- Compliant with ACPI and PCI bus power management specifications
- Secondary bus arbitration support for up to nine bus master devices
- Evaluation Design Kit speeds time-to-market
- Fully compliant with Revision 2.3 of the PCI specification including delayed transactions
- Available in 33 and 66 MHz

Product Overview

Intel's 21555 Non-Transparent PCI-to-PCI bridge chip enables add-in card vendors to deliver high-performance, intelligent option cards and embedded products that previously were not possible. Designed specifically for applications where a processor is used behind a PCI-to-PCI bridge, the 21555 provides a clean architecture for creating a product with multiple processor domains.

A Unique Bridge Architecture

Intel's 21555 is a unique new Non-Transparent PCI-to-PCI bridge solution. The 21555 provides designers of intelligent controllers and embedded systems with a Non-Transparent PCI-to-PCI bridge solution capable of resolving resource conflicts between a PCI-based host system and a PCI-based subsystem. This gives a local processor maximum flexibility in mapping and managing subsystem resources.

Efficient Management of System and Subsystem Resources

The 21555 provides independent primary and secondary address spaces, which allow independent host and local address mapping. With this key feature, local memory requirements need not impact the host address map. The 21555 performs address translation between the primary and secondary buses, resolving address resource conflicts between the host and local address domains.

Featuring a subsystem PCI configuration boundary, the 21555 allows the local processor to have complete PCI configuration control of subsystem devices, without host interference. This advanced feature also allows the 21555 to present a subsystem, such as a RAID controller, as a single virtual PCI device. An added benefit of this design is the ability to easily identify a single device driver for the entire subsystem. Another feature of the 21555, a serial ROM interface, allows manufacturers to customize the 21555 for a particular application by pre-loading the ROM with vendor-specific configuration data.

Flexible, Robust Design

The 21555 Non-Transparent design provides an advanced transaction forwarding engine, including deeper read and write buffers, support for more simultaneous transactions, more flexible ordering mechanisms, and more performance tuning options.

The 21555 offers high-bandwidth 64-bit primary and 64-bit secondary PCI interfaces. This interface supports application designs requiring the high performance associated with 64-bit buses.

Power Management

The 21555 Non-Transparent PCI-to-PCI bridge chip complies with the Advanced Configuration Power Interface (ACPI) and PCI Bus Power Management Interface specifications. Through serial pre-load, the 21555's power management interface can be tailored to vendor-specific application needs.

Additional Features

The 21555 supports either asynchronous or synchronous primary and secondary clocks. The chip's I_2O-compliant controller uses local memory for Inbound and Outbound List storage with on-chip prefetch and posting buffers, giving lower latency access.

The 21555 includes a parallel ROM interface that can be used to attach the Expansion ROM for the subsystem. The ROM interface can also function as a generic 8-bit multiplexed interface with programmable read, write and ready signals to allow attachment on external devices.

The chip also includes a secondary bus arbiter implementing a 2-level rotating priority algorithm, supporting nine external bus masters. In addition to incorporating a JTAG interface, the 21555 implements compact PCI hot swap support, enabling the 21555 to serve as a hot swap controller on a compact PCI card.

As a 3.3-volt device with 5.0-volt-tolerant receivers, the 21555 reduces power dissipation and enables the design of universal PCI cards.

Specifications

Characteristic	Specification
Power supply	Vdd = 3.3 V + VI/O = 5 V or 3.3 V
Operating temperature range	0° C to 70° C
Storage temperature range	-55° C to 125° C
Power dissipation	2.5 W maximum @ Vdd = 3.3 V PCI clock frequency = 66 MHz
Package	304-pin PBGA

Evaluation Design Kit Improves Time-to-market

Intel offers a 21555 Evaluation Design Kit that includes all of the tools option card suppliers need to bring 21555-based products to market quickly. The kit contains a PCI evaluation board featuring a 21555 with two PCI slots on the secondary bus, schematics, gerber files, configuration software and complete documentation.

Intel Access

Developer's Site	http://developer.intel.com/
Bridges Home Page	http://developer.intel.com/design/bridge/
Other Intel Support:	http://developer.intel.com/design/litcentr/
Intel Literature Center	(800) 548-4725 7 a.m. to 7 p.m. CST (U.S. and Canada) International locations please contact your local sales office.
General Information Hotline	(800) 628-8686 or (916) 356-3104 5 a.m. to 5 p.m. PST

For more information, visit the Intel Web site at: **developer.intel.com**

UNITED STATES AND CANADA
Intel Corporation
Robert Noyce Bldg.
2200 Mission College Blvd.
P.O. Box 58119
Santa Clara, CA 95052-8119
USA

EUROPE
Intel Corporation (UK) Ltd.
Pipers Way
Swindon
Wiltshire SN3 1RJ
UK

ASIA-PACIFIC
Intel Semiconductor Ltd.
32/F Two Pacific Place
88 Queensway, Central
Hong Kong, SAR

JAPAN
Intel Kabushiki Kaisha
P.O. Box 115 Tsukuba-gakuen
5-6 Tokodai, Tsukuba-shi
Ibaraki-ken 305
Japan

SOUTH AMERICA
Intel Semicondutores do Brazil
Rue Florida, 1703-2 and CJ22
CEP 04565-001 Sao Paulo-SP
Brazil

Order Number: 279011-001 Printed in USA/0200/5K/IL0180B CM