AZ DISPLAYS, INC.

SPECIFICATIONS FOR

LIQUID CRYSTAL DISPLAY

PART NUMBER:	AGM9624A
DATE:	September 6, 2005

General Specification

Driving IC S6B0724A

Interace With Paraller MPU 8080 Series

Display Specification

Display Dot Matrix :96*24

Display Mode:Positive/Transflective/FSTN Type

Viewing Angle :6:00 Clock

Display Duty:1/33 Driving Bias:1/6 Driving Voltage:7.5V

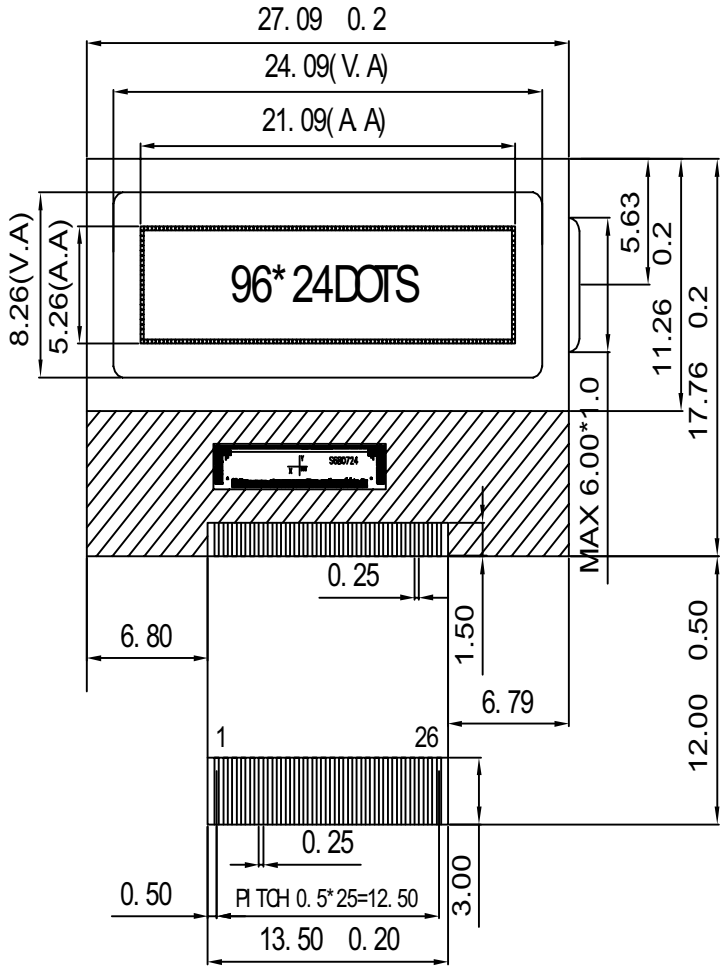
Mechanical Characteristics(Unit:mm)

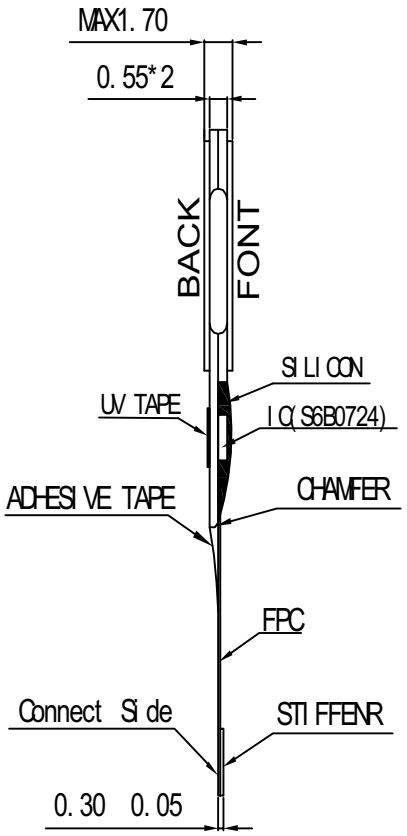
Extenal Dimension:27.09* 17.76*1.7

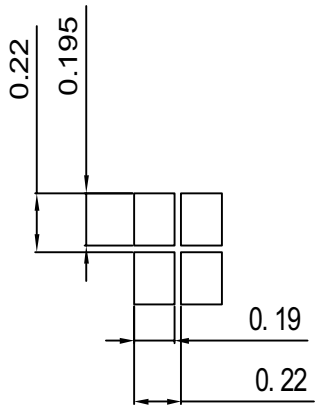
View Area:24.09* 8.26

Dots Size:0.19*0.0.195

Dots Pitch:0.22* 0.22







NO.	SYMBOL
1	V0
2	V4
3	V3
4	V2
5	V1
6	C2-
7	C2+
8	C1+
9	C1-
10	C3+
11	VOUT
12	VSS
13	VDD
14	D7
15	D6
16	D5
17	D4
18	D3
19	D2
20	D1
21	D0
22	E_RDB
23	RW_WRB
24	RS
25	/RES
26	/CS1

NOTES:

1. VIEWING ANGLE: 6:00 O'CLOCK
2. DISPLAY MODE:Shown as in table 3
3. DRIVING VOLTAGE: 7.5V,DUTY:1/33,BIAS:1/6,FREQUENCY:64Hz
4. OPERATING TEMP.:-20° C TO 70° C
5. STORAGE TEMP.:-30° C TO 80° C
6. CONNECTOR:FPC+COG TYPE

VER.	MODIFY CONTENTS	DATE	DESIGN
6			
5			
4			
3			
2			
1			

AZ DISPLAYS, INC.

PART NO. AGM9624A

DESIGN BY H.J 28/06-04

CHECKED BY

APP BY

TOLERANCES UNLESS OTHERWISE STATED

.X ±0.30

.XX ±0.10 ANGLE±1°

ALL DIMENSIONS IN MM UNLESS OTHERWISE STATED

CUSTOMER:

APPLICATION:

☐Instrument ☐Audio Equipments ☐Automobile ☒Other

☐Telephone ☐Automobile

☐Home Appliances ☐Air-condition

SAMPLE: ☐Yes ☒No

SHEET 1 OF

Absolute Maximum Ratings

Item	Symbol	Standard			Unit
Power supply voltage	V_{DD}-V_{SS}	0	-	5.5	V
Input voltage	VIN	VSS	-	VDD	
Operating temperature range	T_A	-20	-	+70	"
Storage temperature range	T_{STO}	-30	-	+80	

*Wide temperature range is available

Interface Pin Description

Pin No	Symbol	I/O	Function
26	CS1B	I	This is the chip select signal .When CS1B=# L″ and CS2=# H″,then the chip select becomes active,and data/command I/O is enabled
25	RESETB	I	When RESETB is set to "L",the setting are initialized The RESETB operation is performed by the RESETB signal level
24	RS	I	Select register. 0:Instruction register (for write) Busy flag &address counter(for read) 1:Data register(for write and read).
23	RW-WRB	I	Read/write select signal.
22	E-RDB	I	Operation (data read/write) enable signal.
21	DB0	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected,then D7 serves as the serial data input terminal and D6 serves as the serial clock input terminal.At this time,D0-D5 are set to high impedence. When the chip select is inactive,D0 to D7 are set to high impedance.
20	DB1		
19	DB2		
18	DB3		
17	DB4		
16	DB5		
15	DB6		
14	DB7		
13	VDD	Supply	Power supply for logic
12	VSS	Supply	Ground.
11	VOUT	O	DC/DC voltage converter output
10	C3+	O	Capacitor3+ for internal DC/DC voltage converter
9	C1-	O	Capacitor1- for internal DC/DC voltage converter
8	C1+	O	Capacitor1+ for internal DC/DC voltage converter
7	C2+	O	Capacitor2+ for internal DC/DC voltage converter
6	C2-	O	Capacitor2- for internal DC/DC voltage converter

<table>
<tr><td>5</td><td>V1</td><td rowspan="6">Supply</td><td rowspan="6">LCD driver supply voltages.The voltage determined by LCD cell is impedangce-converted by a resistive driver or an operation amplifier for application .Voltages should be the following relationship:
V0>V1>V2>V3>V4>VSS
When the on-chip operating power circuit is on,the following are given to V1 to V4 by the on-chip power circuit .Voltage selection is performed by the set LCD bias command.
<table>
<tr><th>LCD BIAS</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/5BIAS</td><td>4/5V0</td><td>3/5V0</td><td>2/5V0</td><td>1/5V0</td></tr>
<tr><td>1/6 BIAS</td><td>5/6V0</td><td>4/6 V0</td><td>2/6 V0</td><td>1/6 V0</td></tr>
<tr><td>1/7 BIAS</td><td>6/7 V0</td><td>5/7 V0</td><td>2/7 V0</td><td>1/7 V0</td></tr>
<tr><td>1/8 BIAS</td><td>7/8 V0</td><td>6/8 V0</td><td>2/8 V0</td><td>1/8 V0</td></tr>
<tr><td>1/9 BIAS</td><td>8/9 V0</td><td>7/9 V0</td><td>2/9 V0</td><td>1/9 V0</td></tr>
</table>
</td></tr>
<tr><td>4</td><td>V2</td></tr>
<tr><td>3</td><td>V3</td></tr>
<tr><td>2</td><td>V4</td></tr>
<tr><td>1</td><td>V0</td></tr>
</table>

Electrical Characteristics

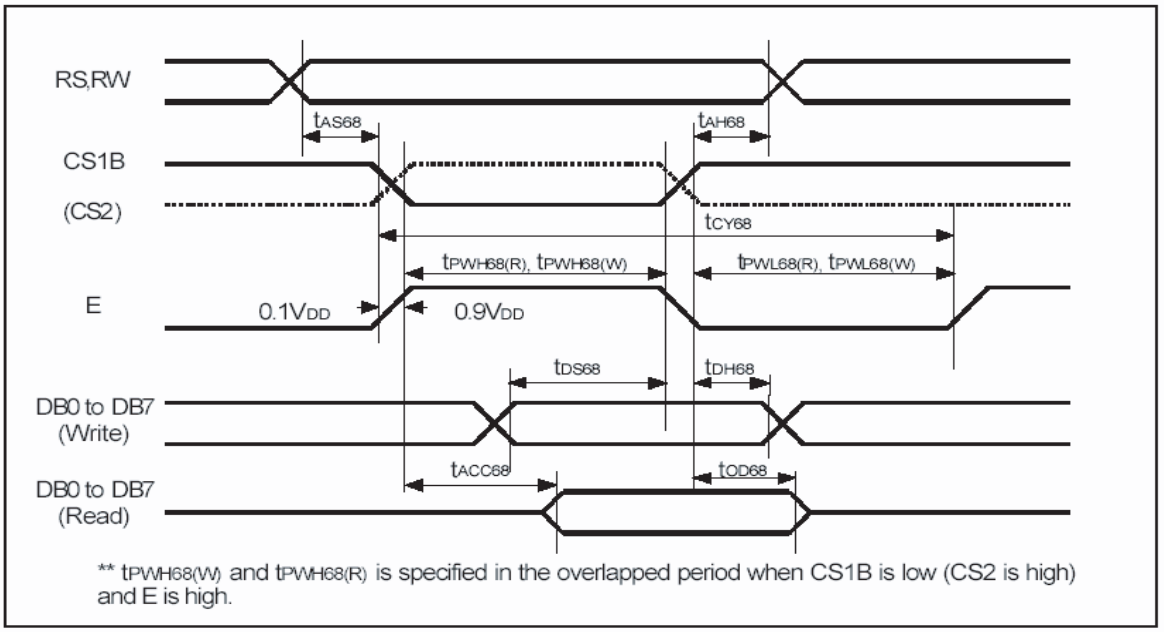
DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 5.5V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}	Select by product code	2.4	-	3.6	V	VDD *1
				2.4	-	5.5		
Operating voltage (2)		V0		4.5	-	15.0	V	V0 *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{DD} = 3.0V V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	μA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	μA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency	Internal	f_{OSC}	V_{DD} = 3.0V Ta = 25°C Duty ratio = 1/65	32.7	43.6	54.5	kHz	CL *8
	External	f_{CL}		4.09	5.45	6.81		
Voltage converter input voltage		VCI	× 2	2.4	-	5.5	V	VCI
			× 3	2.4	-	5.0		
			× 4	2.4	-	3.75		
			× 5	2.4	-	3.0		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT		6.0	-	16.0	V	VOUT
Voltage follower operating voltage		V0		4.5	-	15.0	V	V0 *9
Reference voltage		V_{REF}	V_{DD}= 3.0V Ta = 25°C	- 0.05%/°C	2.04	2.1	2.16	V	*10

AC Characteristics

Read / Write Characteristics (6800-series Microprocessor)



** $t_{PWH68(W)}$ and $t_{PWH68(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and E is high.

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS,RW	tAS68 tAH68	0 0	-	-	ns	
System cycle time		E	tCY68	300	-	-	ns	
Enable Pulse High Width	Read	E	tPWH68 (R)	120			ns	
	Write		tPWH68 (W)	60				
Enable Pulse Low Width	Read	E	tPWL68 (R)	60			ns	
	Write		tPWL68 (W)	60				
Data setup time Data hold time		DB7 To DB0	tDS68 tDH68	40 15	-	-	ns	
Access time Output disable time			tACC68 tOD68	- 10	-	140 100	ns	CL = 100 pF

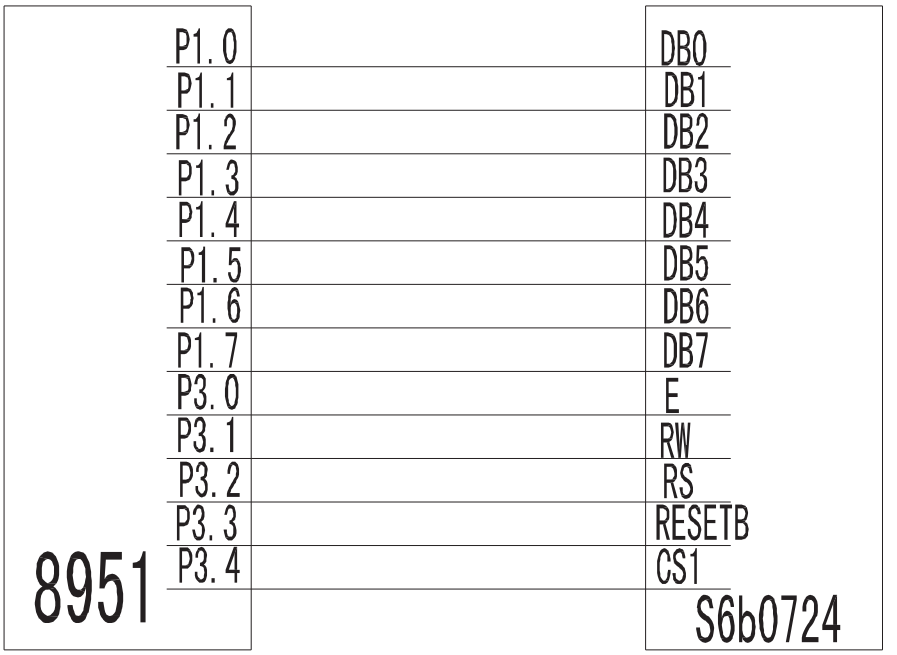
(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS,RW	tAS68 tAH68	0 0	-	-	ns	
System cycle time		E	tCY68	166	-	-	ns	
Enable Pulse High Width	Read	E	tPWH68 (R)	70			ns	
	Write		tPWH68 (W)	30				
Enable Pulse Low Width	Read	E	tPWL68 (R)	30			ns	
	Write		tPWL68 (W)	30				
Data setup time Data hold time		DB7 To DB0	tDS68 tDH68	30 10	-	-	ns	
Access time Output disable time			tACC68 tOD68	- 10	-	70 50	ns	CL = 100 pF

Note: 1. The input signal rising time and falling time (tr, tf) is specified at 15ns or less. Or (tr + tf) < (t_{CY68} – $t_{PWL68 (W)}$ – $t_{PWH68 (W)}$) for write, (tr + tf) < (t_{CY68} – $t_{PWL68 (R)}$ – $t_{PWH68 (R)}$) for read.

Application Example

1.



2.