AKD4588
Evaluation board Rev.C for AK4588

FEATURE

The AKD4588 is an evaluation board for the AK4588, a single chip 24bit CODEC that includes two channels of ADC and eight channels of DAC with internal DIR, DIT. The AKD4588 has the interface with AKM's A/D converter evaluation boards and AKM's D/A converter evaluation boards. Therefore, it is easy to evaluate the AK4588. The AKD4588 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector or BNC connector.

■ Ordering guide

AKD4588 --- Evaluation board for AK4588
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software dose not support Windows NT.)

FUNCTION

- ☐ **On-board clock generator**
- ☐ **Compatible with 2 types of interface**
  - **- Optical output/input and BNC input**
  - **- Direct interface with AC3 decoder by 10pin header**
- ☐ **10pin header for serial control interface**

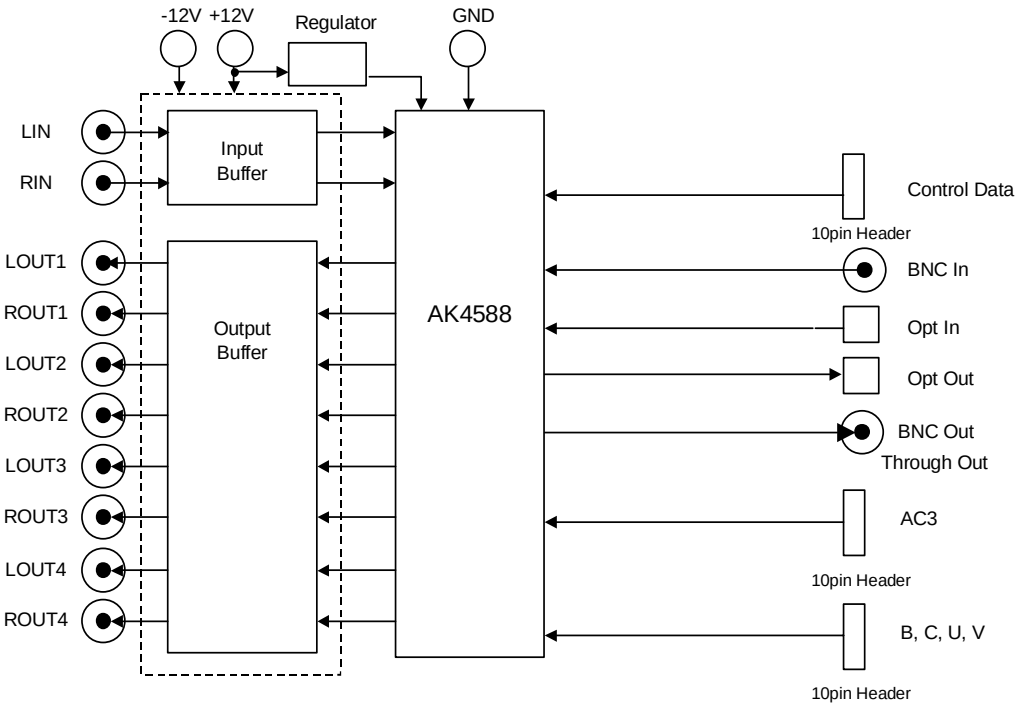


Figure 1 AKD4588 Block Diagram
* Circuit diagram and PCB layout are attached at the end of this manual.

■ Analog Inputs

Analog inputs use J10 (LIN) and J9 (RIN) the analog inputs are single-ended. Each channel signal range is nominally 3.1Vpp@5V. It is proportional to VREFH (Vin=0.6 x VREFH). VREFH is connected to AVDD on the AKD4588.

■ Analog Outputs

J2 (LOUT1), J1 (ROUT1), J4 (LOUT2), J3 (ROUT2), J6 (LOUT3), J5 (ROUT3) J8 (LOUT4) and J7 (ROUT4) are used for analog outputs. The analog outputs are single-ended. Each channel signal range is nominally 3.0Vpp@5V. It is proportional to VREFH (Vin= 0.6 x VREFH). VREFH is connected to AVDD on the AKD4588.

■ Digital Inputs

Toslink (TORX176: PORT3) or BNC connector (J12) is used for digital inputs. When Toslink (TORX176: PORT3) is used, JP3 (RX0) set "OPT" side. When BNC connector (J12) is used, JP3 (RX0) set "BNC" side.

■ Digital Outputs

Digital outputs use Toslink (TOTX176: PORT2), BNC connector (J11). When Toslink (PORT2) is used for TX1, JP2 (TX1) set "OPT" side. When BNC connector (J11) is used, JP2 (TX1) set "BNC" side.

■ Operation sequence

1) Set up the power supply lines. (See "Other jumpers set-up".)

Name	Color	Voltage	Comments	Attention
+12V	Red	+12~+15V	Regulator, Power supply for Op-amp.	This jack is always needed. Power line
-12V	Blue	-12~-15V	Regulator, Power supply for Op-amp.	This jack is always needed. Power line
AGND	Black	0V	GND	This jack is always needed.
DGND	Black	0V	GND	

Table 1 Set up of power supply lines

Each supply line should be distributed from the power supply unit.

2) Evaluation Mode

(1) Evaluation of DAC part used internal DIR
(2) Evaluation of ADC part used internal DIT

(See the followings)

3) Set-up the evaluation modes, jumper pins and DIP switches. (See the followings.)

4) Power on

The AK4588 should be reset once bringing SW1 (PDN) "L" upon power-up.

■ Evaluation mode

Evaluation of DAC part used internal DIR

1-1. Digital input (Bi-phase input)

1-1-1. Digital input (Bi-phase input) is used by Optical Link PORT3 (TORX176). And Digital input (Bi-phase input) is used by BNC connector J12.

1-1-2. Set the part of (DIR/DIT part) control resister software (addr00H: CM10=00) is (Clock Mode is PLL Mode.)
This mode is able to operate by default setting.

DIP-SW SW2-2 (MASTER) is ON. Audio Digital Interface Format is 24bit left justified at this time.(Refer datasheet.).

1-1-3. When Digital input (Bi-phase input) is used for RX0 pin, Optical Link PORT3 (TORX176) or BNC Connector J12 is used. JP3 (RX0) selects this. (Refer Figure 2)

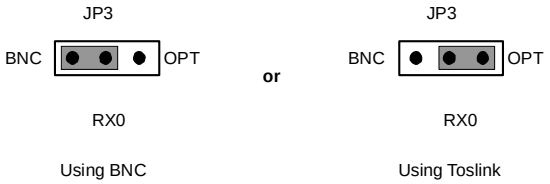


Figure 2 Selection of Digital input (Bi-phase input)

1-2. Analog Output

1-2-1. Analog Output used BNC connector J2 (LOUT1), J1 (ROUT1), J4 (LOUT2), J3 (ROUT3), J6 (LOUT3), J8 (LOUT), J7 (ROUT4).

1-2-2. Analog Output can be selected of output buffer (OP-Amp: Gain=2) is using or not using.
This is selected JP5 (LOUT1), JP4 (ROUT1), JP10 (LOUT2), JP6 (ROUT2), JP12 (LOUT3), JP11 (ROUT3), JP16 (LOUT4) and JP15 (ROUT4) (Refer Figure8~9.)

(2) ADC Evaluation of using internal DIT

2-1. Analog input

2-1-1. BNC connectors J10 (LIN) and J9 (RIN) are used for analog input.

2-2. Digital output (bi-phase output)

2-2-1. PORT2 (TORX176) or J11 (TX1) is used for digital output.

2-2-2. Digital output (bi-phase output) is selected using Toslink (TOTX176: PORT2) or using BNC Connecter J11 (TX1) by JP2 (TX1) (Refer Figure3.)

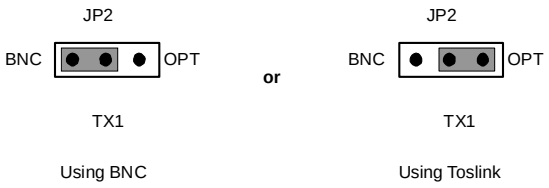


Figure 3 Selection of digital output (bi-phase)

2-2-3. Set the part of (DIR/DIT part) control resister software (addr00H: CM10=01) is (Clock Mode is X'tal Mode.)

2-2-4. Clock source is X1 (X'tal).

2-2-5. DIP-SW SW2-2 (MASTER) is ON. Audio Digital Interface Format is 24bit, left justified at this time. (Refer datasheet.).

■ Setting of DIP-SW2

[SW2]: Setting of AK4588

No.	Pin	OFF	ON	Default
1	-	-	-	OFF
2	MASTER	Slave Mode	Master Mode	ON
3	XTL1	Reference X'tal frequency (Refer Table 4,5)		ON
4	XTL0			ON
5	CAD1	Setting of Chip Address (ADC/DAC PART)		OFF
6	CAD0	Setting of Chip Address (ADC/DAC PART)		ON

Table 2 Setting of SW2 (No.3~6;ON: 1, OFF:0)

■ Sampling frequency as follows

AK4588 has two methods for detecting the sampling frequency. Clock is compared between recovered clock and X'tal oscillator by XTL1-0. This information outputs FS0, FS1, and FS2, FS3 bit for detecting the sampling frequency. The compared X'tal frequency is selected by setting of XTL1-0 (Refer Table 4.) When XTL1-0 is 11, X'tal oscillator is stopped and the encored sampling frequency information of channel status output FS0, FS1, FS2, FS3, PEM bit of resister control.

XTL1	XTL0	X'tal Frequency	
0	0	11.2896MHz	
0	1	12.288MHz	
1	0	24.576MHz	
1	1	(use channel status)	Default

Table 3 Reference X'tal frequency

Register output				fs	Except XTL1,0= "1,1"	XTL1, 0= "1,1"		
					Clock comparison (Note 1)	Consumer mode (Note 2)	Professional mode	
FS3	FS2	FS1	FS0			Byte3 Bit3, 2,1,0	Byte0 Bit7, 6	Byte4 Bit6, 5,4,3
0	0	0	0	44.1kHz	44.1kHz	0 0 0 0	0 1	0 0 0 0
0	0	0	1	Reserved	Reserved	0 0 0 1	(Others)	
0	0	1	0	48kHz	48kHz	0 0 1 0	1 0	0 0 0 0
0	0	1	1	32kHz	32kHz	0 0 1 1	1 1	0 0 0 0
1	0	0	0	88.2kHz	88.2kHz	(1 0 0 0)	0 0	1 0 1 0
1	0	1	0	96kHz	96kHz	(1 0 1 0)	0 0	0 0 1 0
1	1	0	0	176.4kHz	176.4kHz	(1 1 0 0)	0 0	1 0 1 1
1	1	1	0	192kHz	192kHz	(1 1 1 0)	0 0	0 0 1 1

Note1: At least ±3% range is identified as the value in the Table 4. In case of intermediate frequency of those two, FS3-0 bits indicate nearer value. When the frequency is much bigger than 192kHz or much smaller than 32kHz, FS3-0 bits may indicate "0001".

Note2: When consumer mode, Byte3 Bit3-0 are copied to FS3-0 bits.

Table 4 fs Information

■ Jumper setting

[JP1] (GND): Analog grand and digital grand

Open: Analog grand and digital grand is separated. < Default>
Short: Analog grand and digital grand is common. “DGND” jack is able to open at this time.

■ Operation of toggle switch.

[SW1](PDN): Resetting of AK4588. It must be “H” during operation this board.

■ Indication of LED

It turns on each pin when each pin output is “H”.

[LE1] (INT0): Indicate of AK4588’s INT0 pin output.
[LE2] (INT1): Indicate of AK4588’s INT1 pin output.

■ Serial Control

The AK4588 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT1 (uP-I/F) with PC by 10 wire flat cable packed with the AKD4588.

Be careful connector direction. Flat cable should be connected 10-pin header, red line put on 10pin header 5 and 6 pin.

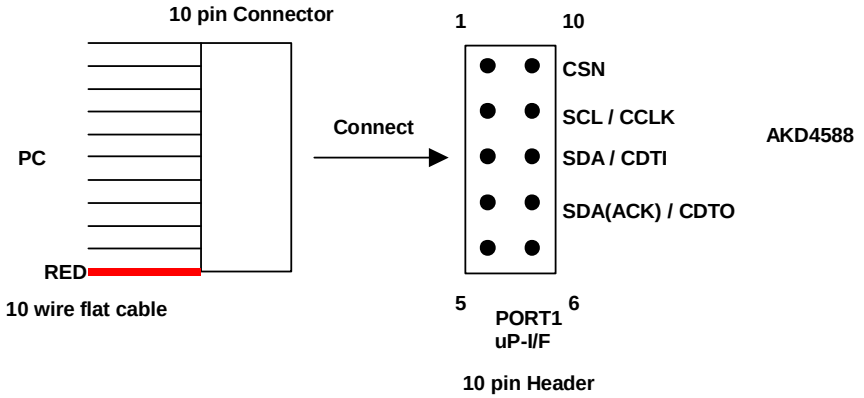


Figure 4 The connection of 10 flat cable.

■ Interface of AC3 decoder

AC3 decoder is able to be interface by using PORT5 (ADC/DAC).
Three serial data is input through PORT5 form AC3 decoder input.
PORT5 pin order is showed Figure 5

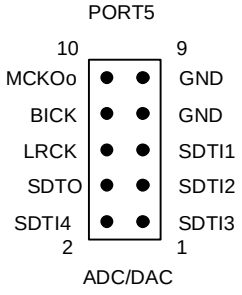


Figure 5 PORT5 pin order

■ B, U, C, V output and V input

B, U, C, V output and V input is used PORT4 (BUCV).
PORT4 pin order is showed Figure 6.

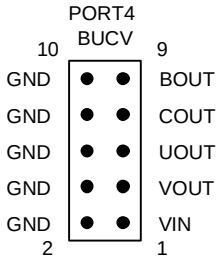


Figure 6 PORT4 pin order

AKD4588 (DIR/DIT) part Control Program operation manual

■ Set-up of evaluation board and control software

1. Set up the AKD4588 (DIR/DIT) according to previous term.

2. Connect IBM-AT compatible PC with AKD4588 by 10-line type flat cable (packed with AKD4588). Take care of the direction of 10pin header. (Please install the driver in the floppy-disk when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AK4588 Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "AKD4588 (DIR/DIT)-1.exe" (address 00H-0FH) to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Then set up the dialog and input data.

■ Explanation of each buttons

1. [Port Setup]: set up the printer port.
2. [Write default]: initialize the register of AK4588.
3. [All read]: read all registers.
4. [Read]: read data from each register.
5. [Write]: write data to each register.

If you want to write the input data to AK4588, click "OK" button. If not, click "Cancel" button.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

AK4588 (ADC/DAC) part Control Program Operation Manual

■ Set-up of evaluation board and control software

This evaluation board does not support to I^2C control.

1. Set up the AKD4588 according to above mentioned setting.

2. Connect IBM-AT compatible PC with AKD4588 by 10-line type flat cable (packed with AKD4588). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM-disk when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM-disk labeled "AKD4588 Control Program ver 1.0" into the CD-ROM-disk drive.

4. Access the CD-ROM-disk drive and double-click the icon of "AKD4588 (DIR/DIT)-1.exe" (address 00H-0FH) to set up the control program.

5. Then please evaluate according to the followings.

Attention: Please use fixed "CAD1-0=01".

■ Operation flow

Keep the following flow.

1. Set up the control program.
2. Then set up the dialog and input data.

   If you want to write the input data to AK4588, click "OK" button. If not, click "Cancel" button.

■ Explanation of each buttons

1. [Port Setup]: Set up the printer port.
2. [Write default]: Initialize the register of AK4588.
3. [Function1]: Dialog to write data by keyboard operation.
4. [Function2]: Dialog to evaluate IPGA and ATTL/ATTR/ATTM.
5. [Write]: Write data to each register.

■ Explanation of each dialog

1. [Function1 Dialog]: Dialog to write data by keyboard operation

   Address Box: Input registers address in 2 figures of hexadecimal.
   Data Box: Input registers data in 2 figures of hexadecimal.

   If you want to write the input data to AK4588, click "OK" button. If not, click "Cancel" button.

2. [Function2 Dialog]: Dialog to evaluate IPGA and ATTL/ATTR/ATTM

   This dialog corresponds to only addr=0BH, 0CH and 0DH.

   Address Box: Input register address in 2 figures of hexadecimal.

Start Data Box: Input start data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4588 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4588, click “OK” button. If not, click “Cancel” button.

3. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the “Write” button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to AK4588, click “OK” button. If not, click “Cancel” button.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Attention on the operation

If you set up Function1 or Function2 dialog, input data to all boxes. Attention dialog is indicated if you input data or address that is not specified in the datasheet or you click “OK” button before you input data. In that case set up the dialog and input data once more again. These operations does not need if you click “Cancel” button or check the check box.

Measure Result

1) ADC part

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : fs=48kHz:256fs, fs=96kHz:256fs
- BICK : 64fs
- fs : 48kHz, 96kHz
- BW : 10Hz~20kHz (fs=48kHz), 10Hz~40kHz (fs=96kHz)
- Bit : 24bit
- Power Supply : AVDD=PVDD=DVDD=5V, TVDD=3.3V
- Interface : Internal DIT (48kHz, 96kHz), PSIA (192kHz)
- Temperature : Room

fs=48kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, -0.5dB	20kLPF	96.6 dB
DR	1kHz, -60dB	20kLPF	99.5 dB
DR	1kHz, -60dB	20kLPF, A-weighted	102.3 dB
S/N	No signal	20kLPF, A-weighted	99.6 dB
S/N	No signal	20kLPF, A-weighted	102.6 dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, -0.5dB	fs/2	91.7 dB
DR	1kHz, -60dB	fs/2	97.7 dB
DR	1kHz, -60dB	20kLPF, A-weighted	104.2 dB
S/N	No signal	fs/2	97.7 dB
S/N	No signal	20kLPF, A-weighted	104.5 dB

2) DAC part

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 256fs (48kHz, 96kHz), 128fs (192kHz)
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- Resolution : 24bit
- Power Supply : AVDD=PVDD=DVDD=5V, TVDD=3.3V
- Interface : Internal DIR (48kHz, 96kHz), PSIA (192kHz)
- Temperature : Room

fs=48kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	20kLPF	96.4 dB
DR	1kHz, -60dB	20kLPF	102.9 dB
DR	1kHz, -60dB	20kLPF, A-weighted	105.7 dB
S/N	“0” data	20kLPF	102.9 dB
S/N	“0” data	20kLPF, A-weighted	105.9 dB

fs=96kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	40kLPF	94.5 dB
DR	1kHz, -60dB	40kLPF	99.8 dB
DR	1kHz, -60dB	22kLPF, A-weighted	104.5 dB
S/N	“0” data	40kLPF	100.7 dB
S/N	“0” data	22kLPF, A-weighted	105.3 dB

fs=192kHz

Parameter	Input signal	Measurement filter	Results
S/(N+D)	1kHz, 0dB	40kLPF	94.0 dB
DR	1kHz, -60dB	40kLPF	100.8 dB
DR	1kHz, -60dB	22kLPF, A-weighted	105.6 dB
S/N	“0” data	40kLPF	100.7 dB
S/N	“0” data	22kLPF, A-weighted	105.8 dB

■ プロット図

1) ADC

[Measurement condition]

- Measurement Unit : Audio Precision System two Cascade
- MCLK : 256fs(fs=44.1kHz), 256fs(fs=96kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz
- BW : 20Hz~20kHz (fs=44.1kHz), 40Hz~40kHz (fs=96kHz)
- Resolution : 24bit
- Power Supply : AVDD=PVDD=DVDD=5V, TVDD=3.3V
- Interface : Internal DIR (fs=44.1kHz, 96kHz)
- Temperatur : Room

fs=44.1kHz

Figure 7 FFT (1kHz, 0dBFS input)
Figure 8 FFT (1kHz, -60dBFS input)
Figure 9 FFT (noise floor)
Figure 10 THD+N vs Input Level (fin=1kHz)
Figure 11 THD+N vs fin (Input level=0dBFS)
Figure 12 Linearity (fin=1kHz)
Figure 13 Frequency Response (Input level=0dBFS)
Figure 14 Cross-talk (Input level=0dBFS)

fs=96kHz

Figure 15 FFT (1kHz, 0dBFS input)
Figure 16 FFT (1kHz, -60dBFS input)
Figure 17 FFT (noise floor)
Figure 18 THD+N vs Input Level (fin=1kHz)
Figure 19 THD+N vs fin (Input level=0dBFS)
Figure 20 Linearity (fin=1kHz)
Figure 21 Frequency Response (Input level=0dBFS)
Figure 22 Cross-talk (Input level=0dBFS)

FFT point=16384, Avg=8, Window=Equirriple

2) DAC

[Measurement Condition]

- Measurement Unit : Audio Precision System two Cascade
- MCLK : 256fs(fs=44.1kHz), 256fs(fs=96kHz), 128fs(fs=192kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- BW : 20Hz~20kHz (fs=44.1kHz), 40Hz~40kHz (fs=96kHz), 40Hz~80kHz (fs=192kHz)
- Resolution : 24bit
- Power Supply : AVDD=PVDD=DVDD=5V, TVDD=3.3V
- Interface : Internal DIR (48kHz, 96kHz), PSIA (192kHz)
- Temperature : Room

fs=44.1kHz

Figure 23 FFT (1kHz, 0dBFS input)
Figure 24 FFT (1kHz, -60dBFS input)
Figure 25 FFT (noise floor)
Figure 26 FFT (out-of-band noise)
Figure 27 THD+N vs Input Level (fin=1kHz)
Figure 28 THD+N vs fin (Input level=0dBFS)
Figure 29 Linearity (fin=1kHz)
Figure 30 Frequency Response (Input level=0dBFS)
Figure 31 Cross-talk (Input level=0dBFS)

fs=96kHz

Figure 32 FFT (1kHz, 0dBFS input)
Figure 33 FFT (1kHz, -60dBFS input)
Figure 34 FFT (noise floor)
Figure 35 FFT (outband noise)
Figure 36 THD+N vs Input Level (fin=1kHz)
Figure 37 THD+N vs fin (Input level=0dBFS)
Figure 38 Linearity (fin=1kHz)
Figure 39 Frequency Response (Input level=0dBFS)
Figure 40 Cross-talk (Input level=0dBFS)

fs=192kHz

Figure 41 FFT (1kHz, 0dBFS input)
Figure 42 FFT (1kHz, -60dBFS input)
Figure 43 FFT (noise floor)
Figure 44 FFT (outband noise)
Figure 45 THD+N vs Input Level (fin=1kHz)
Figure 46 THD+N vs fin (Input level=0dBFS)
Figure 47 Linearity (fin=1kHz)
Figure 48 Frequency Response (Input level=0dBFS)
Figure 49 Cross-talk (Input level=0dBFS)

FFT point=16384, Avg=8, Window=Equirriple

1.ADC

(ADC fs=48kHz)

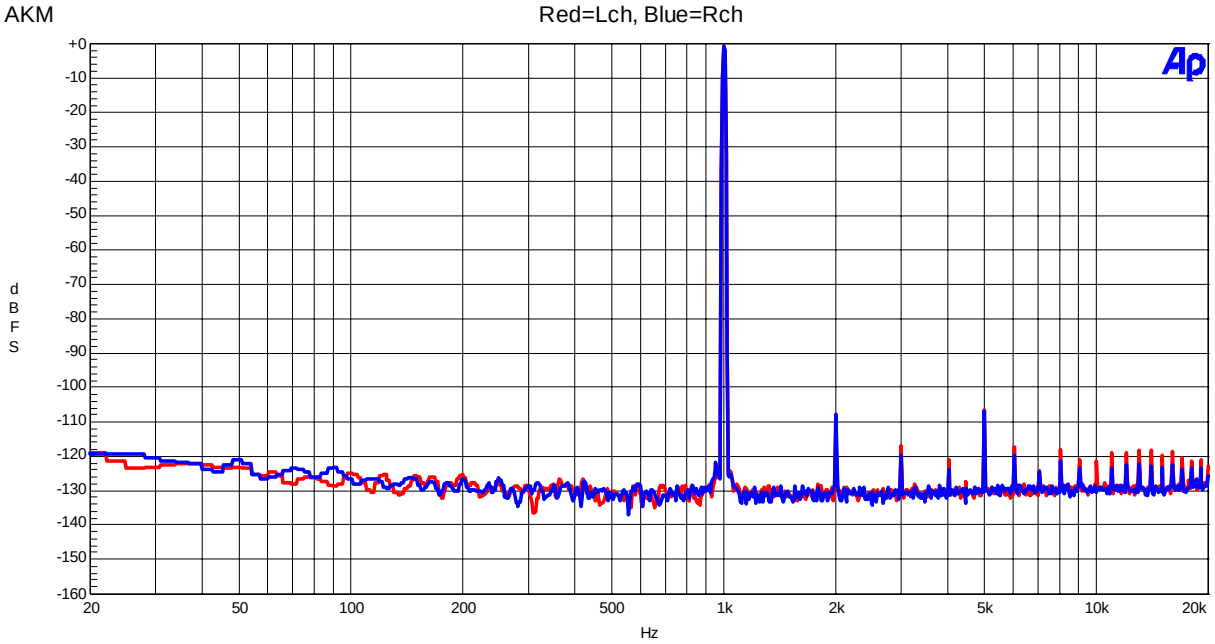


Figure 7 (Input=-0.5dBFS, fin=1kHz)

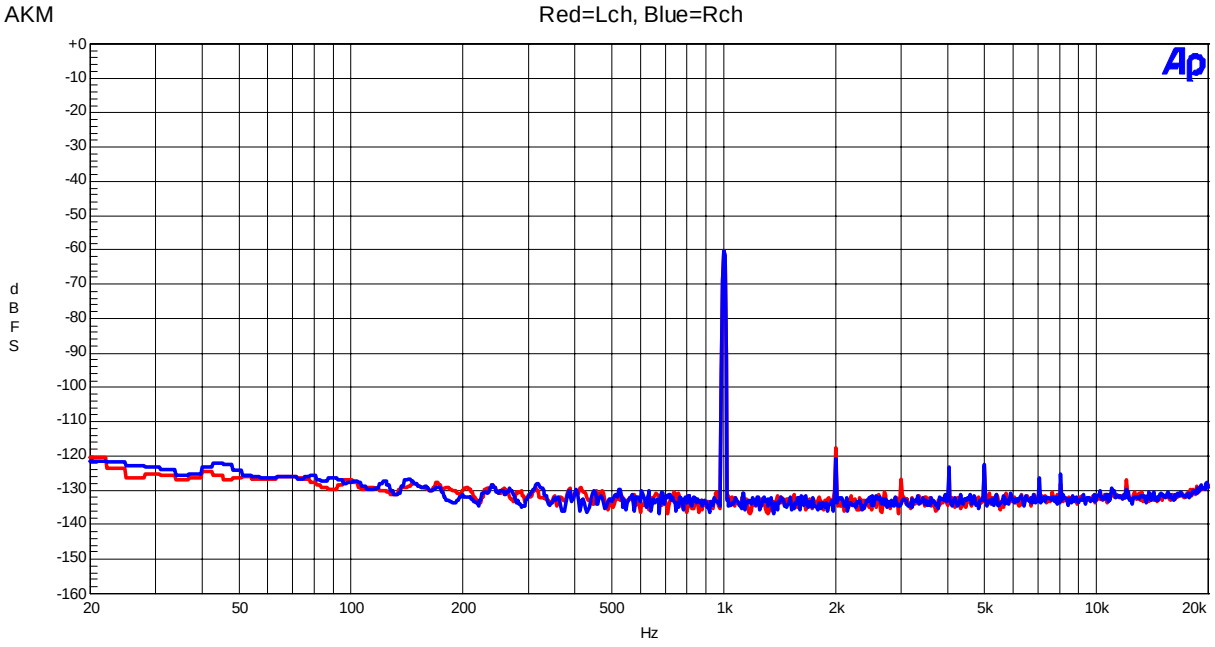


Figure 8 (Input=-60dBFS, fin=1kHz)

(ADC fs=48kHz)

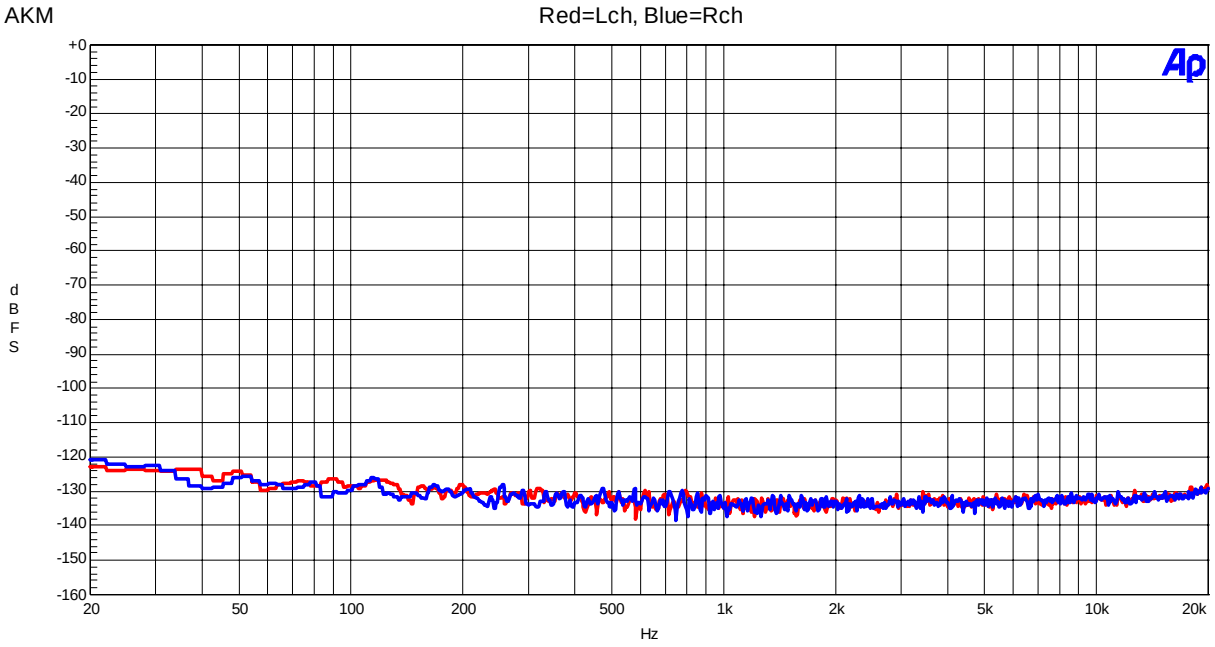


Figure 9 (noise floor)

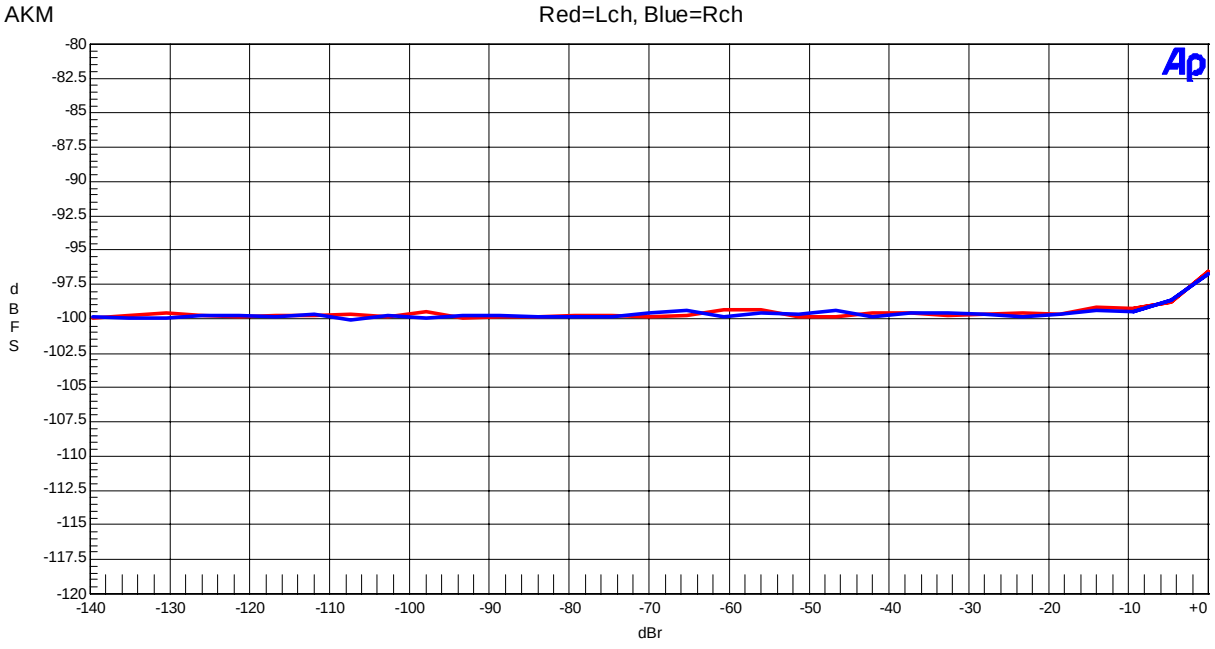


Figure 10 THD + N vs Amplitude (fin=1kHz)

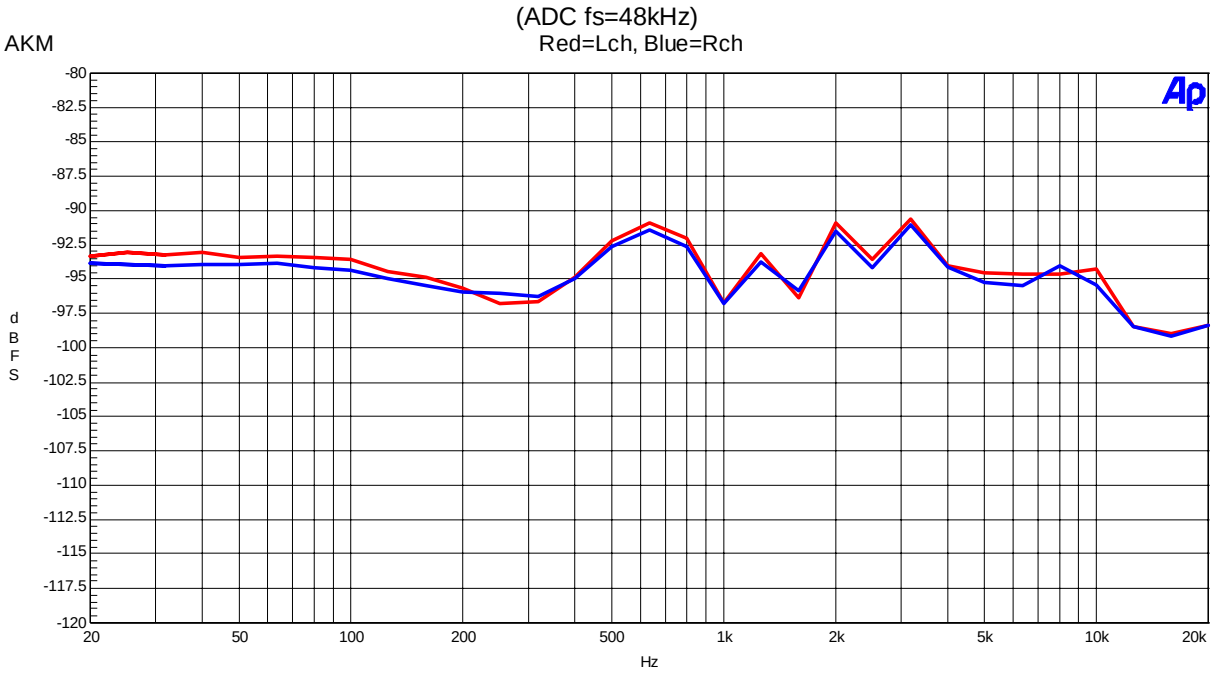


Figure 11 THD + N vs Input Frequency (Input=-0.5dBFS)

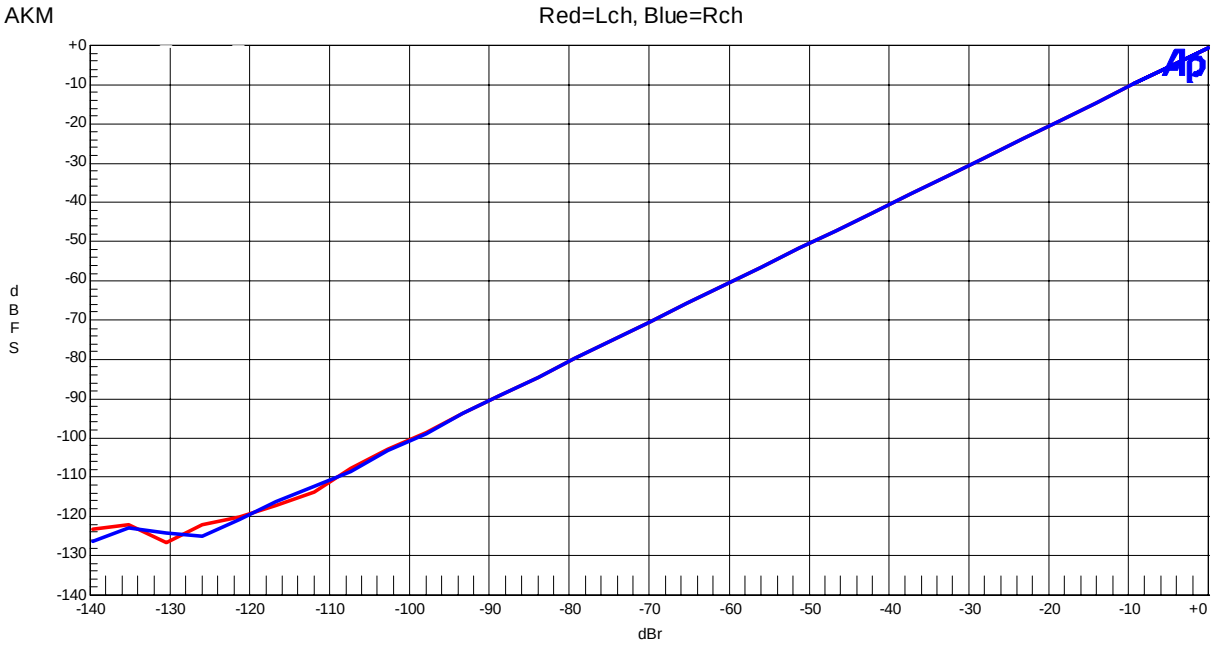


Figure 12 Linearity (fin=1kHz)

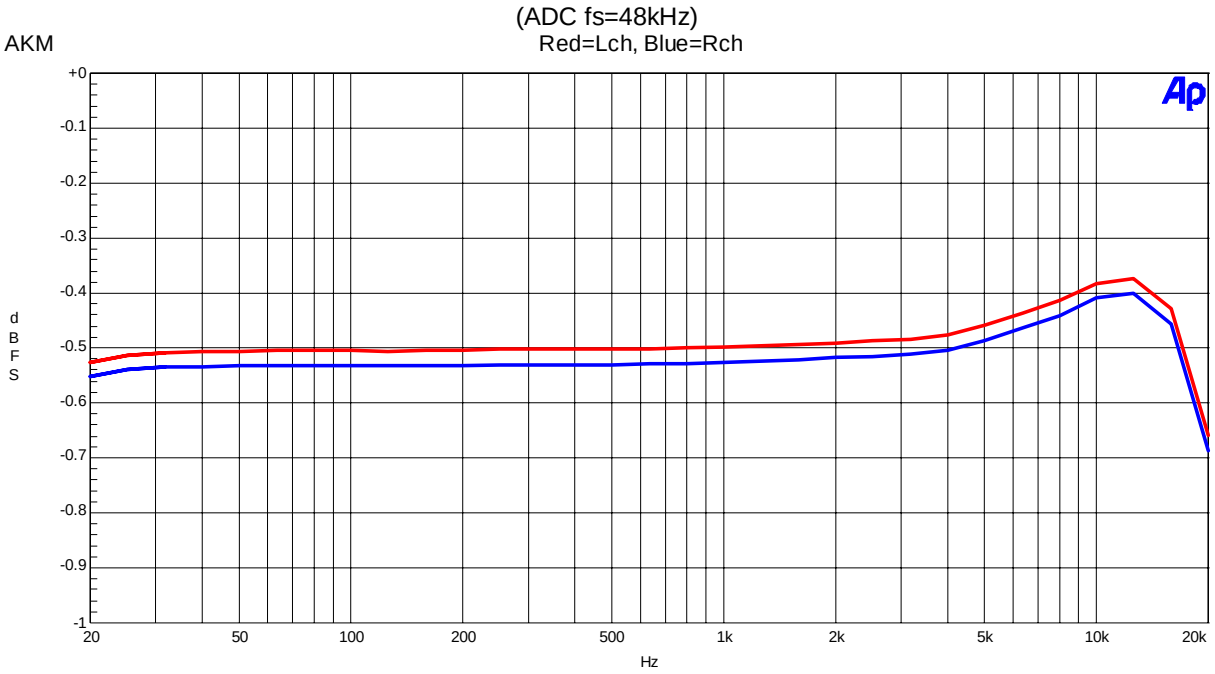


Figure 13 Frequency Response(Input Level=-0.5dBFS)
(including input RC filter)

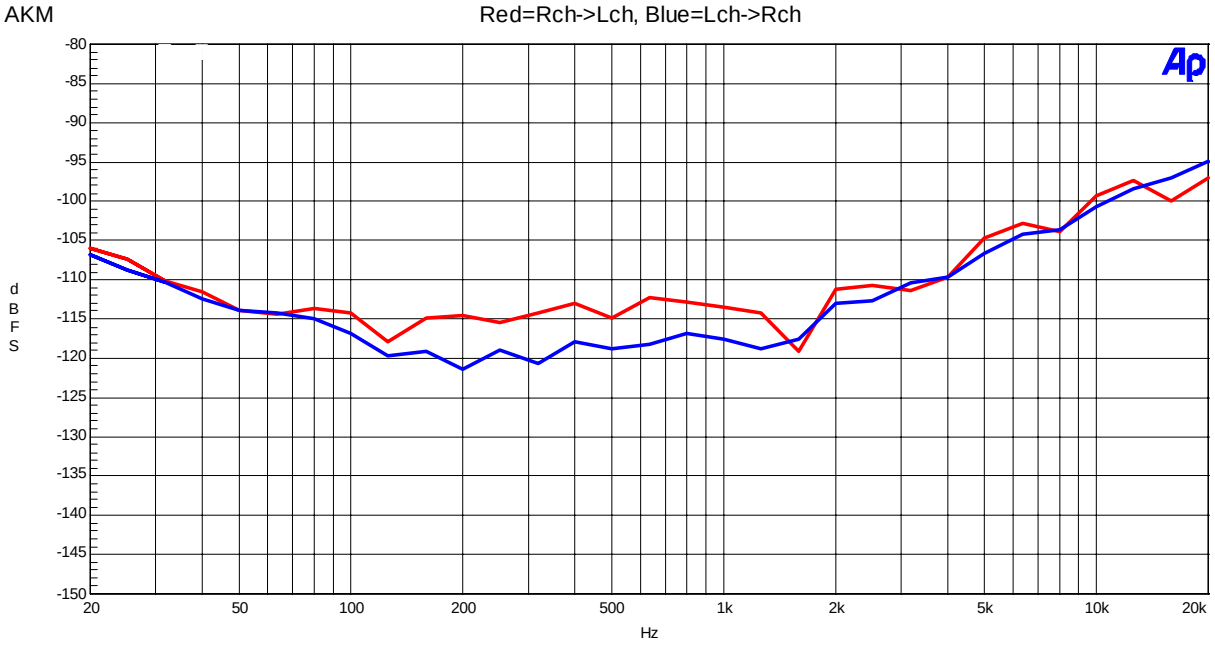


Figure 14 Crosstalk (Upper@1k = Rch, Lower@1k = Lch)

(ADC fs=96kHz)

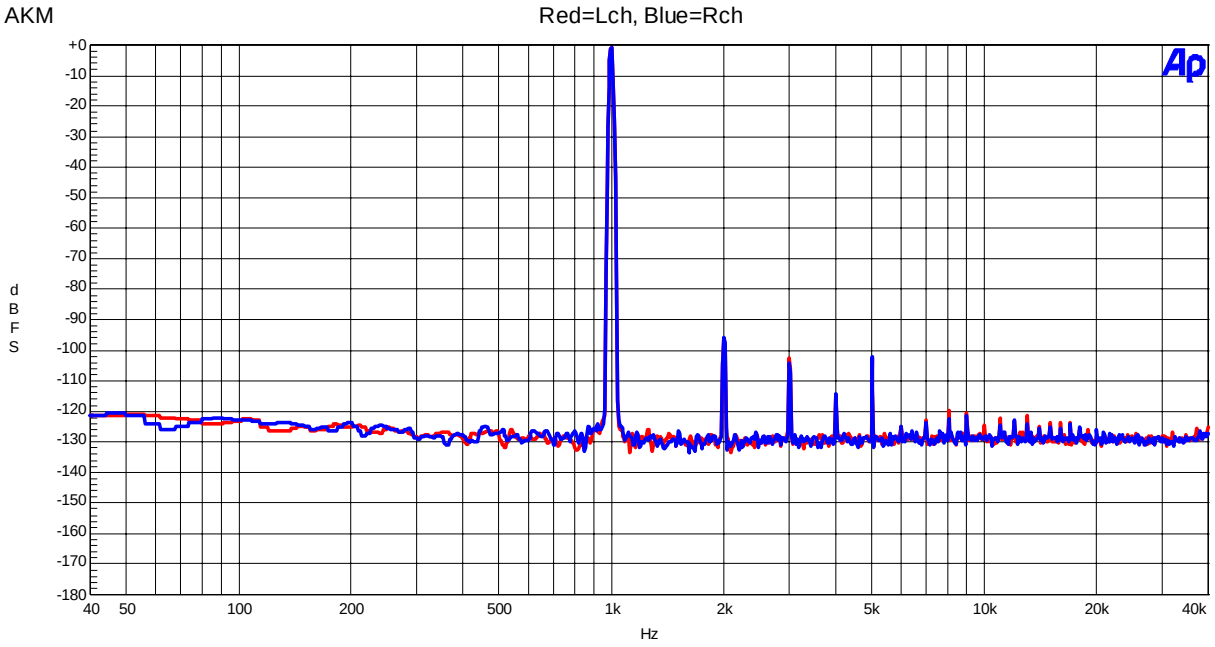


Figure 15 FFT (Input=-0.5dBFS, fin=1kHz)

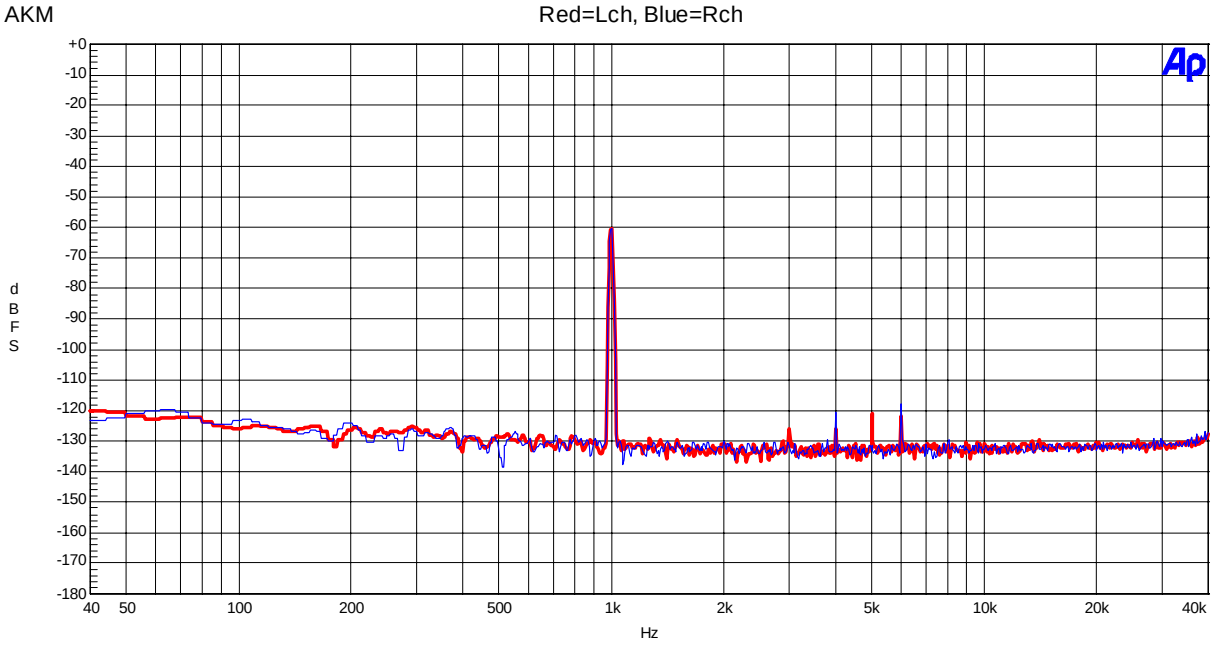


Figure 16 FFT (Input=-60dBFS, fin=1kHz)

(ADC fs=96kHz)

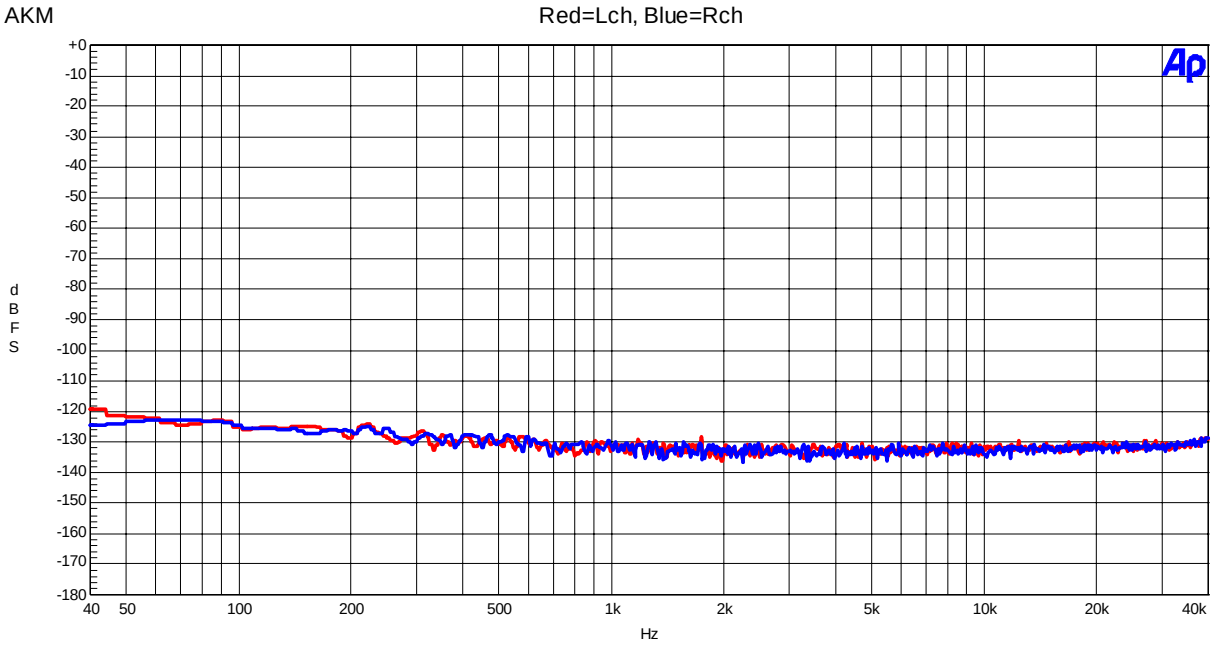


Figure 17 FFT (Noise floor)

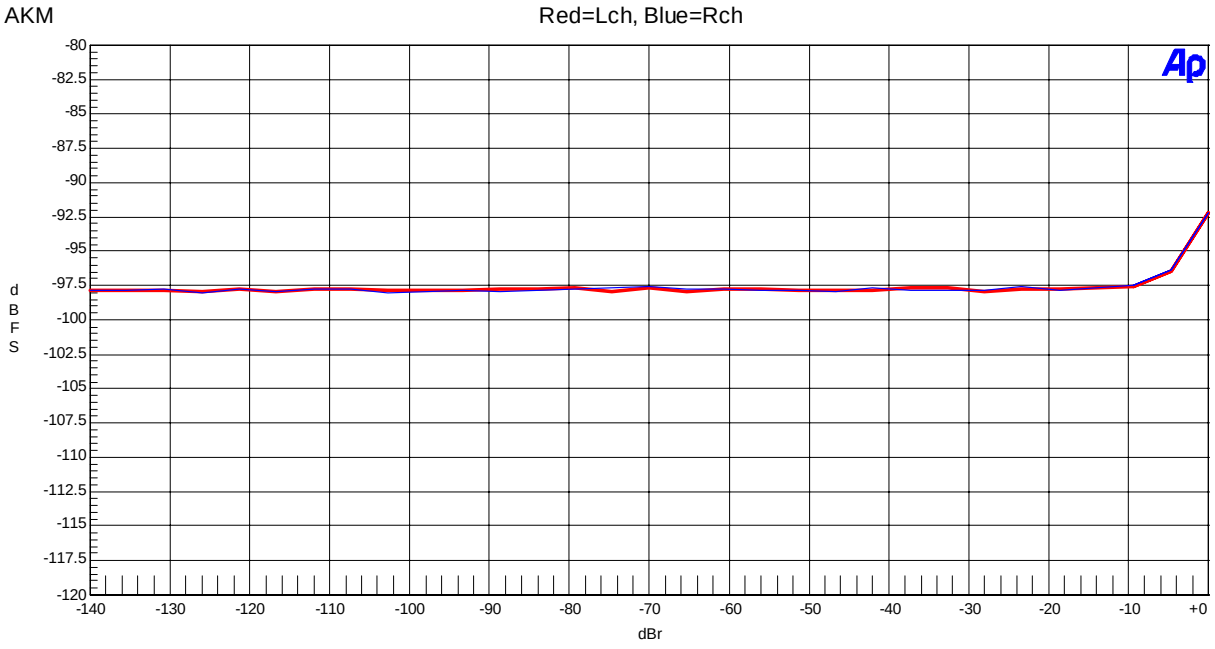


Figure 18 THD + N vs Amplitude (fin=1kHz)

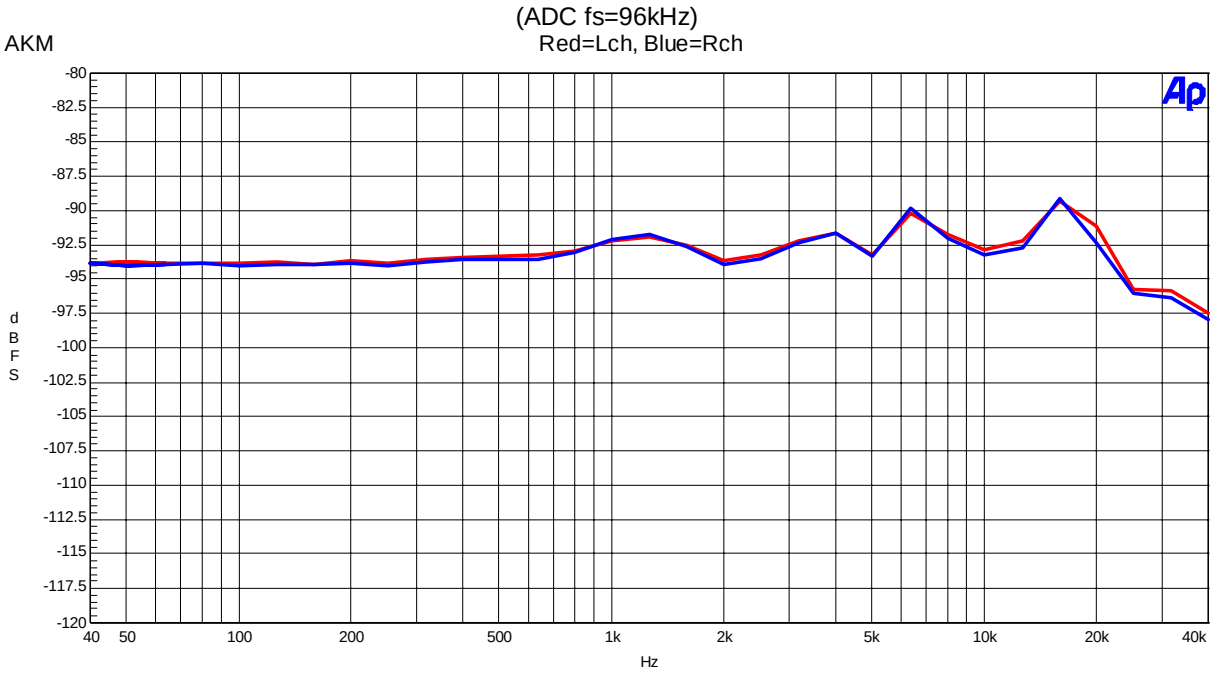


Figure 19 THD + N vs Input Frequency (Input Level=-0.5dBFS)

Figure 20 Linearity (fin=1kHz)

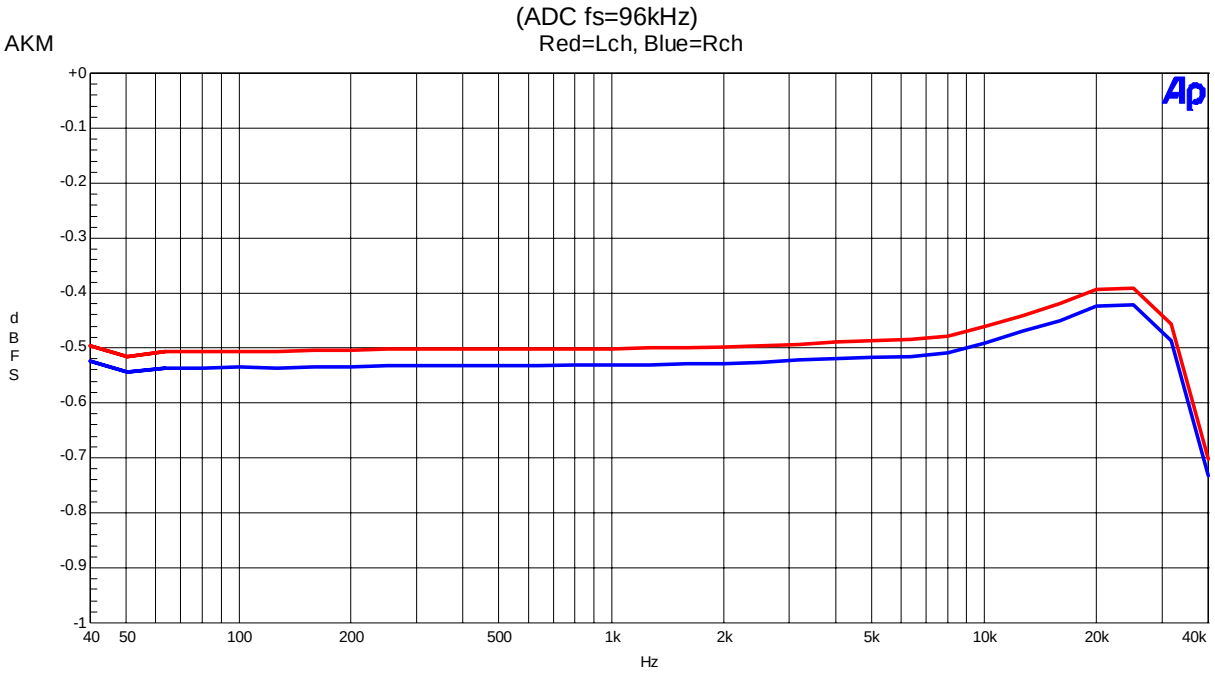


Figure 21 Frequency Response (Input Level=-0.5dBFS)
(including input RC filter)

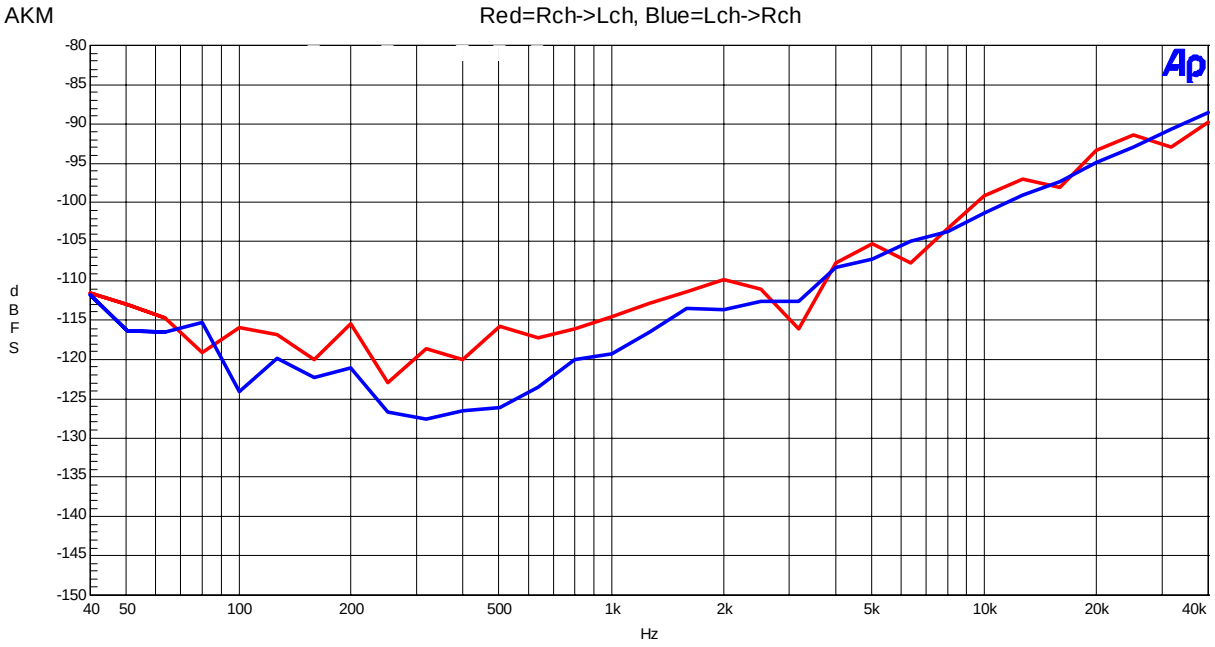


Figure 22 Crosstalk (Upper = Rch, Lower = Lch)

2.DAC

(DAC fs=48kHz)

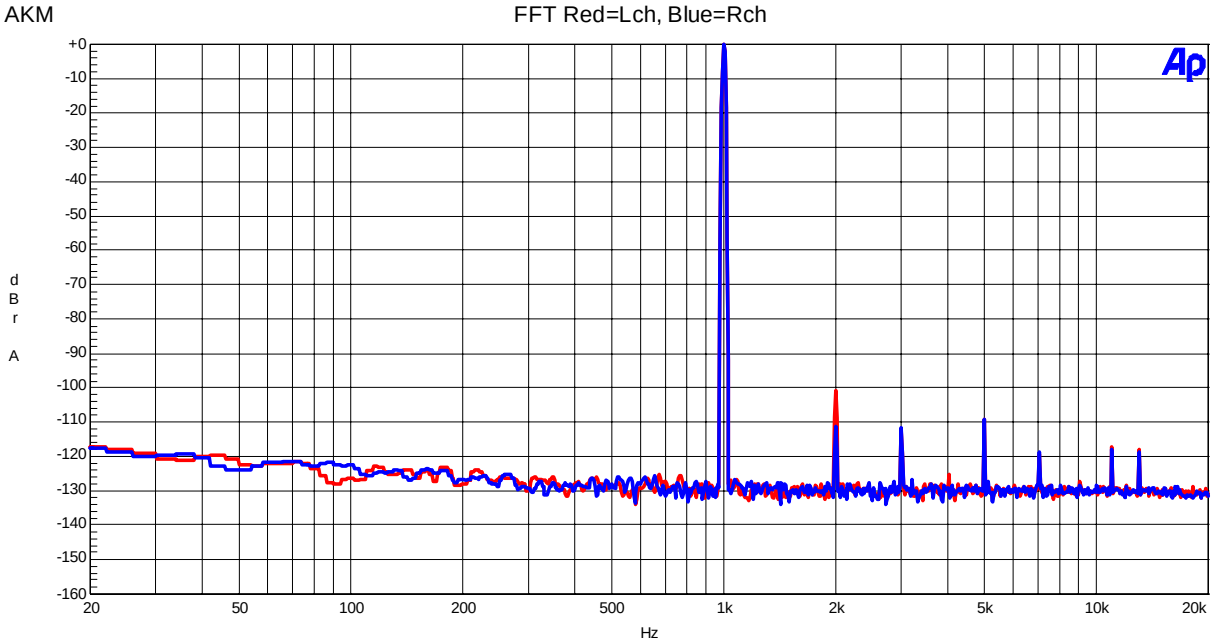


Figure 23 FFT (1kHz, 0dBFS input)

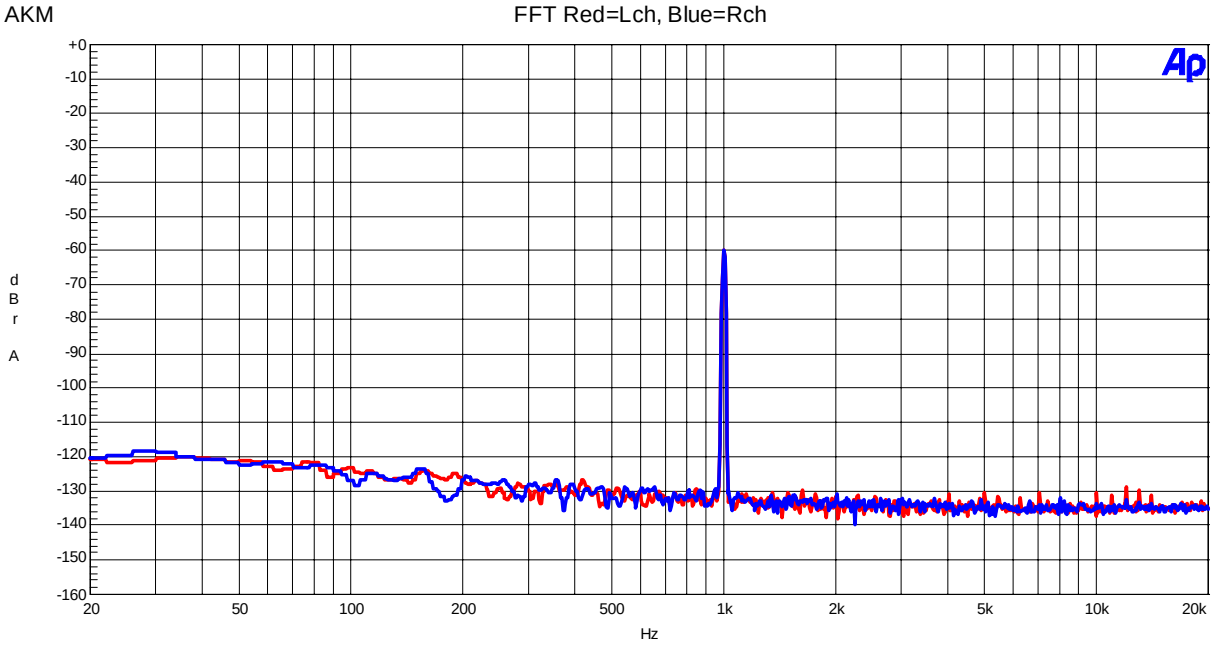


Figure 24 FFT (1kHz, -60dBFS input)

(DAC fs=48kHz)

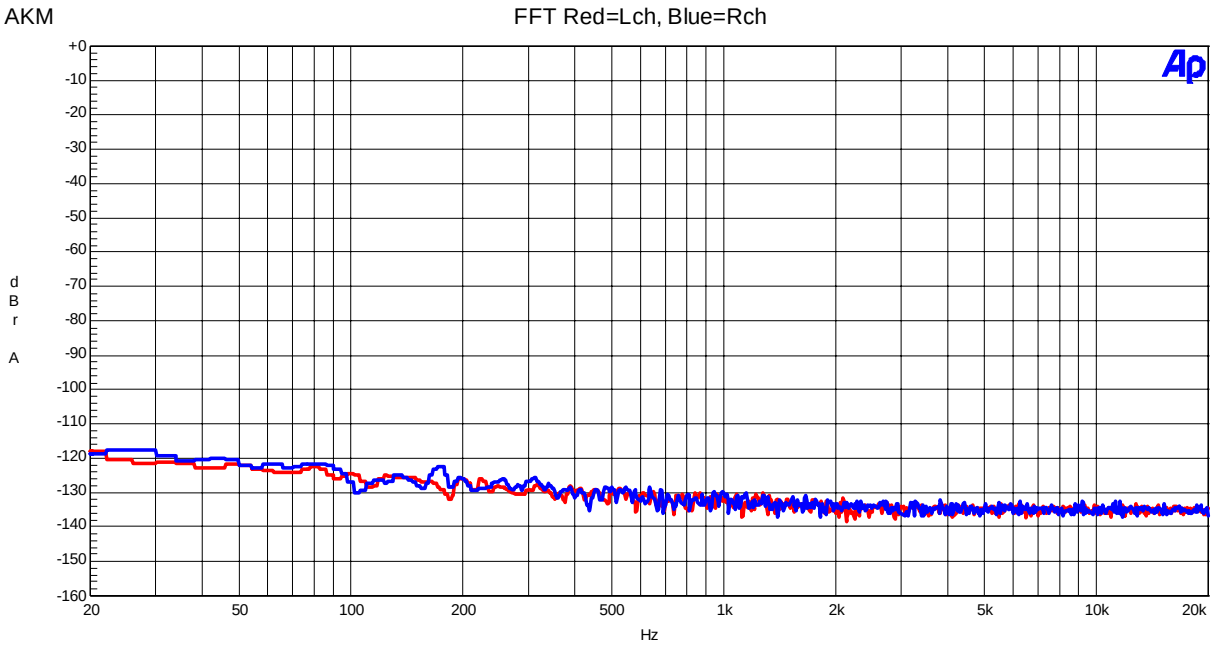


Figure 25 FFT (noise floor)

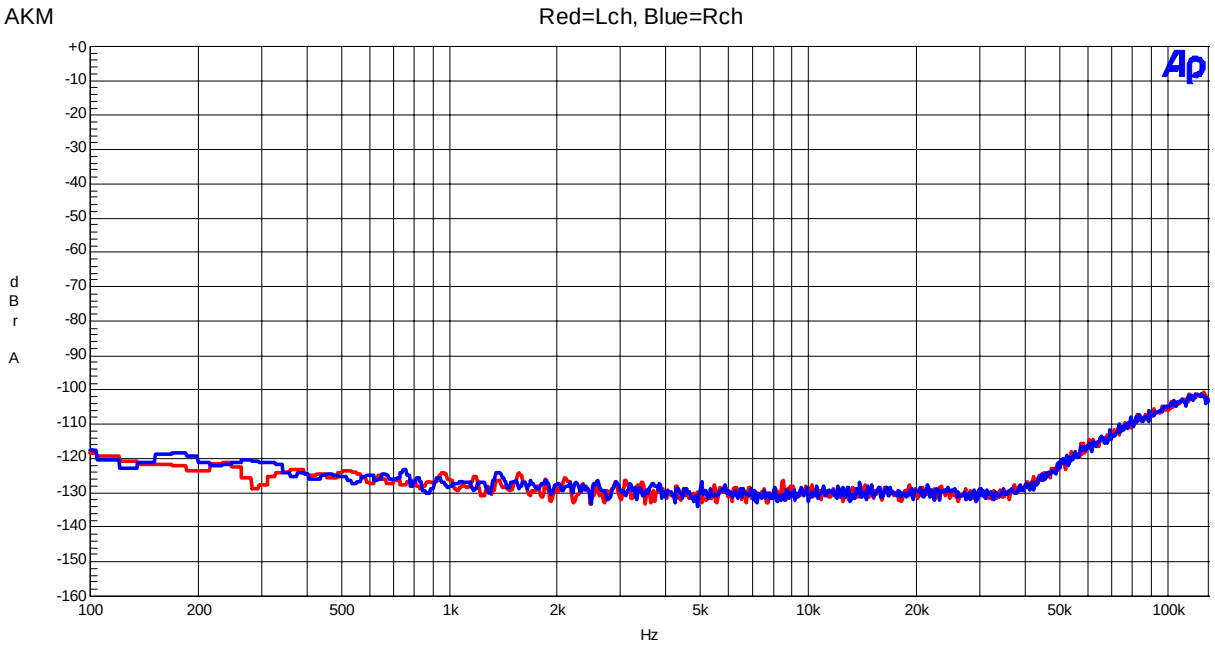


Figure 26 FFT (out-of-band noise)

(DAC fs=48kHz)

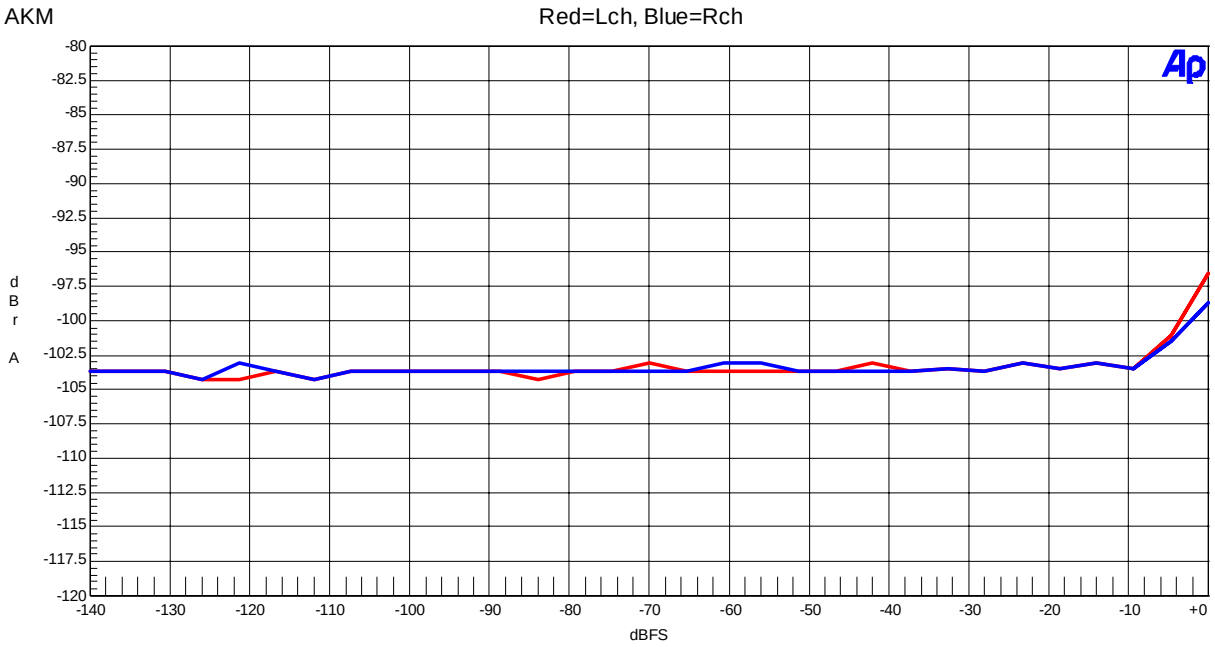


Figure 27 THD+N vs Input Level (fin=1kHz)

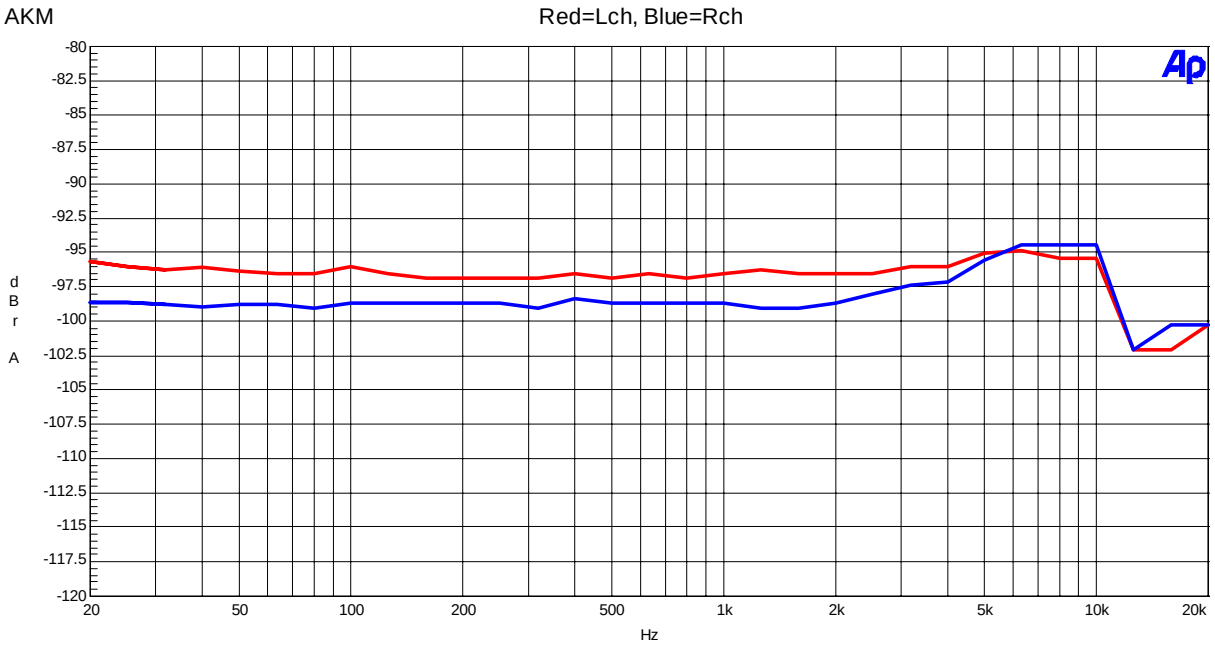


Figure 28 THD+N vs fin (Input level=0dBFS)

(DAC fs=48kHz)

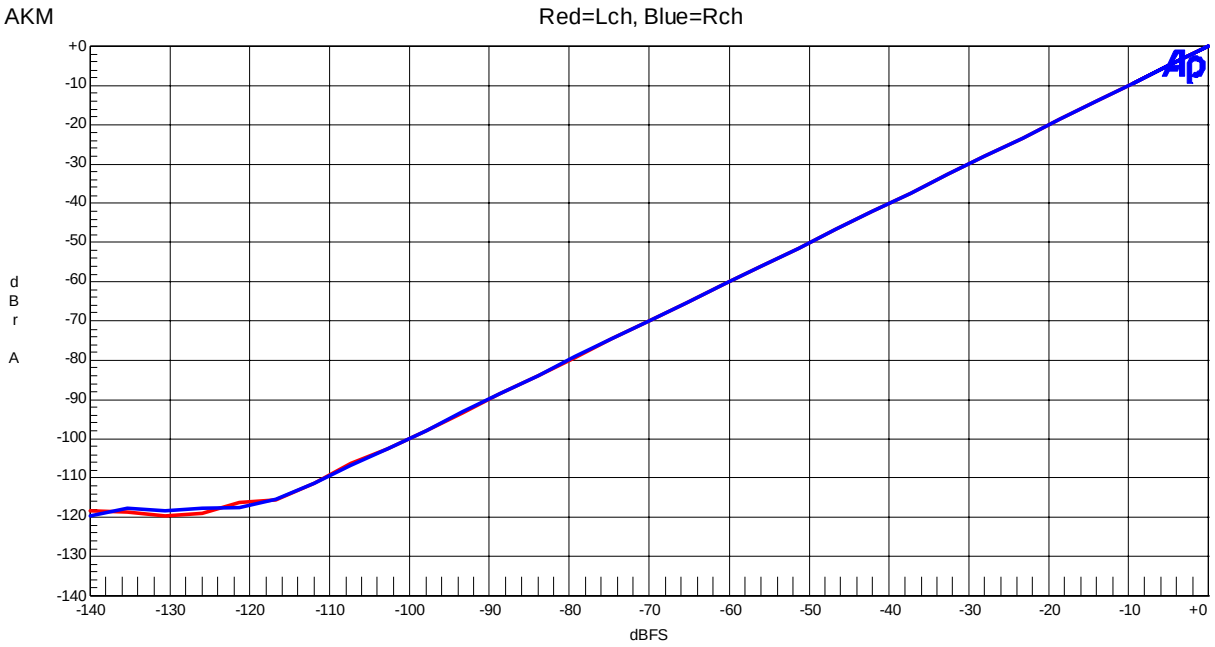


Figure 29 Linearity (fin=1kHz)

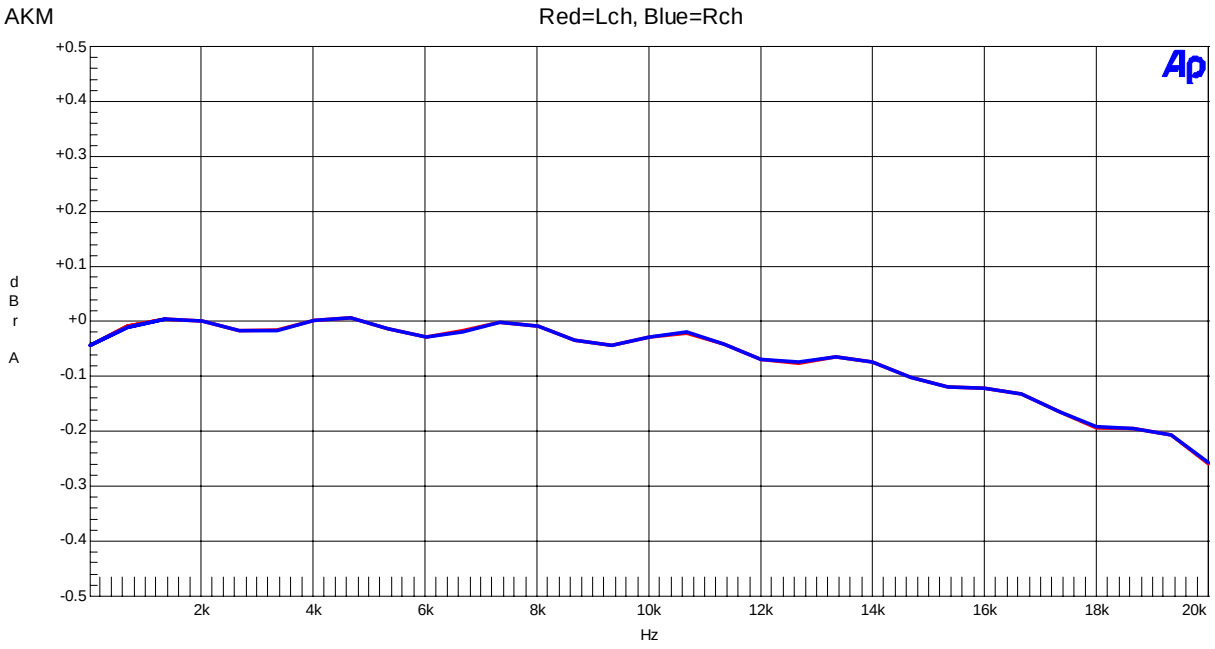


Figure 30 Frequency Response (Input level=0dBFS)

(DAC fs=48kHz)

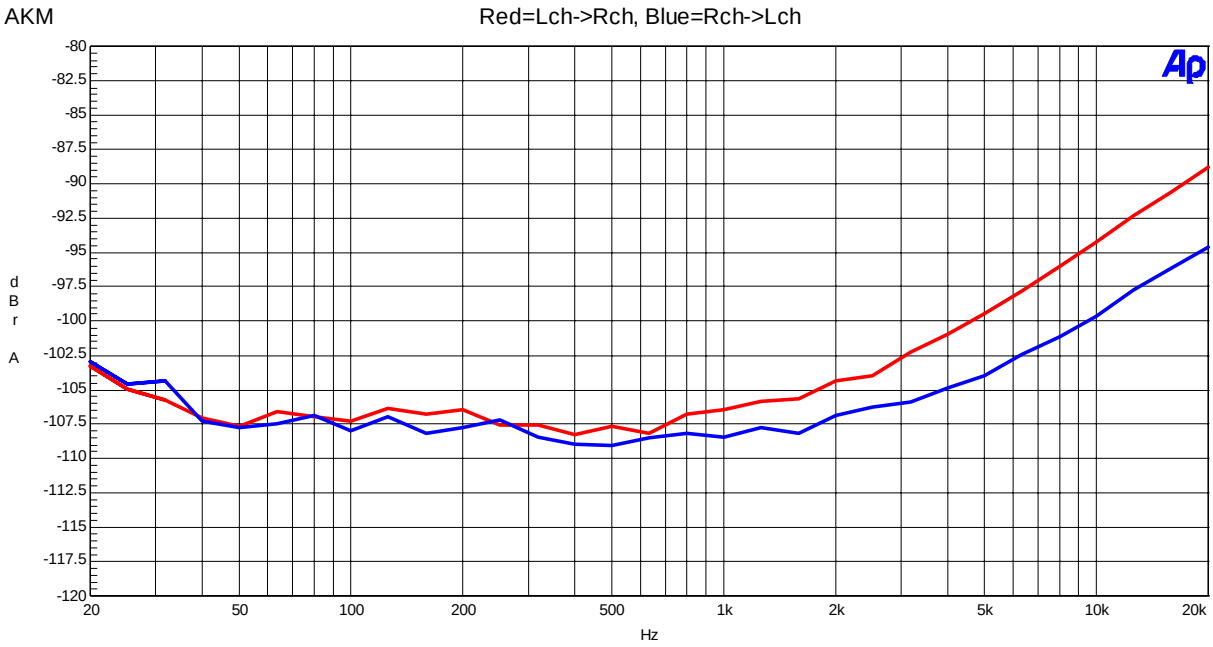


Figure 31 Cross-talk (Input level=0dBFS)

(DAC fs=96kHz)

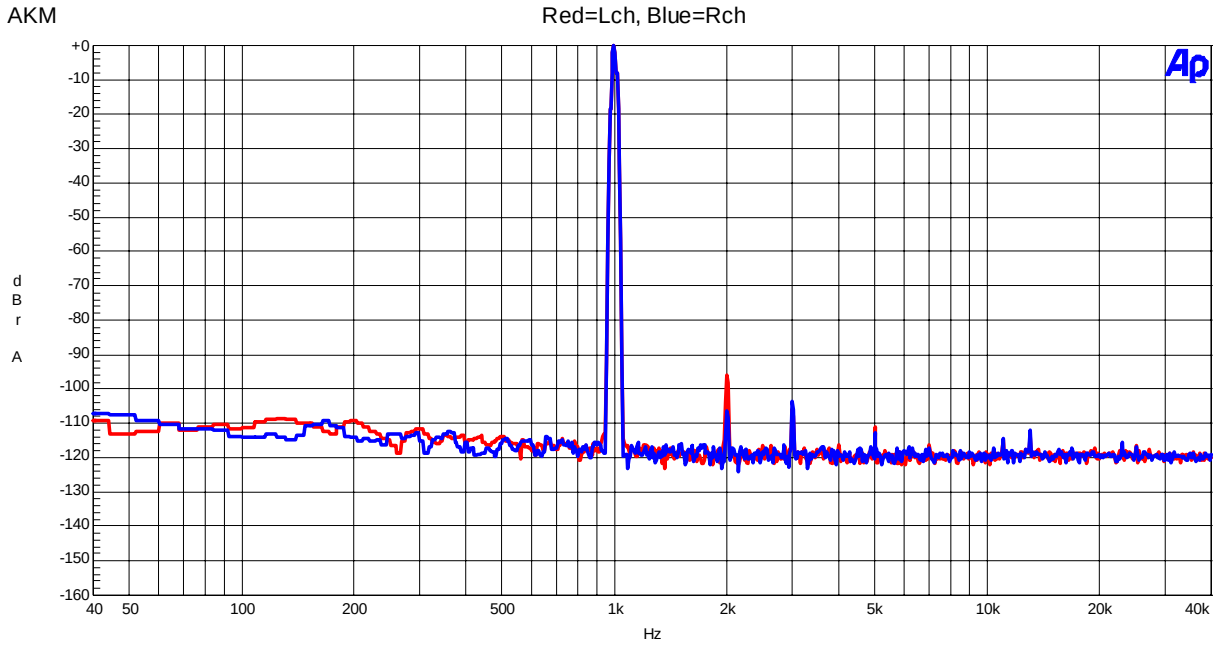


Figure 32 FFT (1kHz, 0dBFS input)

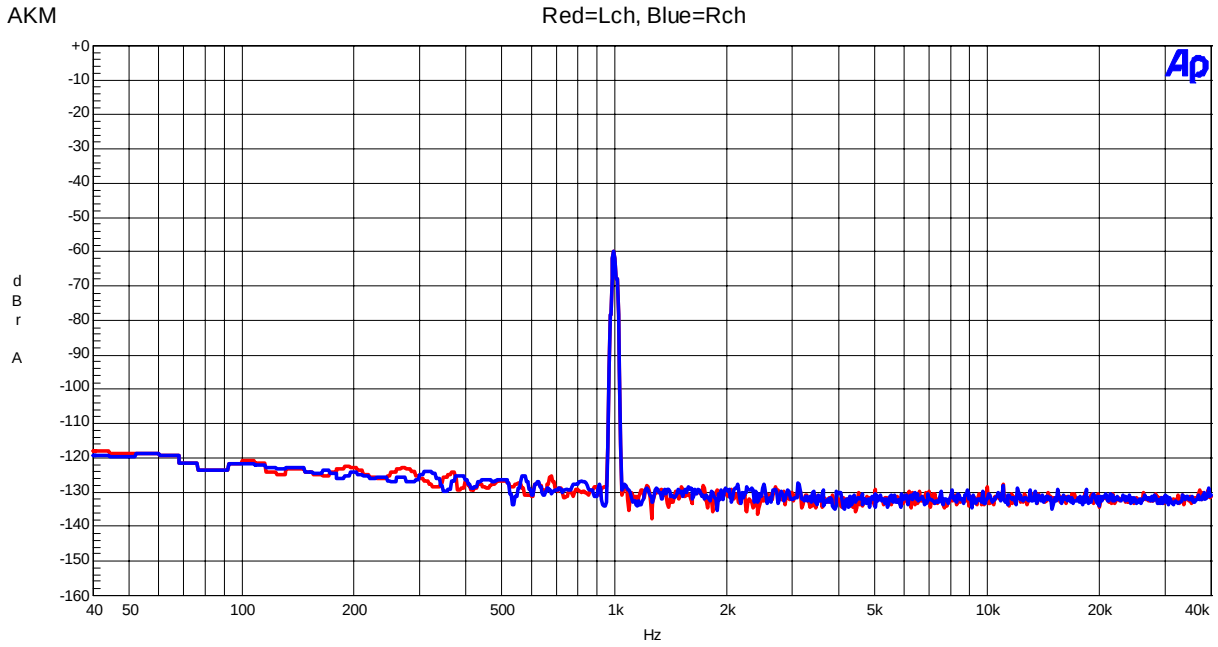


Figure 33 FFT (1kHz, -60dBFS input)

(DAC fs=96kHz)

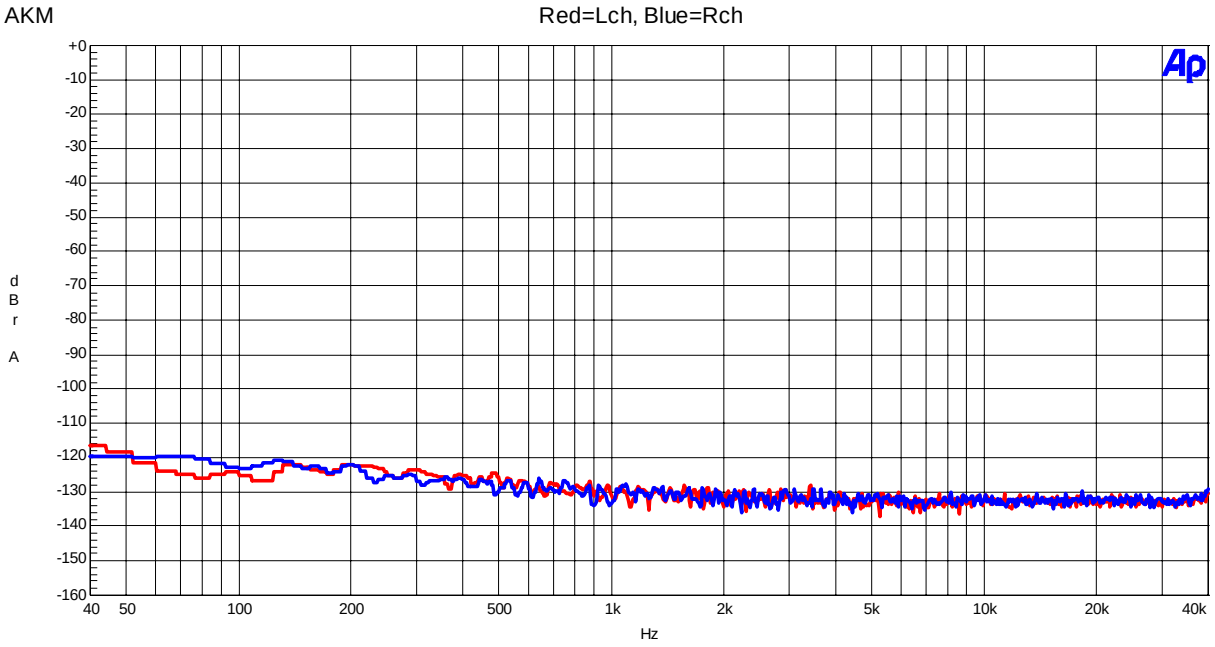


Figure 34 FFT (noise floor)

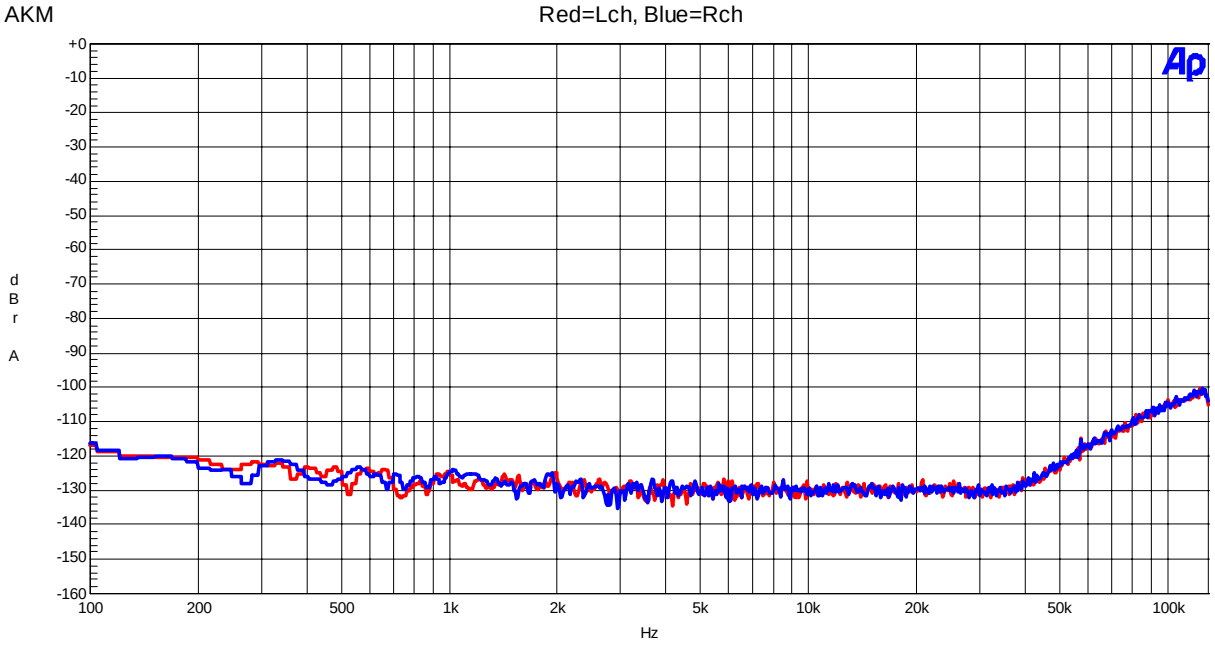


Figure 35 FFT (out band noise)

(DAC fs=96kHz)

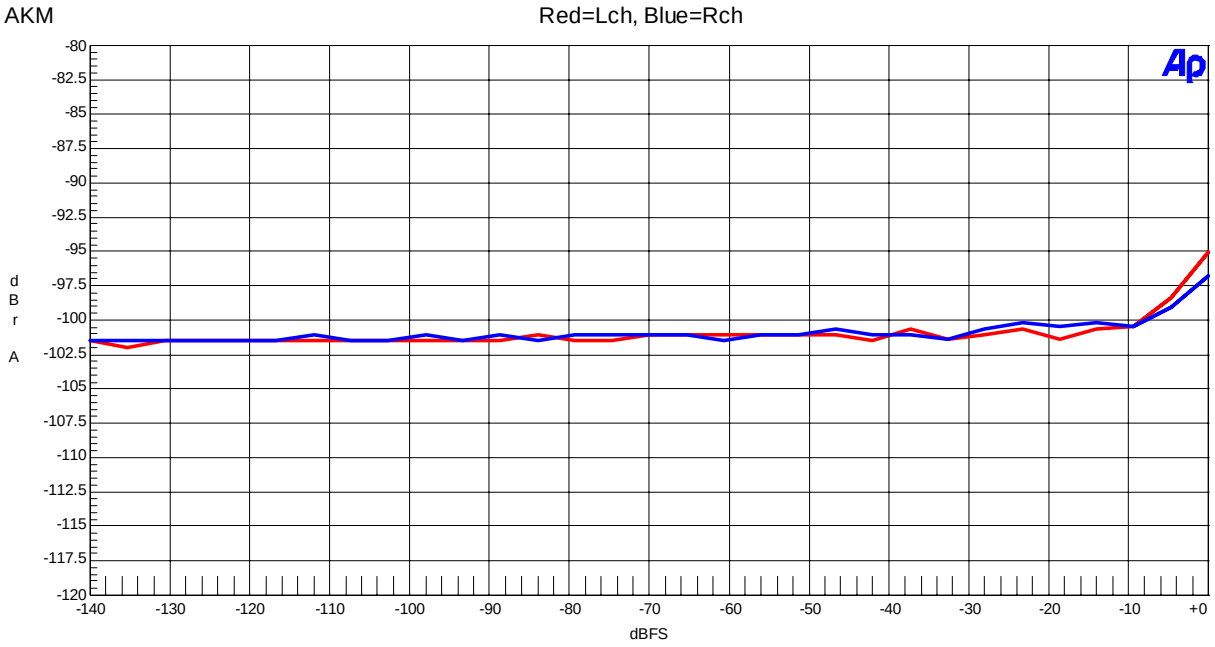


Figure 36 THD+N vs Input Level (fin=1kHz)

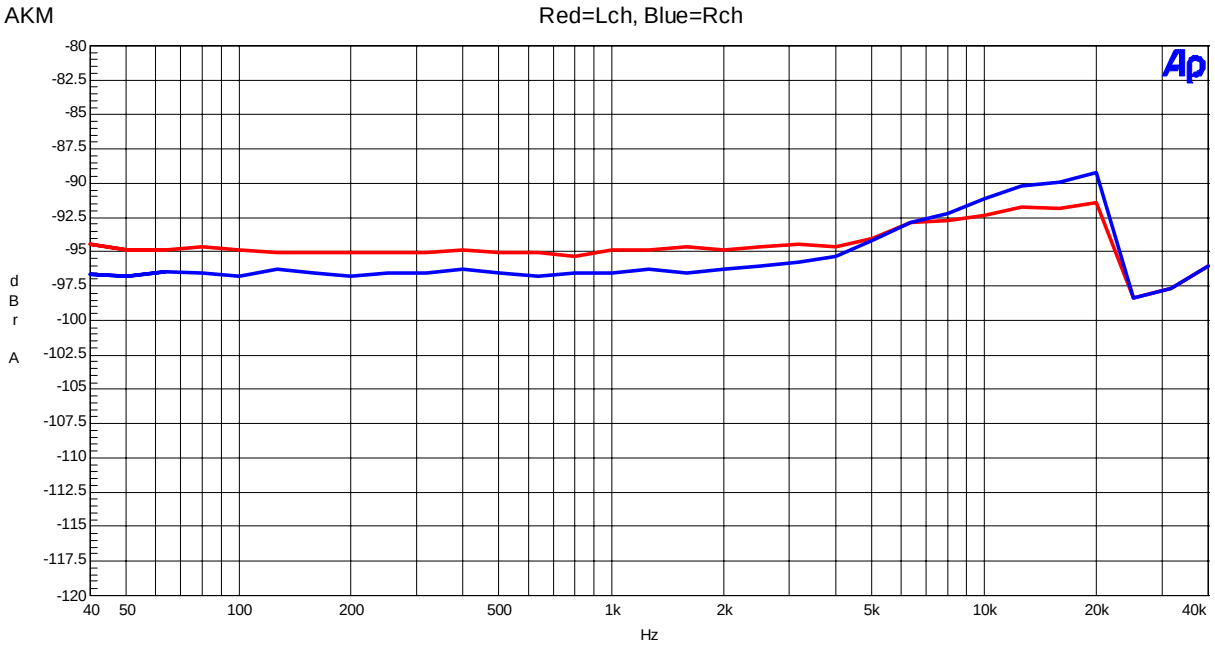


Figure 37 THD+N vs fin (Input level=0dBFS)

(DAC fs=96kHz)

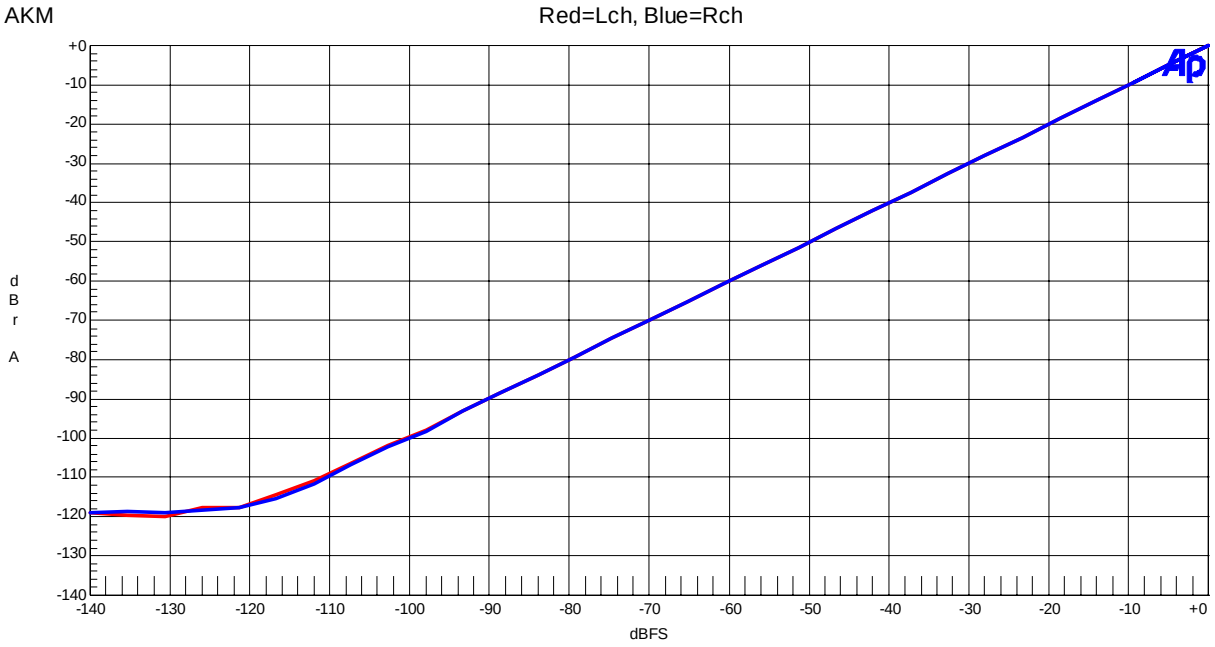


Figure 38 Linearity (fin=1kHz)

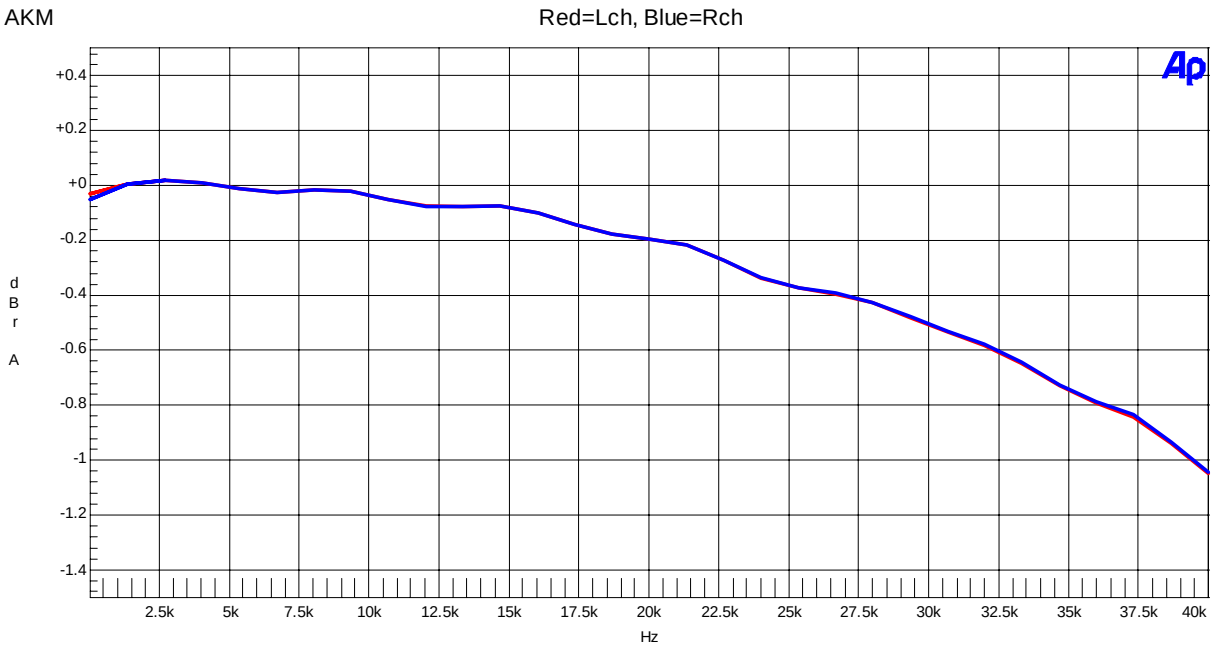


Figure 39 Frequency Response (Input level=0dBFS)

(DAC fs=96kHz)

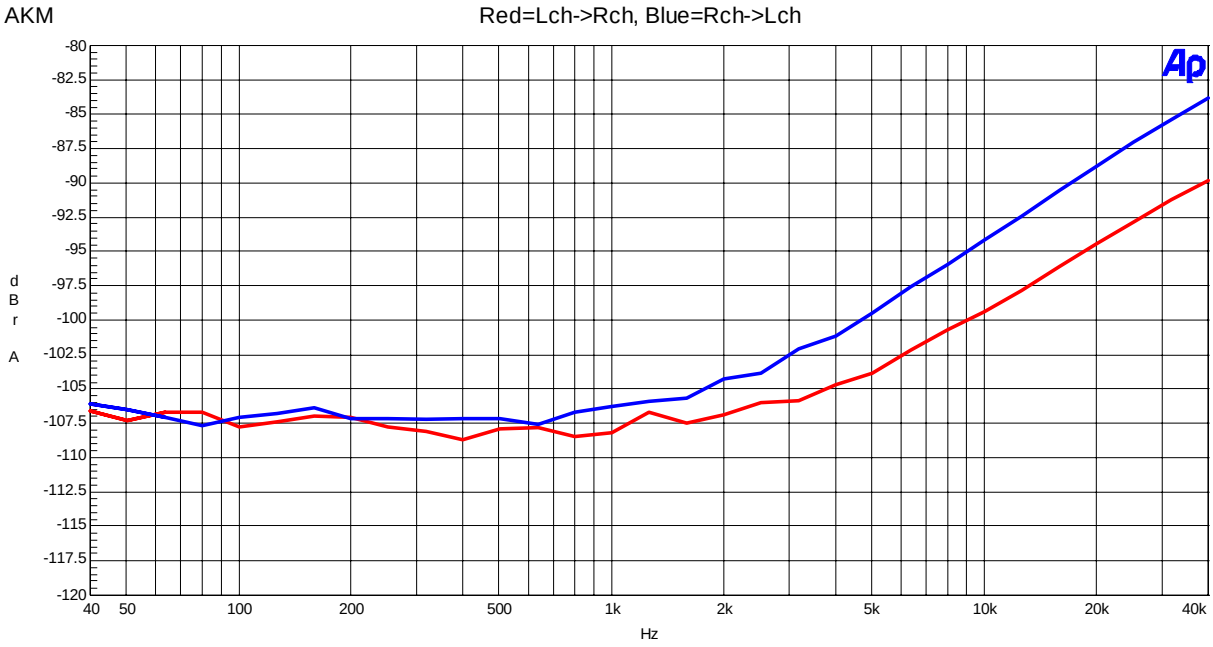


Figure 40 Cross-talk (Input level=0dBFS)

(DAC fs=192kHz)

Red=Lch, Blue=Rch

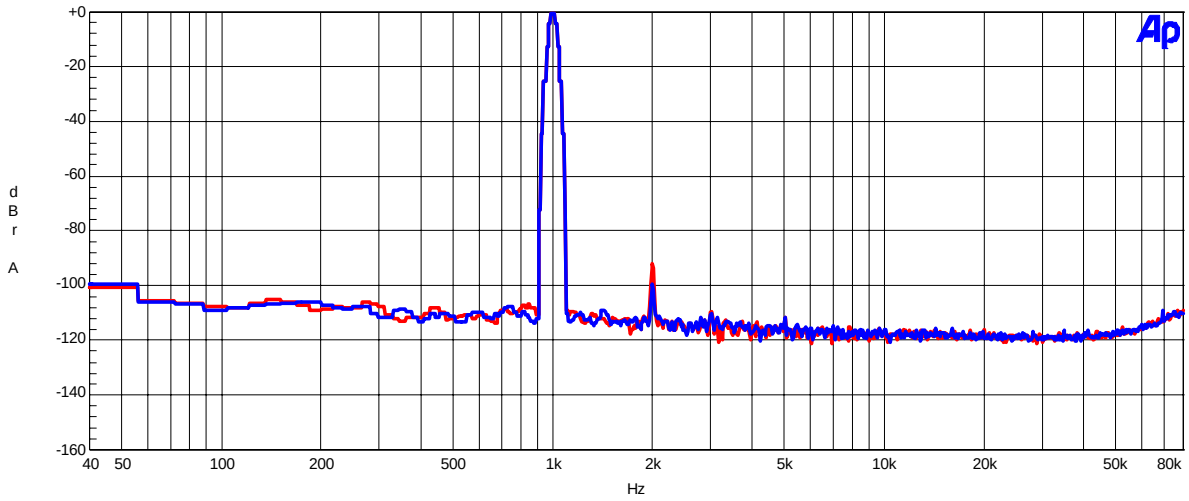


Figure 41 FFT (1kHz, 0dBFS input)

Red=Lch, Blue=Rch

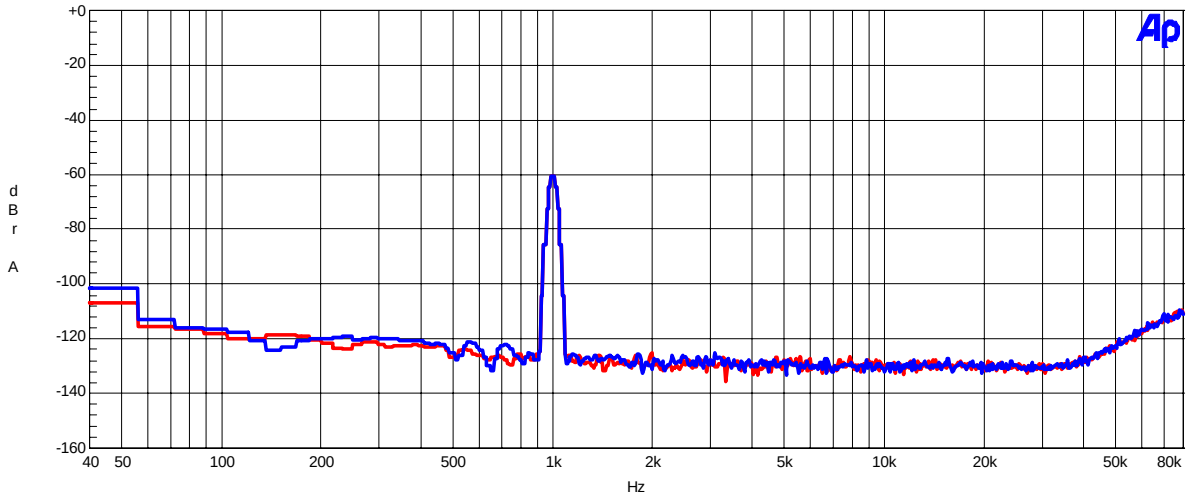


Figure 42 FFT (1kHz, -60dBFS input)

(DAC fs=192kHz)

Red=Lch, Blue=Rch

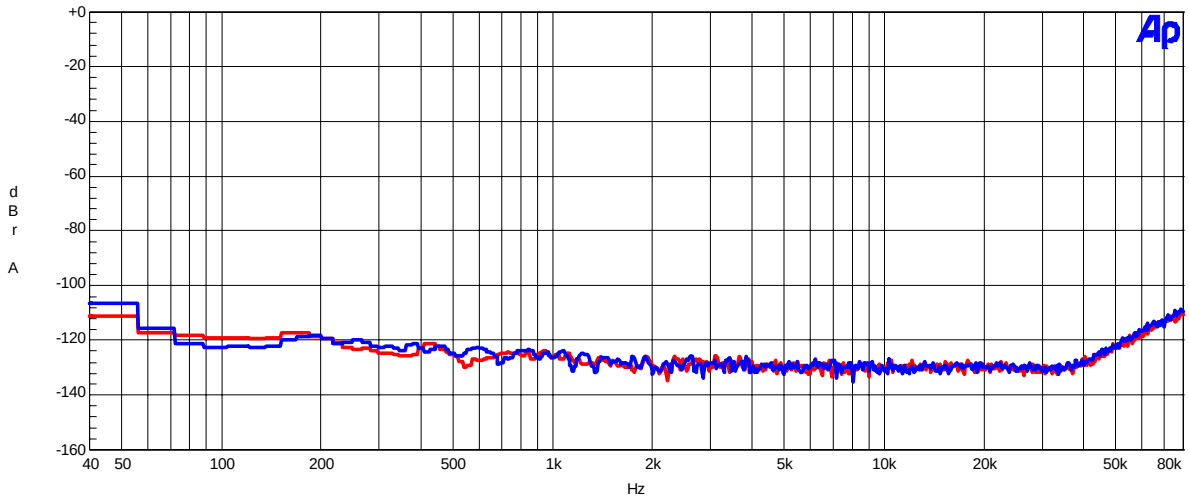


Figure 43 FFT (noise floor)

Red=Lch, Blue=Rch

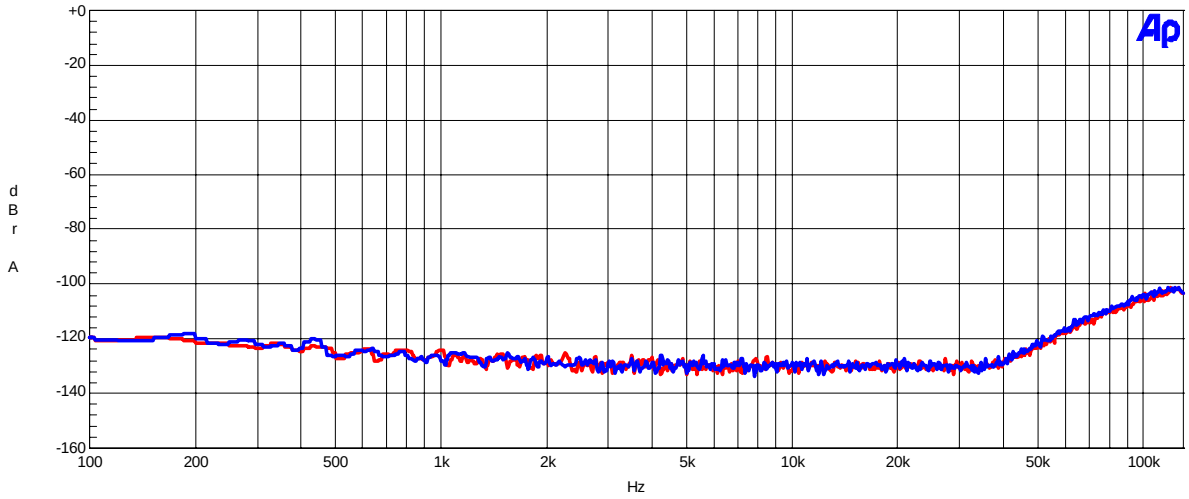


Figure 44 FFT (outband noise)

(DAC fs=192kHz)

Red=Lch, Blue=Rch

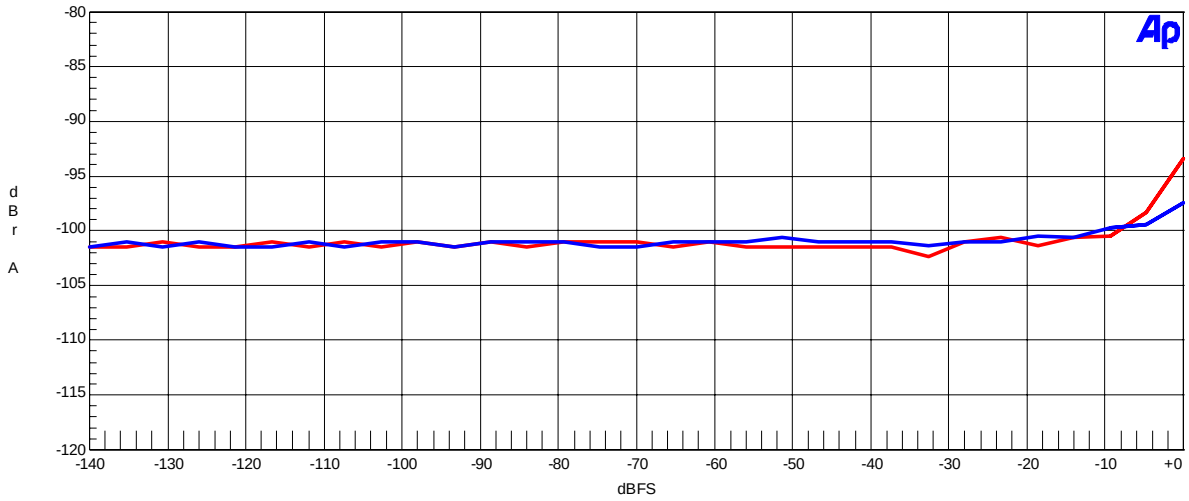


Figure 45 THD+N vs Input Level (fin=1kHz)

Red=Lch, Blue=Rch

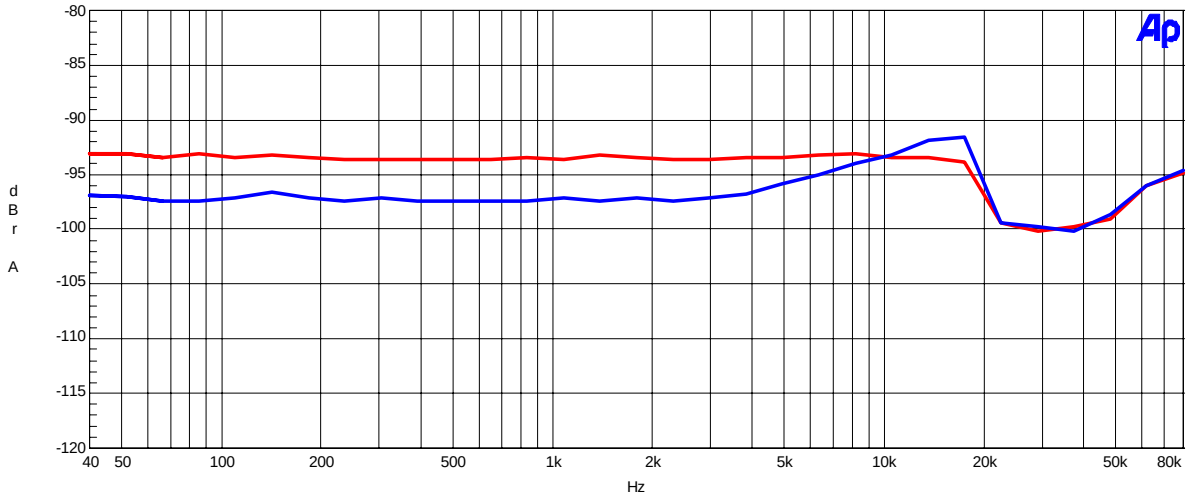


Figure 46 THD+N vs fin (Input level=0dBFS)

(DAC fs=192kHz)

Red=Lch, Blue=Rch

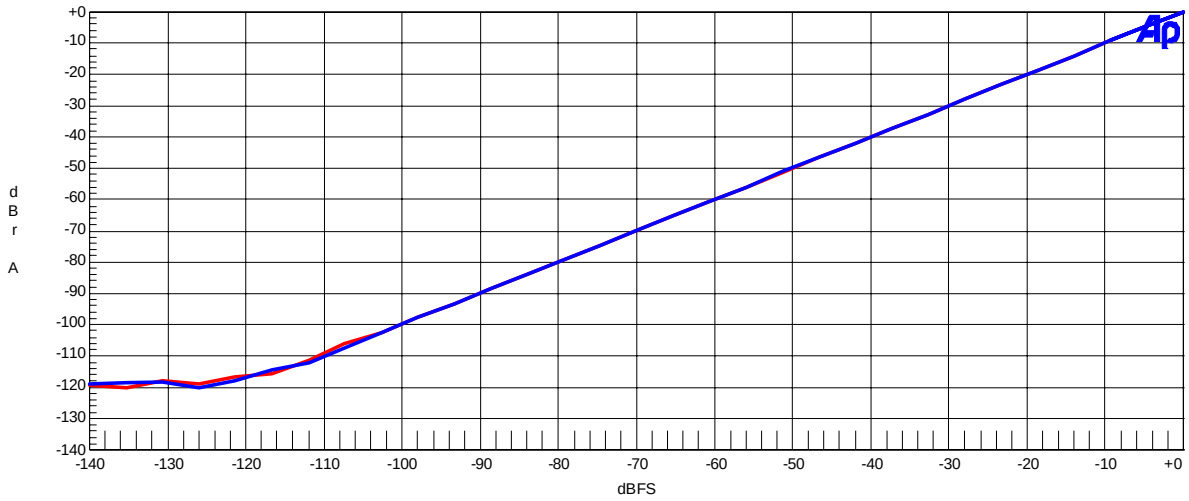


Figure 47 Linearity (fin=1kHz)

Red=Lch, Blue=Rch

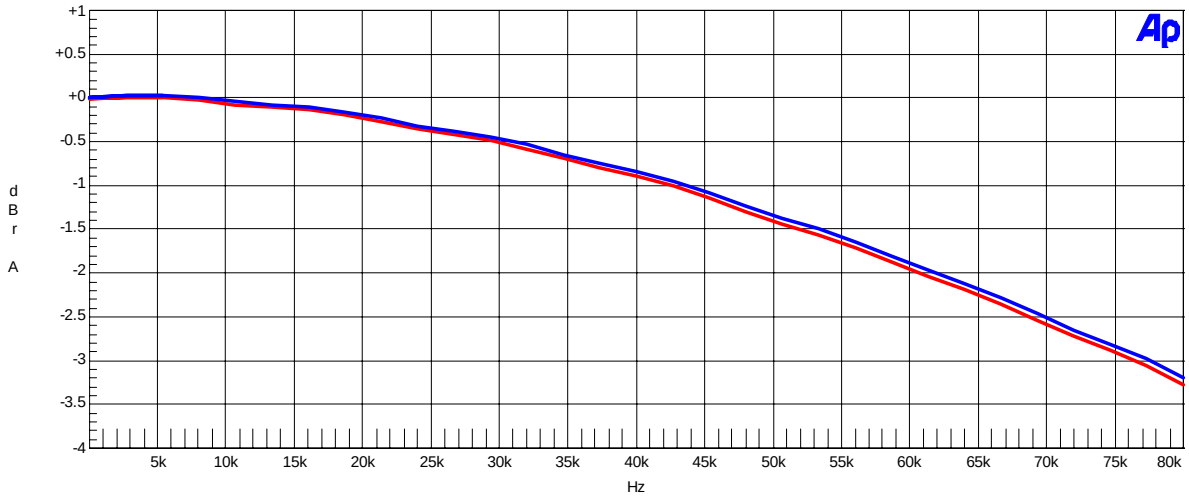


Figure 48 Frequency Response (Input level=0dBFS)

(DAC fs=192kHz)

Red=Rch->Lch, Blue=Lch->Rch

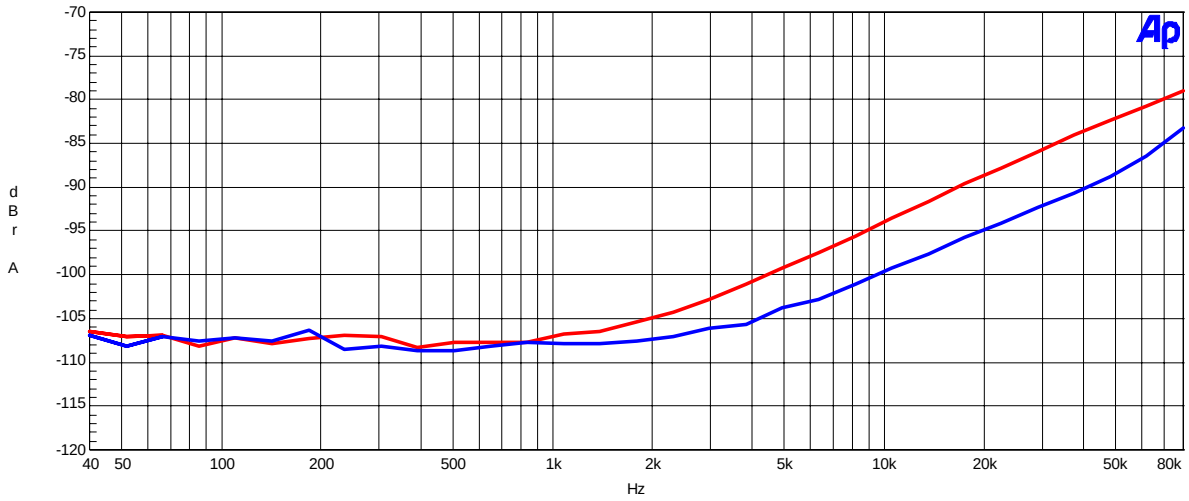
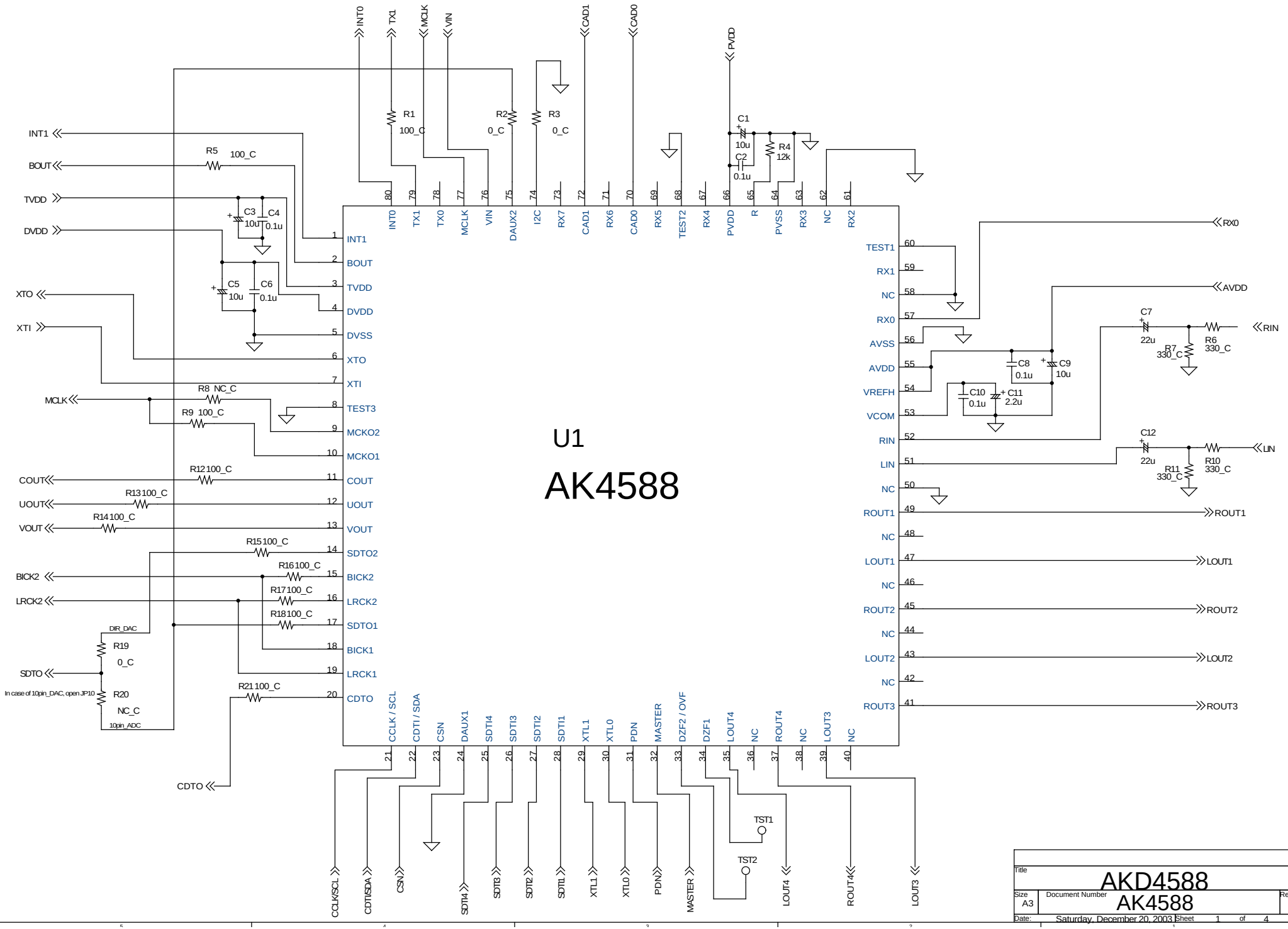
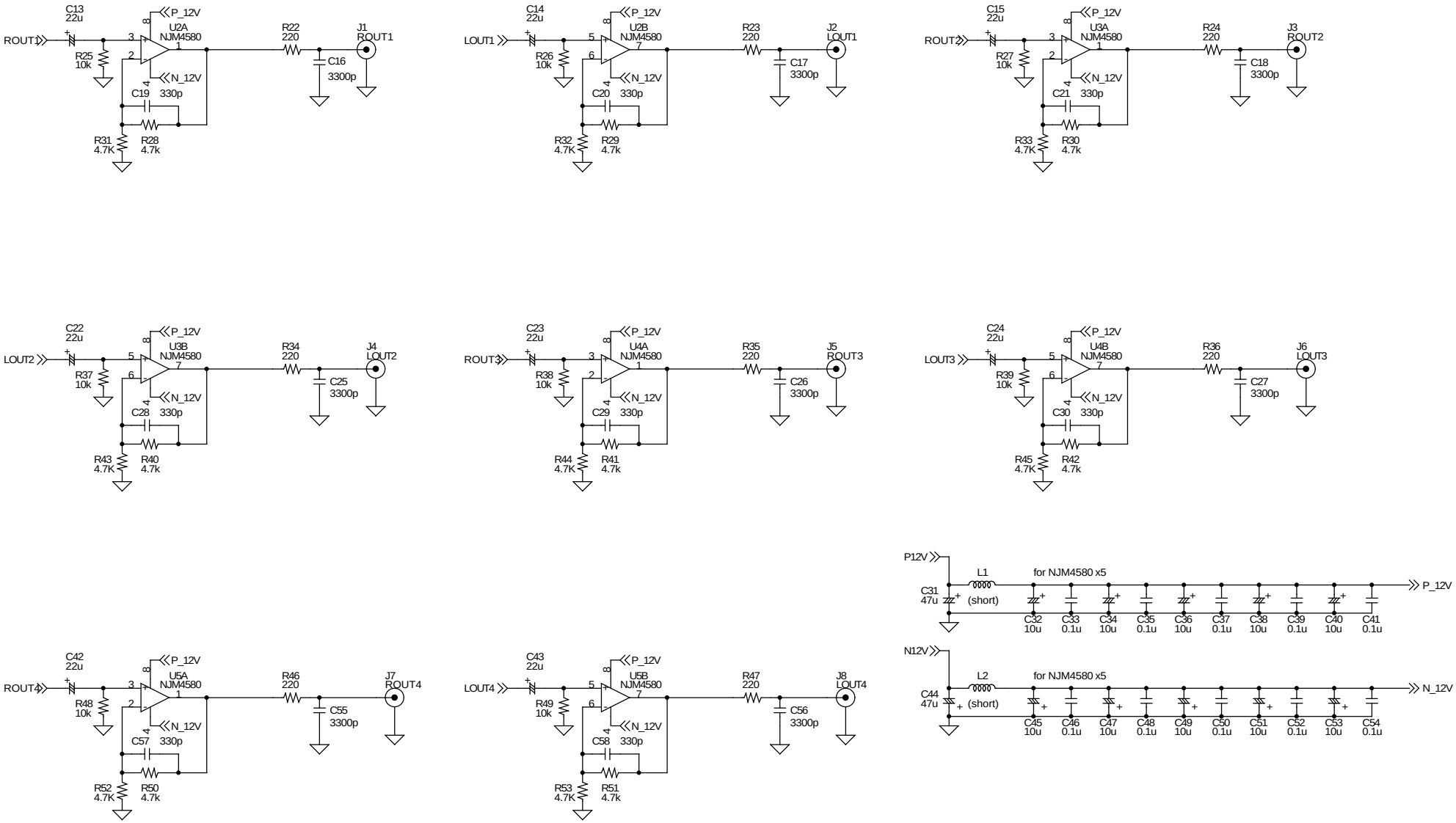


Figure 49 Cross-talk (Input level=0dBFS)

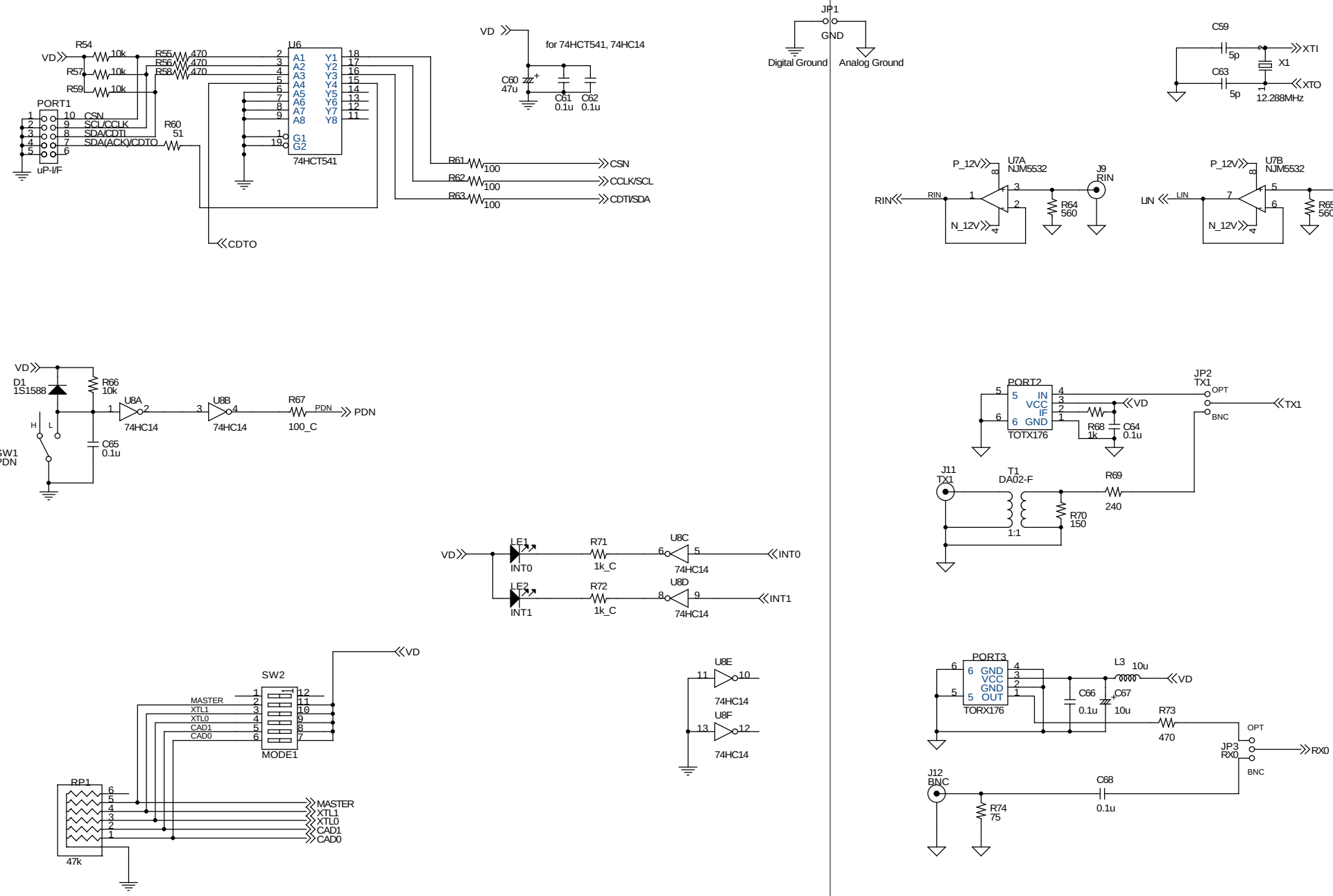
IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.

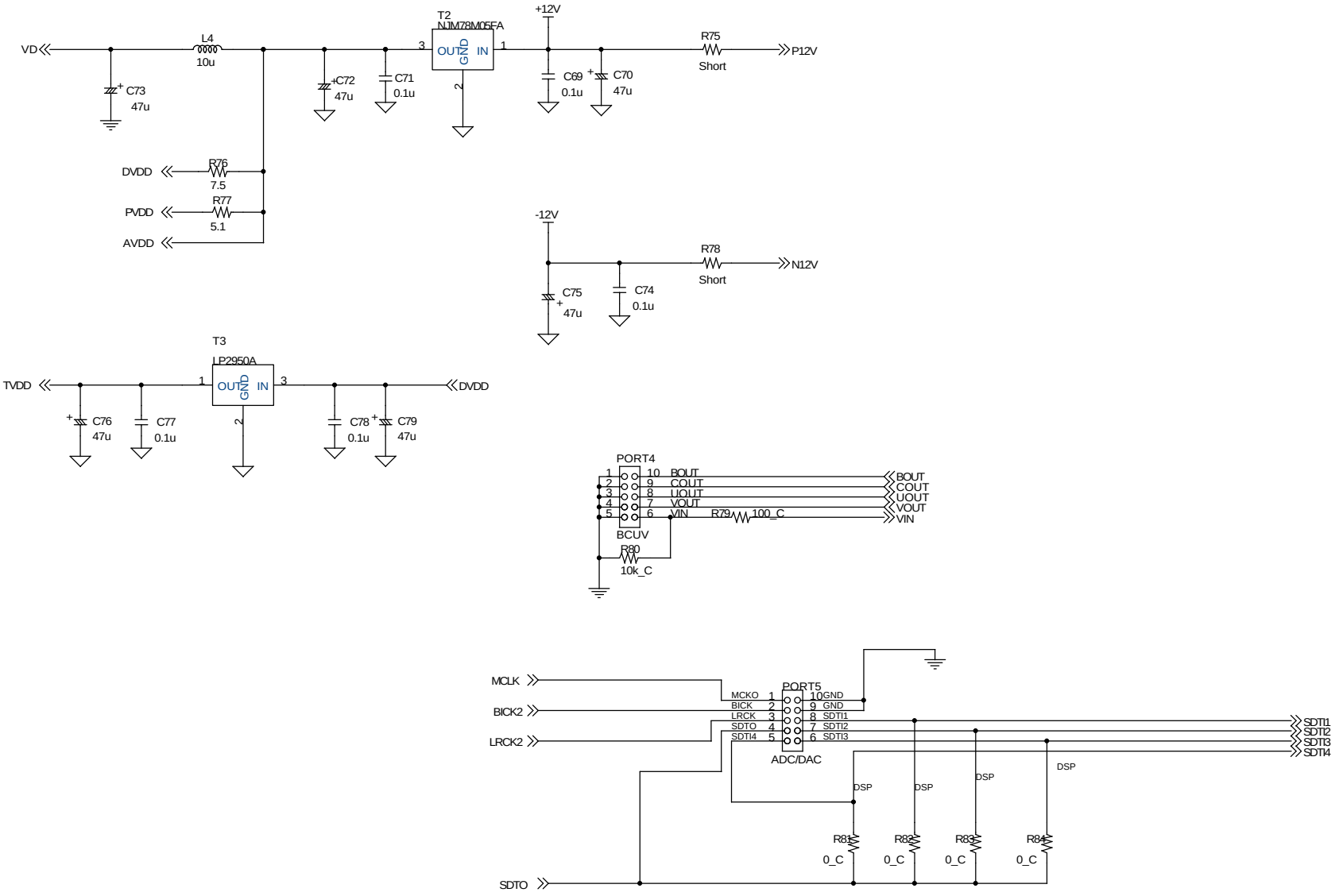

U1
AK4588
INT0
TX1
MCLK
VIN
CAD1
CAD0
PVDD
INT1
BOUT
TVDD
DVDD
XTO
XTI
MCLK
COUT
UOUT
VOUT
BICK2
LRCK2
SDTO
CDTO
CCLK/SCL
CDTI/SDA
CSN
SDTI4
SDTI3
SDTI2
SDTI1
XTL1
XTL0
PDN
MASTER
TST1
TST2
LOUT4
ROUT4
LOUT3
RX0
AVDD
RIN
LIN
ROUT1
LOUT1
ROUT2
LOUT2
ROUT3
R1 100_C
R2 0_C
R3 0_C
R4 12k
R5 100_C
C1 10u
C2 0.1u
C3 10u
C4 0.1u
C5 10u
C6 0.1u
C7 22u
C8 0.1u
C9 10u
C10 0.1u
C11 2.2u
C12 22u
R6 330_C
R7 330_C
R8 NC_C
R9 100_C
R10 330_C
R11 330_C
R12 100_C
R13 100_C
R14 100_C
R15 100_C
R16 100_C
R17 100_C
R18 100_C
R19 0_C
R20 NC_C
R21 100_C
DIR_DAC
In case of 10pin_DAC, open JP10
10pin_ADC
AKD4588
AK4588
A3
B
Saturday, December 20, 2003
1 of 4



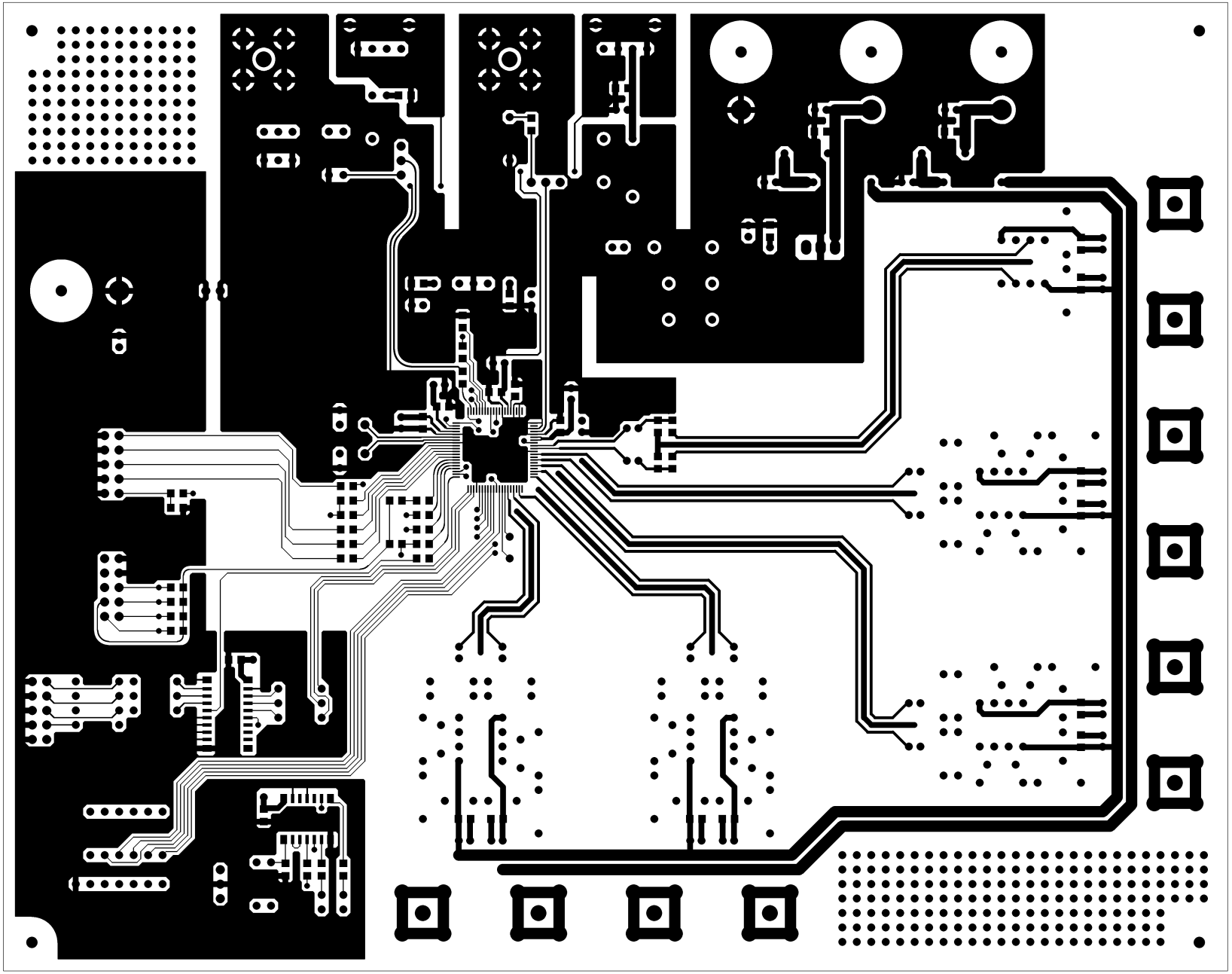
Title	AKD4588	
Size A3	Document Number AOUT	Rev B
Date: Saturday, December 20, 2003	Sheet 2 of 4	



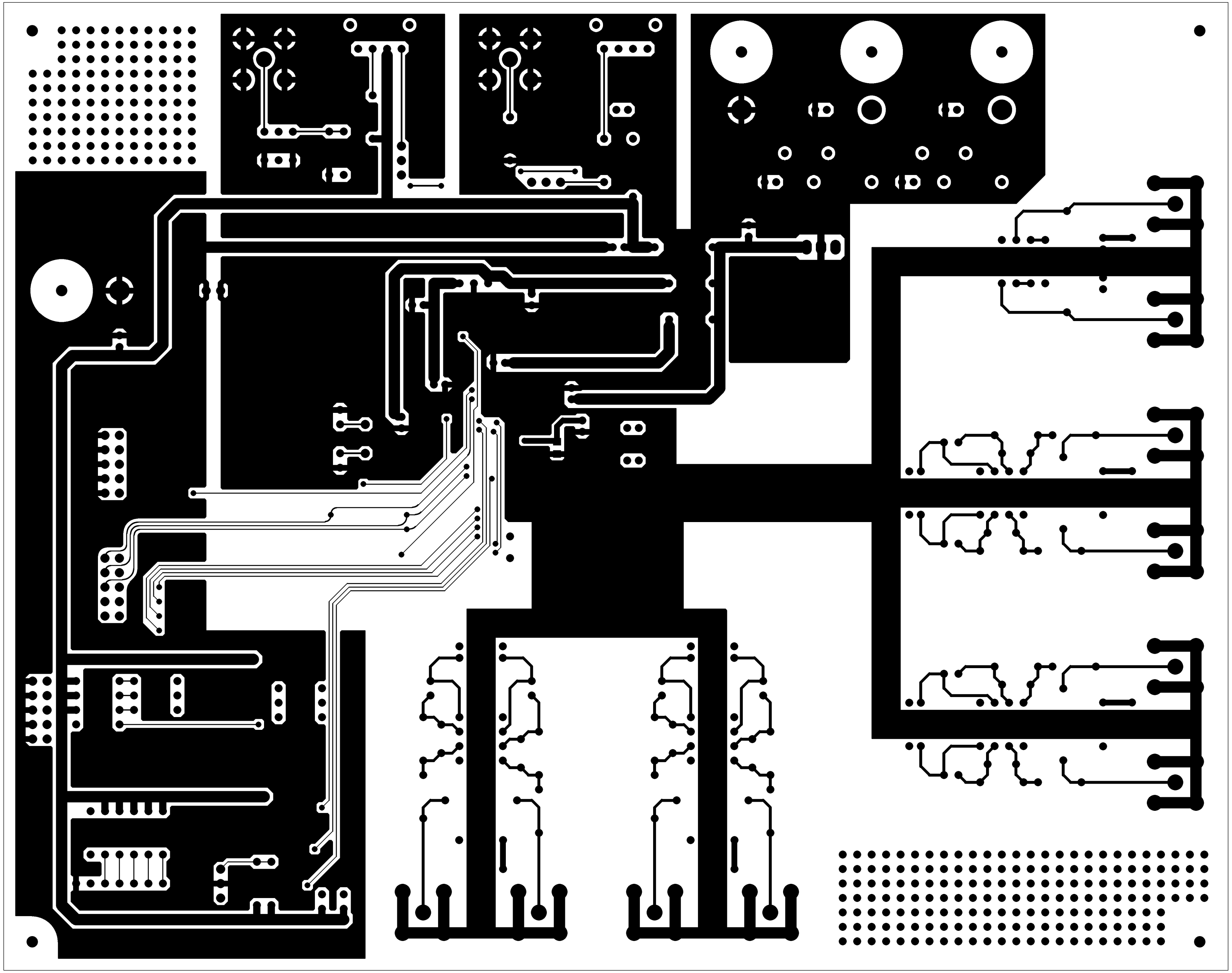
Title	AKD4588	
Size A3	Document Number INPUT	Rev B
Date: Saturday, December 20, 2003	Sheet 3 of 4	



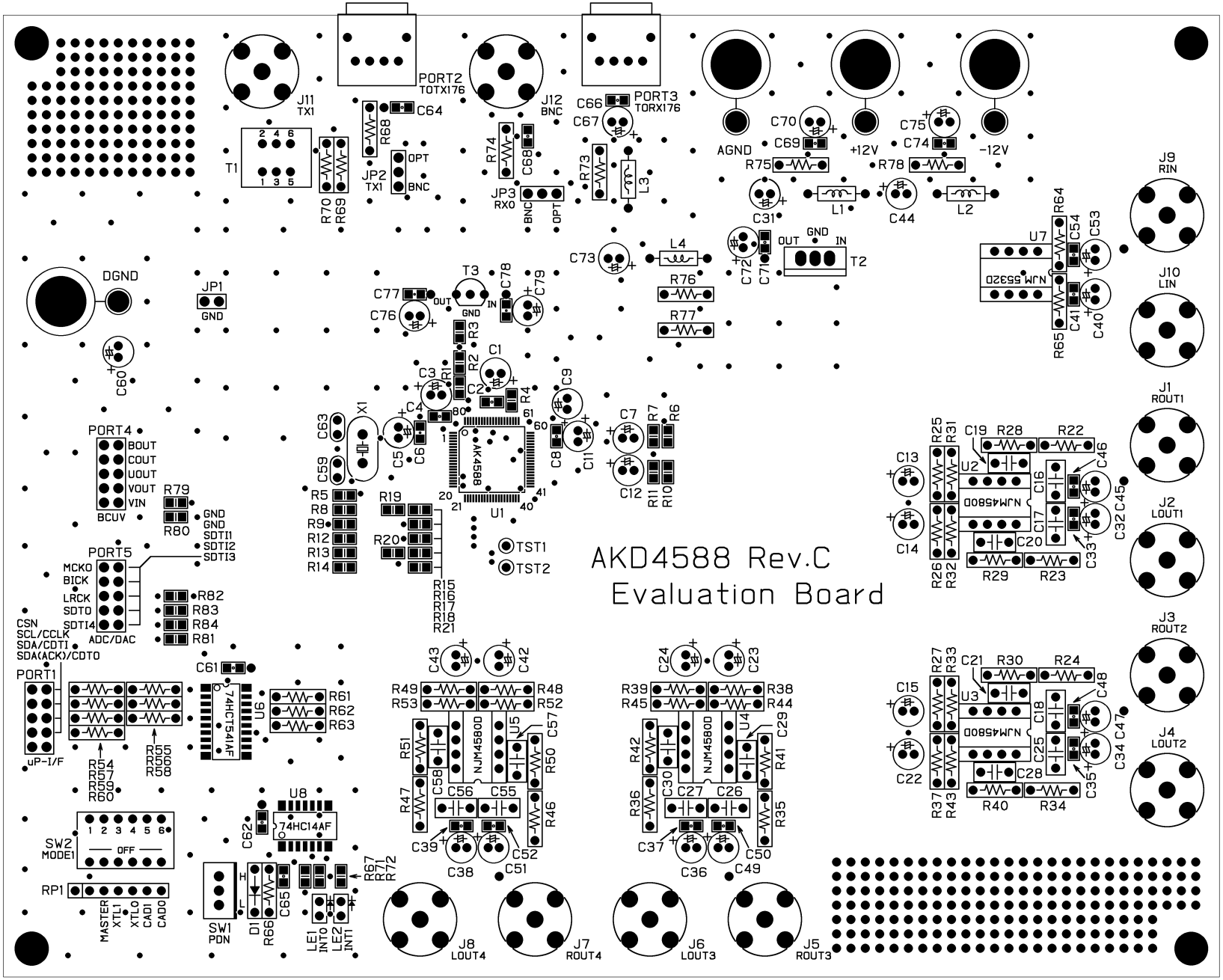
Title	AKD4588	
Size A3	Document Number Power Supply	Rev A
Date: Saturday, December 20, 2003	Sheet 4 of 4	



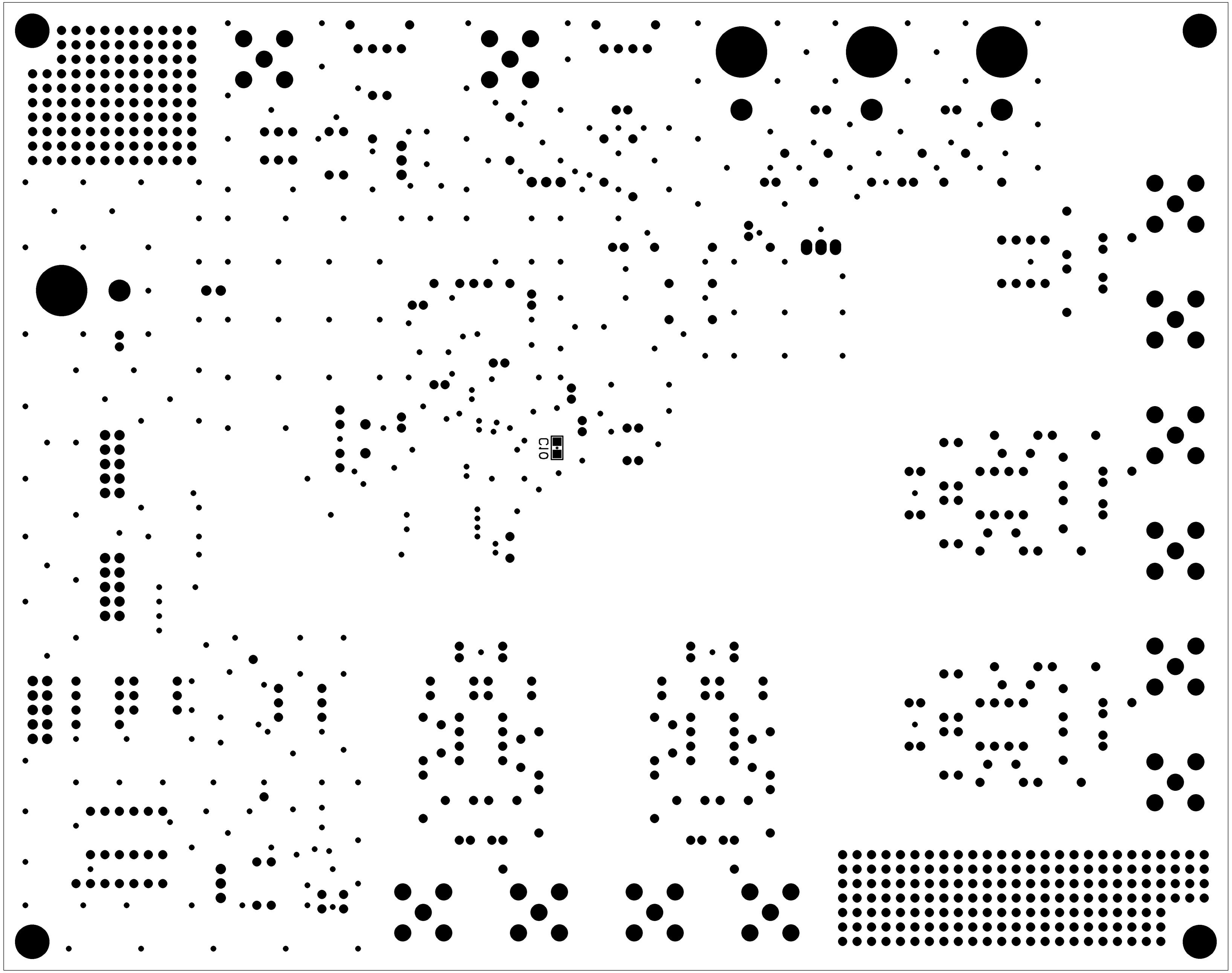
AKD4588 Rev.C L1



AKD4588 Rev.C L2



AKD4588 Rev.C L1 SR SILK



AKD4588 Rev.C L2 SR SILK