



**Video Enhancement
Processor
AL260 Data Sheets**

Amendments

- 99.10.04 Preliminary version
- 02.12.19 Preliminary version A0.1:
(1) Updated from Preliminary version
- 03.05.16 Version B1.0:
(1) Updated from Preliminary version A0.2
(2) Add Register Description

THE INFORMATION CONTAINED HEREIN IS SUBJECT TO CHANGE WITHOUT NOTICE.

Contents:

| | |
|---|-----------|
| 1. General Description | 5 |
| 2. Function Block Diagram | 6 |
| 3. Features | 6 |
| 3.1 General Features | 6 |
| 3.2 Feature Description: | 7 |
| 4 Applications | 8 |
| 5 Application Example | 9 |
| 6 Pin-Out Diagram | 10 |
| 7 Pin Definition and Description | 11 |
| 7.1 Input Format Table of AL260:..... | 11 |
| 8 General Function Description | 15 |
| 8.1 Function Blocks | 15 |
| 8.2 VIU (Video Input Unit)..... | 15 |
| 8.2.1 Input Data Format | 15 |
| 8.2.2 Video Capture and Down Scale Engine | 16 |
| 8.2.3 Automatic Positioning Registers..... | 17 |
| 8.2.4 PLL Programming for Memory and Display Clock..... | 17 |
| 8.3 MIU (Memory Interface Unit)..... | 17 |
| 8.3.1 DRAM Bandwidth Consideration | 17 |
| 8.3.2 DRAM Input/Output Windows | 18 |
| 8.3 VPU (Video Processing Unit)..... | 18 |
| 8.4.1 Video De-Interlaced with Film Detection and Motion Adaptive..... | 19 |
| 8.4.2 Up Scale Engine..... | 19 |
| 8.4.3 Keystone Up Scale Engine..... | 20 |
| 8.4 VOU (Video Output Unit)..... | 20 |

| | | |
|-------|---|----|
| 8.5.1 | <i>OSD</i> | 22 |
| 8.5.2 | <i>LUT (Look up table for Gamma Correction and Color Enhancement)</i> | 22 |
| 8.5.3 | <i>Dithering</i> | 23 |
| 8.5 | <i>BIU (Bus Interface Unit)</i> | 23 |
| 9 | <i>Register Definition</i> | 24 |
| 9.1 | <i>Register Set</i> | 24 |
| 9.2 | <i>Register Description</i> | 32 |
| 10 | <i>Electrical Characteristics</i> | 76 |
| 10.1 | <i>Absolute Maximum Ratings</i> | 76 |
| 10.2 | <i>Recommended Operating Conditions</i> | 76 |
| 10.3 | <i>DC Characteristics</i> | 76 |
| 10.4 | <i>AC Characteristics</i> | 77 |
| 11 | <i>Timing Diagrams</i> | 78 |
| 12 | <i>Mechanical Drawing- PQFP-208</i> | 79 |

1. General Description

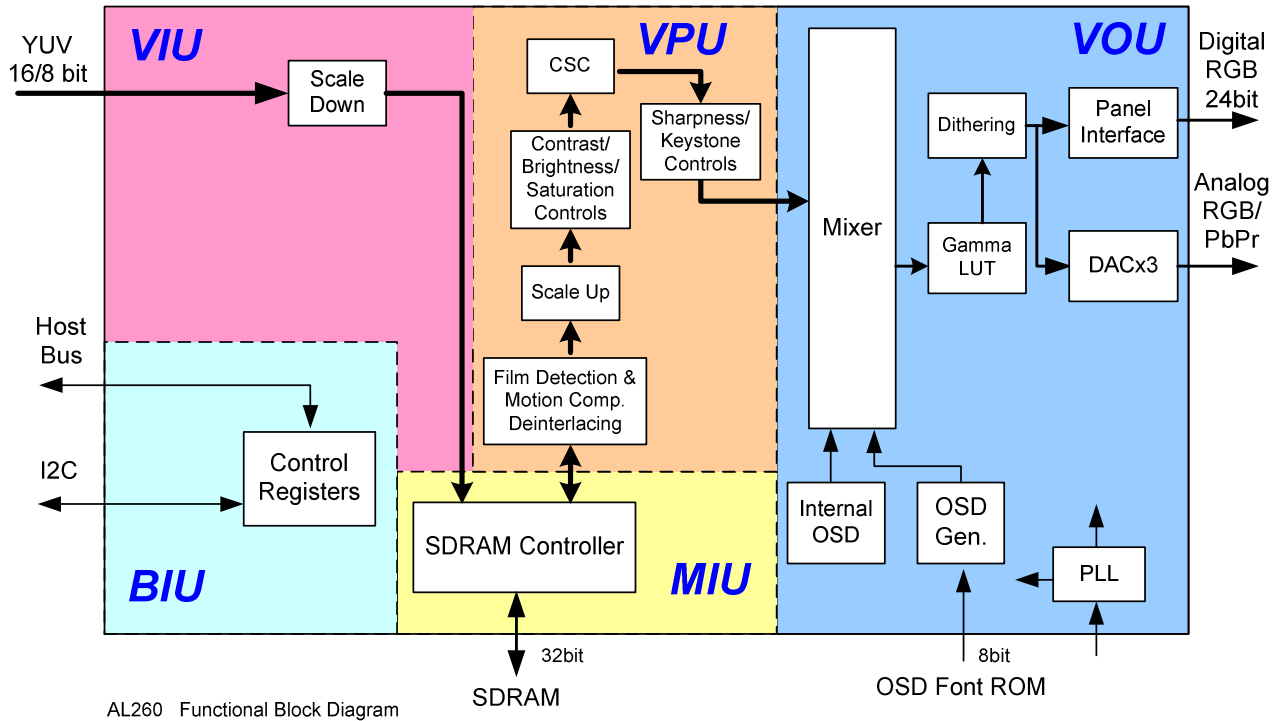
AL260 is a highly integration Video Enhancement Processor which supports video input with multiple video formats then output with De-interlacing and Scaling effects. It can be used for most video conversion and processing applications.

AL260 is equipped with a high quality scaling engine that automatically maintains full screen output display, regardless of the resolution of the incoming signals. Applying AverLogic's proprietary scaling algorithm, the primary input video can be scaled up and scaled down independently in horizontal & vertical directions. It also provides film detection, advanced de-interlacing, filtering, and scaling which's able to convert and process the interlaced video to be displayed on progressive panels.

The On Screen Display (OSD) window provides overlay of a control menu, text, or caption on the output display. It's built-in OSD generator with 2K Bytes programmable RAM fonts and also supports optional external OSD.

AL260 is built-in 3-channel DAC for non-interlaced analog output and also supports 24bit digital output. It's housed with 208-pin QFP.

2. Function Block Diagram



3. Features

3.1 General Features

- Support Digital YUV input and Non-interlaced RGB/YPbPr Analog and Digital outputs
- Film Detection with Inverse 3:2/2:2 Pull Down
- Advanced De-interlacing with Motion Compensation
- AverLogic's Proprietary Cubic Scaling Algorithm for Scaling Up and Down
- Built-in 2K Bytes OSD RAM and support External OSD Font ROM
- Available in 208-pin PQFP
- 2.5V Core and 3.3V I/O power supplies with 5V input tolerant

3.2 Feature Description:

- Input Interface
 - NTSC/PAL support
 - Video interface ITU-R 601/656(8/16bit), YUV422 support
- Output Interface
 - Output resolution up to 1280x1024 @60Hz
 - Analog non-interlaced RGB/YPbPr output supported
- SDRAM Interface
 - Support maximum 32bit bus width SDRAM interface, two SDRAMs configuration up to 125 MHz supported
- De-interlacing and Scan Rate Conversion
 - De-Interlacing for Interlaced Video Input
 - Motion Compensation De-interlacing with Spatial and Temporal Filtering support
 - Film Detection with Inverse 3:2 & 2:2 pull down
 - Frame Rate Conversion(FRC) from 50Hz up to 120Hz
- Scaling Engine and Video Processing
 - Independent Scale Up and Down in both Horizontal and Vertical direction with 4-line, high precision interpolation
 - Digital Brightness/Contrast/Saturation Control
 - Keystone Correction for Front-Projection Systems
 - Sharpness Control
 - Built-in LUT for Gamma Correction and Color Adjustment
 - Dithering Logic for Color Depth Enhancement
- I2C or Parallel Port Registers Access
 - Registers can be accessed by serial I2C port or 8 bit parallel port for high speed registers data update
- On Screen Display (OSD)
 - 2K Bytes Internal OSD RAM for fine bitmaps and text font

- Dual internal OSD windows support with Alpha Blending/Transparency effect
- Support up to 64K Bytes External ROM for Font or Bitmap data
- In ROM mode, Internal OSD RAM supports 1.5K Bytes for Context RAM, 0.5K Bytes for Pre-fetch RAM
- Pre-fetch RAM supports different speed types of Font ROMs (EE-PROM, PROM or Mask-ROM)

- Other Features
 - Primary input stream VBI pass through support
 - Frame capture Mirroring support in Horizontal or Vertical direction
 - NTSC/PAL Video Input Auto-Detection support
 - Power Saving support
 - Slave mode support

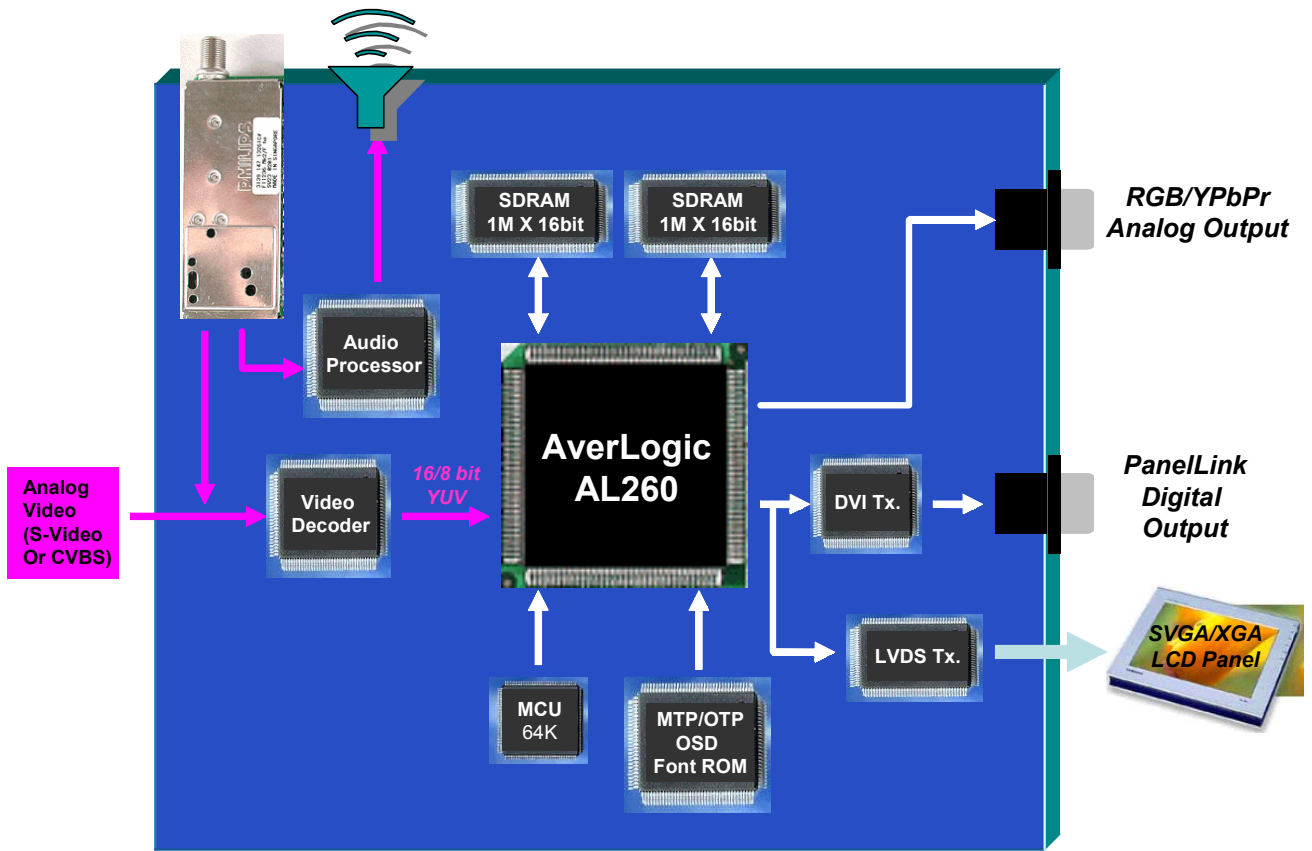
- Operating Power
 - 2.5V core and 3.3V I/O power supplies with 5V input tolerant

- Package
 - 208-pin PQFP

4 Applications

- LCD TV
- DTV & Front Projection/Rear Projection/Progressive Scan TVs
- TV to PC Monitor Format/Scan Rate Converter
- Video Enhancer/TV Tuner box

5 Application Example



7 Pin Definition and Description

7.1 Input Format Table of AL260:

| | | |
|---------|------|---------------|
| VIN No. | 15~8 | 7~0 |
| VIDEO | Y | CbCr YCbCr |

The pin-out definitions are described as follows:

| Pin Name | Pin Number | I/O type | Description |
|--------------------------------------|---------------------------|----------|--|
| Input Interface | | | |
| VIN [15:14], [13:10], [9:8] | 49-48, 46-43, 41-40 | I | Video Input Bus Bit 15-8, lower 8 bits of ITU-R 601 16bit data bus |
| VIN [7:4], [3:0] | 33-30, 28-25 | I | Video Input Bus Bit 7-0, upper 8 bits of ITU-R 601 16bit data bus OR Video Input Bus Bit 7-0 of ITU-R 656 8bit |
| VCLK | 35 | I | Reference Clock of Video Port |
| VHREFF | 37 | I | HDE of Video Port |
| VHS | 38 | I | HSYNC of Video Port |
| VVS | 39 | I | VSYNC of Video Port |
| OSD ROM Interface | | | |
| RDATA [6:0], [7] | 22-16, 24 | I | ROM Data Bus Bit 7-0 |
| RA [15:0] | 203-188 | O | ROM Address Bus Bit 15-0 |
| DAC Output Interface | | | |
| AVDD33 | 154 | AP | 3.3v Analog Power for DAC |
| AVSS33 | 136 | AG | Analog GND for DAC |
| AVDD25 | 152 | AP | 2.5V Analog Power for DAC |
| AVSS25 | 153 | AG | Analog GND for DAC |
| AVDD33R | 146 | AP | 3.3 V Analog Power for Channel R |

| Pin Name | Pin Number | I/O type | Description |
|---|---------------------------------|----------|------------------------------------|
| AVSS33R | 147 | AG | Analog GND for Channel R |
| AVDD33G | 143 | AP | 3.3 V Analog Power for Channel G |
| AVSS33G | 144 | AG | Analog GND for Channel G |
| AVDD33B | 140 | AP | 3.3 V Analog Power for Channel B |
| AVSS33B | 141 | AG | Analog GND for Channel B |
| DVDD25 | 137 | AP | 2.5V Digital Power for DAC |
| DVSS25 | 138 | AG | Digital GND for DAC |
| IOR | 145 | O | Channel R Current Output |
| IOG | 142 | O | Channel G Current Output |
| IOB | 139 | O | Channel B Current Output |
| RSET | 148 | I | Full-Scale Adjust Resister |
| COMP | 149 | I | Compensation Pin |
| VREFIN | 150 | I | Voltage Reference Input |
| VREFOUT | 151 | O | Voltage Reference Output |
| Digital Output Panel Interface | | | |
| VOUT [23:16], [15:5], [4:0] | 185-178, 168-158, 133-129 | O | Digital Video Output Bit 23-0 |
| SCLK | 170 | O | Display Pixel Clock |
| PDSDEN | 172 | O | Display Data Enable |
| PHS | 173 | I | HSYNC Input for Slave Mode |
| PVS | 174 | I | VSYSNC Input for Slave Mode |
| OXIN | 176 | I | Reference Clock for Display Device |
| SDRAM Interface | | | |
| MDATA [31:24], [23:12], [11:0] | 113-106, 103-92, 83-72 | I/O | SDRAM Data Bus Bit 31-0 |
| MADDR [10:6], [5:0] | 128-124, 122-117 | I/O | SDRAM Address Bit 10-0 |

| Pin Name | Pin Number | I/O type | Description |
|----------------------------|-----------------|----------|--------------------------------------|
| PMXIN | 115 | I | SDRAM Read Data Input Sampling Clock |
| BA[1:0] | 91-90 | O | SDRAM Bank Address Bit 0-1 |
| RASB | 89 | O | SDRAM Row Address Strobe |
| CASB | 88 | O | SDRAM Column Address Strobe |
| WEB | 87 | O | SDRAM Write Enable |
| CLK | 85 | O | SDRAM reference Clock |
| Host Interface | | | |
| HOST_DB [7:2], [1:0] | 59-54, 51-50 | I/O | Host Bus Bit 7-0 |
| HOST_WRB | 63 | I | Reference Clock |
| HOST_RDB | 64 | I | Read/Write Strobe |
| HOST_DENB | 65 | I | Data Cycle |
| HOST_MEMB | 69 | I | Memory Cycle |
| HOST_RDYB | 70 | O | Read Data Ready Output |
| IREQ | 71 | O | Interrupt Output |
| SDA | 205 | I/O | Data Bit for Serial Bus |
| SCL | 204 | I | Clock Bit for Serial Bus |
| I2C_EN | 186 | I | I2C Enable |
| INTB | 206 | O | Interrupt for Serial Protocol |
| PLL Interface | | | |
| MXIN | 15 | I | Crystal Input (14.31818MHz) |
| MXOUT | 14 | O | Crystal Output |
| P1VDD25 | 2,7 | DP | 2.5V Pad Ring Power for PLL1 |
| P1VSS25 | 3,6 | DG | Pad Ring GND for PLL1 |
| P1AVDD25 | 5 | AP | Analog Power for PLL1 |
| P1AVSS25 | 4 | AG | Analog GND for PLL1 |
| P2VDD25 | 8,12 | DP | 2.5V Pad Ring Power for PLL2 |
| P2VSS25 | 9,13 | DG | Pad Ring GND for PLL2 |
| P2AVDD25 | 11 | AP | Analog Power for PLL2 |
| P2AVSS25 | 10 | AG | Analog GND for PLL2 |
| Others | | | |

| Pin Name | Pin Number | I/O type | Description |
|-------------------------------|--|----------|---------------------|
| RSTB | 207 | I | Reset |
| NC | 61, 67 | | No Connection |
| DIGITAL POWER / GROUND | | | |
| VDD25 | 34, 42, 62, 86, 116, 134, 156, 177 | DP | Digital Power 2.5V |
| VSS25 | 36, 47, 60, 68, 84, 135, 155, 171, 187 | DG | Digital Ground 2.5V |
| VDD33 | 1, 29, 53, 66, 105, 169, 208 | DP | Digital Power 3.3V |
| VSS33 | 23, 52, 104, 114, 123, 157, 175 | DG | Digital Ground 3.3V |

Note: For I/O type, “I”, “O”, “AP”, “AG”, “DP”, and “DG” stand for “Input”, “Output”, “Analog Power”, “Analog Ground”, “Digital Power”, and “Digital Ground” respectively.

8 General Function Description

8.1 Function Blocks

AL260 provide a fully programmable structure allowing video stream process more flexible. The AL260 data process is executed by parsing in the modules such as capture, down scale, memory, up scale and mixer. In each module, data will be manipulated corresponding to the setting of registers. Due to the lack of the number of registers, some registers require banking to other page for access. There are 4 group registers, base control registers, capture control registers, memory control registers and display control registers. The value of base register 0eh determines which group of registers is taken effect. If register 0eh is programmed to value 00, the group of base control registers is chosen; and the register 0eh with value 01 is for capture register group, value 02 is for memory register group and value 03 is for display register group. The register 0eh must be set to corresponding value before that group of register can be accessed.

| Register | Group ID | Group register Description | | Symbol | Example |
|----------|----------|----------------------------|---|--------|---------|
| 0Eh | <1:0> | 00 | Access only base control registers | BAS# | BAS#16 |
| | | 01 | Access capture and base control registers | CAP# | CAP#20 |
| | | 10 | Access memory and base control registers | MEM# | MEM#32 |
| | | 11 | Access display and base control registers | DIS# | DIS#61 |

8.2 VIU (Video Input Unit)

AL260 accepts 16/8bit YUV 4:2:2 (NTSC/PAL) video data stream with ITU-R-656/601 standards. Applying AverLogic Proprietary Scaling algorithm, the video stream can be scaled down to accommodate required output resolutions with high quality scaling effect. The high quality scaling engine also ensures full screen output display.

8.2.1 Input Data Format

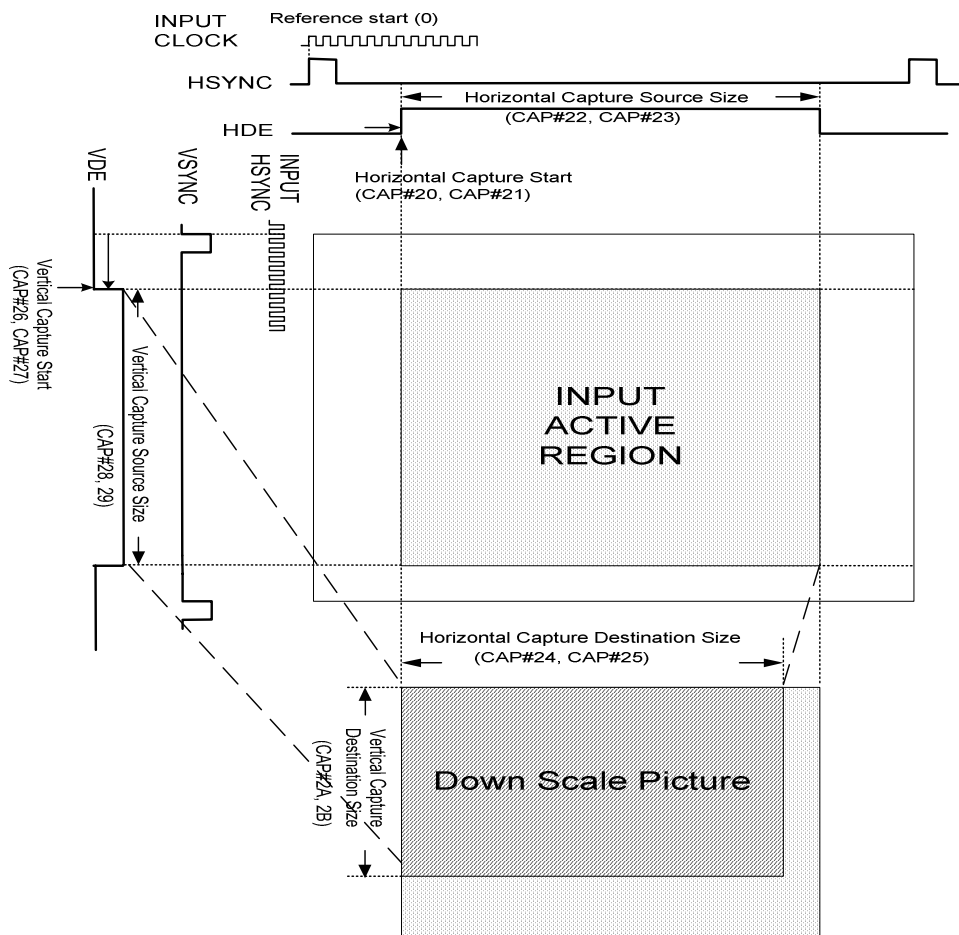
The AL260 is an integrated video processor that automatically detects and converts multiple video formats. The Index and Base registers provide user an expansion of the

control registers, which implements easy control of the input and the desired output format. The Base registers control the input type and target format.

The AL260 accepts two data formats: 8-bit ITU-R BT.656 (CCIR656) and 16-bit CCIR601 422. The clock and sync signal pins separate for RGB or YUV while the YUV data share the same pins as RGB data. For detailed applications, please refer to AL260 Application Notes.

8.2.2 Video Capture and Down Scale Engine

The AL260 has a high-quality scaling engine performing proprietary scaling operations independently in both Horizontal and Vertical direction with 4-line, high precision interpolation.



AL260 Input/Capture timing and Down Scale

8.2.3 Automatic Positioning Registers

The AL260 can detect and report input capture timing for Auto-adjustment function. It detects the starting and ending positions of active video in both direction (Horizontal and Vertical) and ensures the output fit properly into the display region. The data threshold value defines the sensibility of valid data. The capture data will be sampled and qualified base upon the value of data threshold, so that it can determine the starting point and ending point of an active line or an active frame.

8.2.4 PLL Programming for Memory and Display Clock

AL260 embedded 2 independent 200MHz PLL-Based Clock Generator. One is used to generate SDRAM clock, the other is for output clock. They are all reference input clock from XIN (generally 14.318MHZ).

There are 3 operation modes in defined in PLL register: Power Down Mode, Bypass Mode and Normal Mode. Power Down Mode forces FOUT to low and PLL in low power consumption state (<10uW). Bypass Mode provides FOUT with the same frequency as FIN. Normal Mode synthesizes FOUT by programming suitable divider values. It needs a Tready time (Pull_in Time + Locking Time) for PLL to re-lock the FIN clock when PLL wakes up from Power Mode to Normal Mode. In general, it should be reserved a Tread time for re-locking when PLL is changed to Normal Mode from Power Mode or Bypass Mode, or when any divider setting is changed.

8.3 MIU (Memory Interface Unit)

MIU supports SDRAM 32bit bus width interface. AL260 supports various SDRAM configurations, such as 512Kx16, 2ea. It uses sequential Burst mode to control SDRAM memory that operates at minimum 120MHz of clock frequency. For detailed operation of SDRAM, please reference memory specifications.

8.3.1 DRAM Bandwidth Consideration

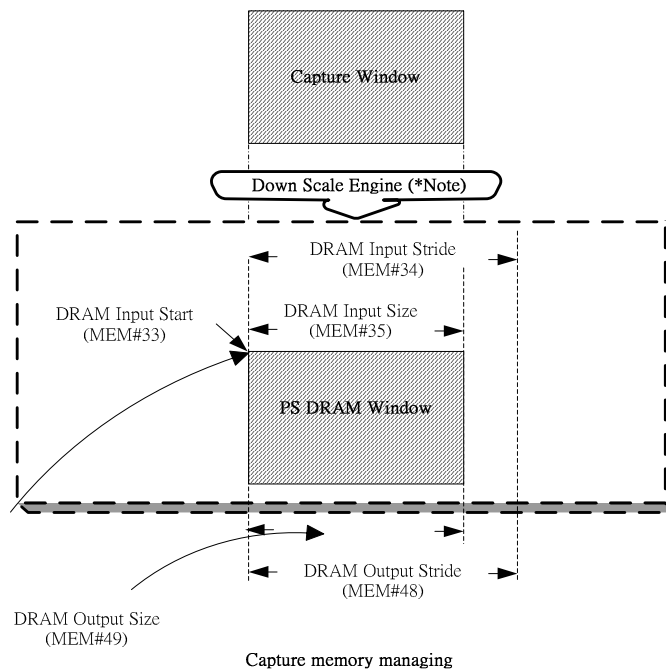
The AL260 uses external DRAMS for the purpose of frame rate conversion between the

input video and the output video device. The frame rate conversion for video is done by double buffering.

8.3.2 DRAM Input/Output Windows

The proceeding diagrams will describe the DRAM input control.

The DRAM input data size depends on the horizontal capture destination size.



After the input data size has been defined, the memory address of input data can be determined by the register DRAM input stride. The DRAM input stride can be programmed to provide extra memory space for input data.

8.3 VPU (Video Processing Unit)

AL260 identifies video input sources including Progressive Film (24/25 frames/sec) and Interlaced Video (50/60 fields/sec) and selects appropriate de-interlacing algorithm for video enhancement. VPU supports Film Detection with Inverse 3:2 or 2:2 Pull Down and AverLogic Proprietary De-interlacing. When AL260 detects the video source as Film, then

progressive scan frames will be reassembled and output twice input rate such as 50/60 frame/sec. Otherwise, it will be taken as Interlaced Video Source, and processed by using De-interlacing to reduce video artifacts. The scaling engine offers Scale-Up effect by applying Cubic Scaling Algorithm. It supports independent Scale-Up in both Horizontal and Vertical direction with 4-line, high precision interpolation. AL260 also offers Digital Contrast, Brightness, and Saturation for Color adjustment. It can be adjusted in YUV data. The Sharpness Control provides good effect for image enhancement. It also provides Keystone function for Projector application.

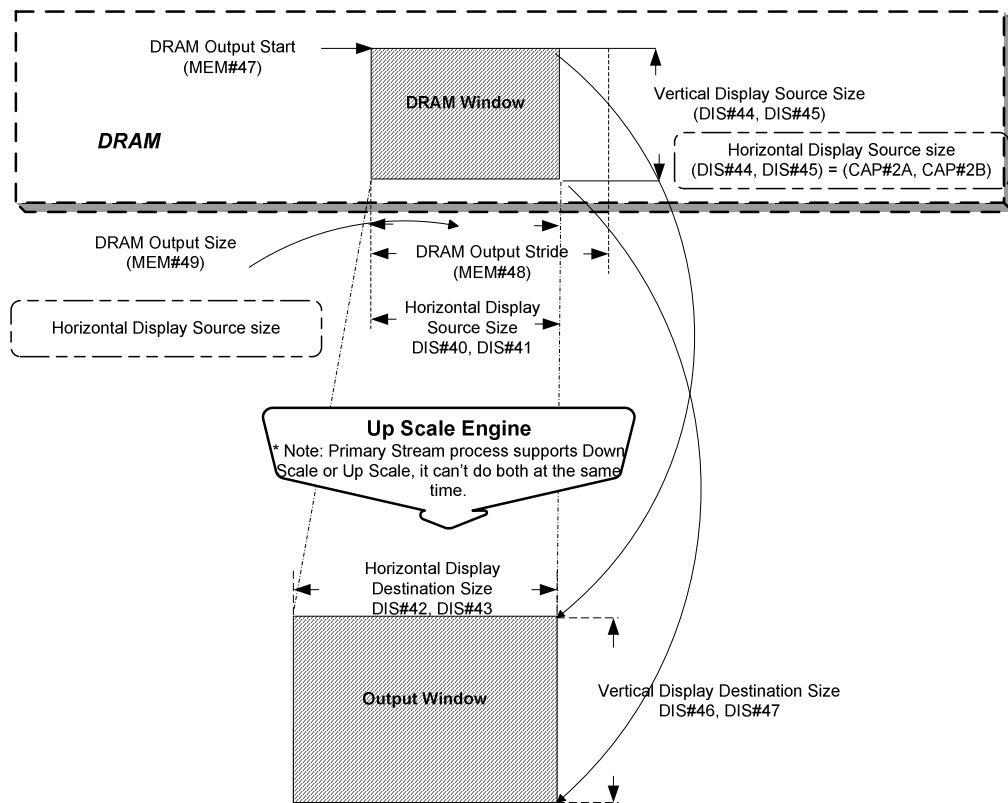
8.4.1 Video De-Interlaced with Film Detection and Motion Adaptive

Video Processing unit equips a high quality de-interlacing algorithm to optimize the output progressive scan frame by recovering film sequence and compensating motion effect during the de-interlacing process. The motion estimation can evaluate both Y/C data or Y data by setting register. In Motion compensation process, the sensitivity of the data estimation can be adjusted by register for Lumina and Chroma threshold. In film video, such as DVD movie, some duplicate fields are inserted into the interlaced video stream. Original film sequence detection and recovery can produce a smooth progressive scan frame transition after de-interlaced.

8.4.2 Up Scale Engine

The Up Scale Engine can scale up Primary Stream to higher resolution in high quality for output display. The AL260 adapts FIR scaling engine that can do horizontal and vertical up scale independently. The primary stream picture can be either down scale to smaller size of picture or up scale to larger size of picture from original capture (input) picture for output, but it can not do both up and down scale process at the same time. Consider to capture full picture of input data if the output resolution of primary stream picture is going to be enlarged.

Following block diagram illustrates the define registers of source primary stream window and destination up scale window.



Up scale block diagram and defined registers

8.4.3 Keystone Up Scale Engine

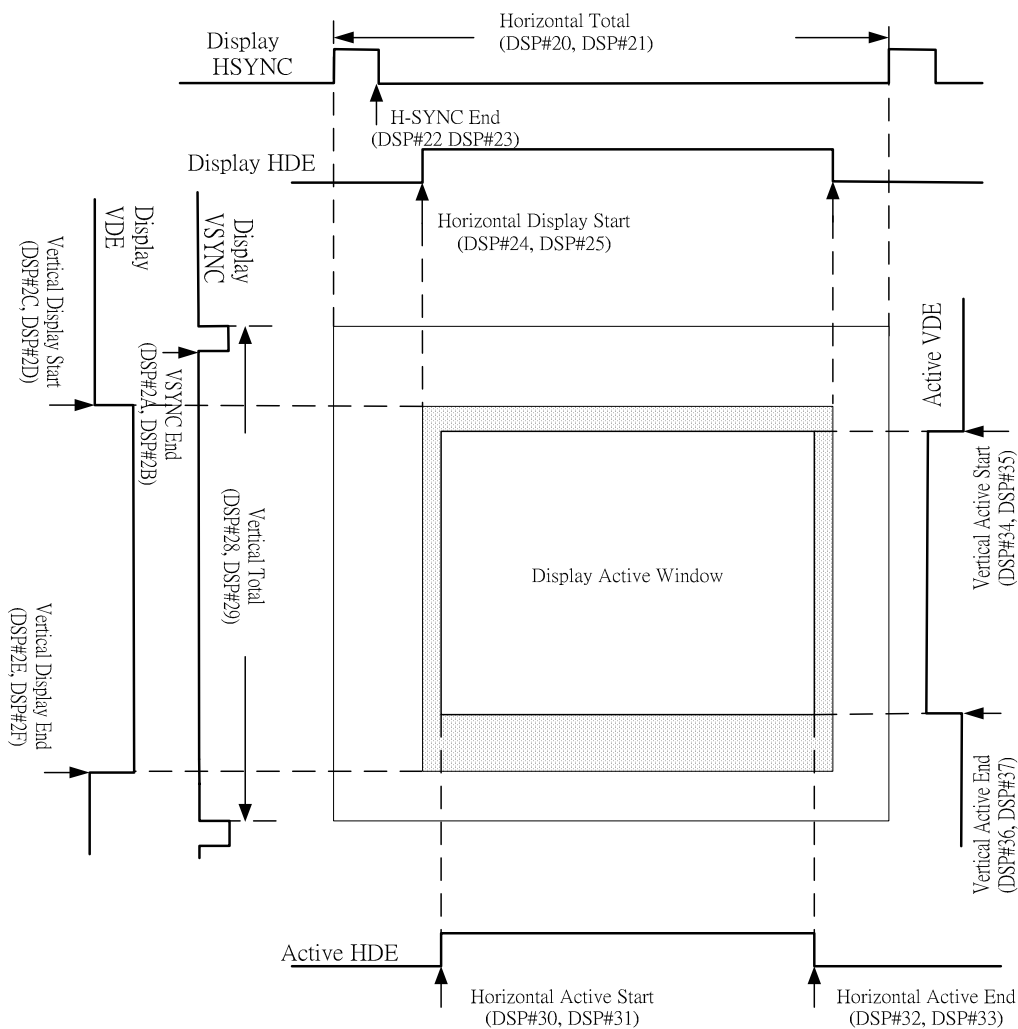
The AL260 can scale up the image in dynamic ratio which is good for LCD projector image correction. The projected images from the LCD projector sometimes show as Figure due to the misalignment or cheap optics. The AL260 can up scale picture in dynamic ratios which are loaded from pre-stored at internal FIFO buffers. The keystone is designed to compensate the distortions, such as figures following.

8.4VOU (Video Output Unit)

Two independent On-Screen-Display (OSD) windows provide overlay for a control menu, text, or caption on the output display. The AL260's OSD is very flexible in the way that the font, size, and display location are all programmable. The internal 2K byte SRAM provides storage for the OSD information. The OSD can be operated with only this

internal SRAM or with an external ROM to store font tables or even larger bitmaps. Built-in 8bit Programmable Gamma Look-Up Table for each input color channel for Gamma Correction. It may be used for RGB Contrast, Brightness and Color Temperature adjustments. Dithering is performed to retain color resolution for LCD panels that support 18-bit color depths.

AL260 provides Digital video output interface that can be directly connected to 24bit TFT LCD Panel or DVI/LVDS Transmitters. It also provides Analog video output which can support up to SXGA resolution.



AL260 Output timing and display windows

8.5.1 OSD

Two independent On-Screen-Display (OSD) windows provide overlay for a control menu, text, or caption on the output display. The AL260's OSD is very flexible in the way that the font, size, and display location are all programmable. The internal 2K byte SRAM provides storage for the OSD information. The OSD can be operated with only this internal SRAM or with an external ROM to store font tables or even larger bitmaps.

Regarding the detailed usage, please refer to AL260's OSD Application Note.

8.5.2 LUT (Look up table for Gamma Correction and Color Enhancement)

Because of the different characteristics of TV's and PC monitors, direct color space conversion from TV to PC may not show the same color that the human eye sees from the original video on the TV. The contrast may not be sufficient, and the hue may not be accurate, so to resolve these issues the AL260 has a gamma correction internal LUT implemented.

The AL260 provides programmable registers for implementing the LUT. The directly converted colors are sent to the LUT that then sends out the mapped, corrected colors.

The user can program the LUT based on his/her own experiments on specific types of monitors. The typical input-output mapping curve is usually somewhat like the following:

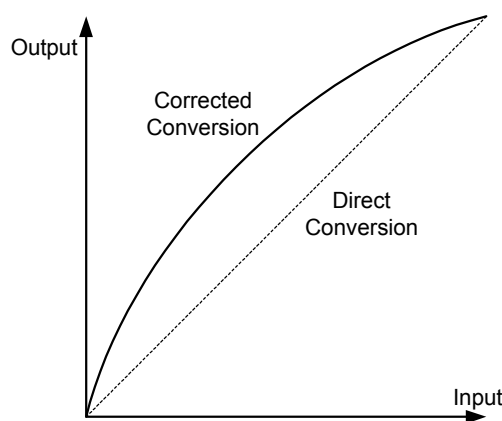


Figure 11 LUT Mapping

8.5.3 Dithering

The AverLogic offers dithering technique that simulates display of colors that are not in the current color space of a particular image. The Dithering logic provides additional color depth enhancement to retain color resolution for LCD panels that support 18-bit color depth.

8.5 BIU (Bus Interface Unit)

It supports I²C serial and proprietary parallel programming interfaces. I²C serial interface requires two wires to access while the proprietary parallel interface needs 11 wires. The communication speed of proprietary parallel interface is much faster than I²C serial interface.

Regarding to the detailed usage, please refer to AL260's General Application Note.

9 Register Definition

Registers are provided to setup AL260. These registers can be programmed via host interface. The host interface protocol is illustrated in “Host Interface” paragraph. The application notes will describe more detailed settings about these registers. Upon request, AverLogic will provide the sample code or tool of host interface control software.

9.1 Register Set

| Register Name | Address | R/W | Default | Function |
|---|-----------|-----|---------|---------------------------------------|
| Base Control Group Registers | | | | |
| COMPANYID | 00h | R | 46h | Company ID |
| INTRMASK | 02h | R/W | 00h | Interrupt Mask |
| INTRSTATUS | 03h | R/W | 00h | Interrupt Vector and Mode |
| CAPCTRL | 06h | R/W | 00h | Capture Data Control |
| DISCTRL1 | 07h | R/W | 00h | Display Data Control 1 |
| DISCTRL2 | 08h | R/W | 00h | Display Data Control 2 |
| POLARITYCTRL | 09h | R/W | 00h | Display Polarity Control |
| OTIMECTRL | 0Ah | R/W | 00h | Display Timing Control |
| GROUPACCESS | 0Eh | R/W | 00h | Group Access ID |
| INSRCFORMAT | 11h | R/W | 00h | Input Video Source Format |
| INPUTCTRL | 12h | R/W | 00h | Input Control |
| HREFDLY | 13h | R/W | 00h | Horizontal Reference Delay |
| CAPCTRL1 | 14h | R/W | 00h | Capture control 1 |
| CAPCTRL2 | 16h | R/W | 00h | Capture control 2 |
| MEMACCR | 17h | R/W | 00h | Memory Access Control |
| INVMSB | 18h | R/W | 00h | Inverted MSB of Capture Data Format |
| PLLSETR | 1Bh | R/W | 00h | PLL Setting for Memory and Display |
| MPLLNF | 1Ch | R/W | 00h | LSB of NF Value for Memory PLL |
| MPLLNRO | 1Dh | R/W | 00h | MSB of NF/NR/NO Value for Memory PLL |
| OPLLNF | 1Eh | R/W | 00h | LSB of NF Value for Display PLL |
| OPLLNRO | 1Fh | R/W | 00h | MSB of NF/NR/NO Value for Display PLL |
| Capture Control Group Registers (Accessible when BAS#0E = 01h) | | | | |
| Capture Timing | | | | |
| CAPHSTART | 21h & 20h | R/W | 00h | Horizontal Capture Start |

| Register Name | Address | R/W | Default | Function |
|--|-----------|-----|---------|---------------------------------------|
| CAPHSRCSIZE | 23h & 22h | R/W | 00h | Horizontal Capture Source Size |
| CAPHDESTSIZE | 25h & 24h | R/W | 00h | Horizontal Capture Destination Size |
| CAVSTART | 27h & 26h | R/W | 00h | Vertical Capture Start |
| CAPVSRCSIZE | 29h & 28h | R/W | 00h | Vertical Capture Source Size |
| CAPVDESTSIZE | 2Bh & 2Ah | R/W | 00h | Vertical Capture Destination Size |
| INTERLACECTRL | 2Eh | R/W | 00h | Interlace Control |
| HDNRATIO | 31h & 30h | R/W | 00h | Horizontal Scale Down Ratio |
| VDNRATIO | 33h & 32h | R/W | 00h | Vertical Scale Down Ratio |
| VBI Input Timing | | | | |
| VBIVSTART | 34h | R/W | 00h | VBI Vertical Capture Start |
| VBIVEND | 35h | R/W | 00h | VBI Vertical Capture End |
| VBIHSTART | 36h | R/W | 00h | VBI Horizontal Capture Start |
| VBIHSIZE | 37h | R/W | 00h | VBI Horizontal Capture Size |
| ITU-656 Detection | | | | |
| 656HSTART | 38h | R/W | 20h | ITU656 data Horizontal sync start |
| 656HEND | 39h | R/W | A0h | ITU656 data Horizontal sync end |
| 656VSTART | 3Ah | R/W | 02h | ITU656 data Vertical sync start |
| 656VEND | 3Bh | R/W | 04h | ITU656 data Vertical sync end |
| Position Detection | | | | |
| POSDATATH | 50h | R/W | 00h | Data Threshold for Position Detection |
| POSHDESTART | 53h & 52h | R | | Horizontal Capture Active Start |
| POSHDEEND | 55h & 54h | R | | Horizontal Capture Active End |
| POSVDESTART | 57h & 56h | R | | Vertical Capture Active Start |
| POSVDEEND | 59h & 58h | R | | Vertical Capture Active End |
| Mode Detection | | | | |
| CAPHTOTALCNT | 63h & 62h | R | | Horizontal Capture Total Counter |
| CAPVTOTALCNT | 65h & 64h | R | | Vertical Capture Total Counter |
| DBUFFLAGNUML | 70h | R/W | 00h | Double Buffer Flag Number LSB |
| DBUFFLAGNUMH | 72h | R/W | 00h | Double Buffer Flag Number MSB |
| TUNEINCLK | 73h | R/W | 00h | Tune Input Clock Timing |
| Memory Control Group Registers(Accessible when reg.0Eh = 02h) | | | | |
| DRAM Control | | | | |

| Register Name | Address | R/W | Default | Function |
|-----------------------------------|-----------|-----|---------|--------------------------------|
| DRAMACCESSCTRL | 20h | R/W | 00h | DRAM Access control |
| DRAMWRITE | 21h | R/W | 00h | DRAM Write |
| OUTFIFOCTRL | 22h | R/W | 00h | Output FIFO Control |
| INFIFOCTRL | 23h | R/W | 00h | Input FIFO Control |
| DRAMMINREFRESH | 28h | R/W | 00h | DRAM Minimum Refresh |
| DRAMCTRL | 2Ah & 29h | R/W | 00h | DRAM Control Register |
| DRAMRADDR | 2Dh ~ 2Bh | R/W | 00h | DRAM Read Address |
| XYMIRRORIN | 30h | R/W | 00h | XY Mirror Input |
| XYMIRROROUT | 31h | R/W | 00h | XY Mirror Output |
| SKIPMODE | 32h | R/W | 10h | Skip Mode |
| DRAM Input Window Control | | | | |
| DRAMSTART | 33h | R/W | 10h | DRAM Input Start |
| DRAMSTRIDE | 34h | R/W | 00h | DRAM Input Stride |
| DRAMISIZE | 35h | R/W | 00h | DRAM Input Size |
| DRAM Window Copy Control | | | | |
| WCSRCSTART | 3Bh ~ 39h | R/W | 00h | Window Copy Source Start |
| GSDRAMINPUTSTRIDE | 3Ch | R/W | 00h | Window Copy Source Stride |
| GSDRAMINPUTSIZE | 3Dh | R/W | 00h | Window Copy HSize |
| WCSTRIDE | 3Eh | R/W | 00h | Direct Write Stride |
| WCDESTSTART | 41h ~ 3Fh | R/W | 00h | Window Copy Destination Start |
| DASTART | 44h ~ 42h | R/W | 00h | Direct Read/Write Address |
| WCSIZE | 45h | R/W | 00h | Window Copy Size |
| WCLINETOTAL | 46h | R/W | 00h | Window Copy Line Total |
| DRAM Output Window Control | | | | |
| DRAMSTART | 47h | R/W | 00h | DRAM Output Start |
| DRAMSTRIDE | 48h | R/W | 00h | DRAM Output Stride |
| DRAMSIZ | 49h | R/W | 00h | DRAM Output Size |
| VBISTART | 4Fh ~ 4Dh | R/W | 00h | VBI Starting Address |
| FRONTMD | 50h | R/W | 00h | Front Motion Detect Control |
| TUNEMCLK | 51h | R/W | 00h | Tune Memory Write Clock Timing |
| TUNEPMCLK | 52h | R/W | 00h | Tune Memory Read Clock Timing |
| DRAM Data Port | | | | |

| Register Name | Address | R/W | Default | Function |
|--|-----------|-----|---------|-------------------------------------|
| READSTATUS | 60h | R | | Read Status |
| BYTE0 | 61h | R/W | 00h | Byte 0 |
| BYTE1 | 62h | R/W | 00h | Byte 1 |
| BYTE2 | 63h | R/W | 00h | Byte 2 |
| BYTE3 | 64h | R/W | 00h | Byte 3 |
| BYTE4 | 65h | R/W | 00h | Byte 4 |
| BYTE5 | 66h | R/W | 00h | Byte 5 |
| Display Control Group Registers (Accessible when reg.0Eh = 03h) | | | | |
| Display Timing | | | | |
| DISHTOTAL | 21h ~ 20h | R/W | 00h | Display Horizontal Total |
| DISHSEND | 23h & 22h | R/W | 00h | Display Horizontal Sync |
| DISHDESTART | 25h & 24h | R/W | 00h | Horizontal Display Start |
| DISHDEEND | 27h & 26h | R/W | 00h | Horizontal Display End |
| DISVTOTAL | 29h & 28h | R/W | 00h | Display Vertical Total |
| DISVSEND | 2Bh & 2Ah | R/W | 00h | Display Vertical Sync |
| DISVDESTART | 2Dh & 2Ch | R/W | 00h | Vertical Display Start |
| DISVDEEND | 2Fh & 2Eh | R/W | 00h | Vertical Display End |
| Window Output Timing | | | | |
| DISHDESTART | 31h & 30h | R/W | 00h | Horizontal Display Start |
| DISHDEEND | 33h & 32h | R/W | 00h | Horizontal Display End |
| DISVDESTART | 35h & 34h | R/W | 00h | Vertical Display Start |
| DISVDEEND | 37h & 36h | R/W | 00h | Vertical Display End |
| Zoom In Control Registers | | | | |
| DISHSRCsize | 41h & 40h | R/W | 00h | Horizontal Display Source Size |
| DISHDESTsize | 43h & 42h | R/W | 00h | Horizontal Display Destination Size |
| DISVSRCSIZE | 45h & 44h | R/W | 00h | Vertical Display Source Size |
| DISVDESTSIZE | 47h & 46h | R/W | 00h | Vertical Display Destination Size |
| ZOOMFCTRL | 48h | R/W | 00h | Zoom In Filter Control |
| HUPRATIO | 4Bh & 4Ah | R/W | 00h | Horizontal Scale Up Ratio |
| DELTAHUPRATIO | 4Bh & 4Ah | R/W | 00h | Delta Horizontal Scale Up Ratio |
| VUPRATIO | 4Dh & 4Ch | R/W | 00h | Vertical Scale Up Ratio |
| HPHASE | 4Fh & 4Eh | R/W | 00h | Horizontal Scale Up Initial Phase |

| Register Name | Address | R/W | Default | Function |
|----------------------------|-----------|-----|---------|--------------------------------------|
| VPHASE | 51h & 50h | R/W | 00h | Vertical Scale Up Initial Phase |
| OUTPUTMODE | 54h | R/W | 00h | Output Mode |
| LUTINDEX | 55h | R/W | 00h | LUT Write Index |
| LUTRED | 5Ch | R/W | 00h | LUT Red Color LSB |
| LUTGREEN | 5Dh | R/W | 00h | LUT Green Color LSB |
| LUTBLUE | 5Eh | R/W | 00h | LUT Blue Color LSB |
| LUTCOLOR | 5Fh | R/W | 00h | LUT Color MSB and Read/Write Trigger |
| PATTERNGEN | 56h | R/W | 00h | Pattern Generator and GPO |
| OSD Color Registers | | | | |
| OSDRAMWADDR | 59h & 58h | R/W | 00h | OSD Write Address |
| OSDRAMWDATA | 5Ah | W | 00h | OSD Write Data Port |
| COLOR0RED | 60h | R/W | 00h | Color 0 Red |
| COLOR0GREEN | 61h | R/W | 00h | Color 0 Green |
| COLOR0BLUE | 62h | R/W | 00h | Color 0 Blue |
| COLOR1RED | 63h | R/W | 00h | Color 1 Red |
| COLOR1GREEN | 64h | R/W | 00h | Color 1 Green |
| COLOR1BLUE | 65h | R/W | 00h | Color 1 Blue |
| COLOR2RED | 66h | R/W | 00h | Color 2 Red |
| COLOR2GREEN | 67h | R/W | 00h | Color 2 Green |
| COLOR2BLUE | 68h | R/W | 00h | Color 2 Blue |
| COLOR3RED | 69h | R/W | 00h | Color 3 Red |
| COLOR3GREEN | 6Ah | R/W | 00h | Color 3 Green |
| COLOR3BLUE | 6Bh | R/W | 00h | Color 3 Blue |
| COLOR4RED | 6Ch | R/W | 00h | Color 4 Red |
| COLOR4GREEN | 6Dh | R/W | 00h | Color 4 Green |
| COLOR4BLUE | 6Eh | R/W | 00h | Color 4 Blue |
| COLOR5RED | 6Fh | R/W | 00h | Color 5 Red |
| COLOR5GREEN | 70h | R/W | 00h | Color 5 Green |
| COLOR5BLUE | 71h | R/W | 00h | Color 5 Blue |
| COLOR6RED | 72h | R/W | 00h | Color 6 Red |
| COLOR6GREEN | 73h | R/W | 00h | Color 6 Green |
| COLOR6BLUE | 74h | R/W | 00h | Color 6 Blue |

| Register Name | Address | R/W | Default | Function |
|------------------------------|-----------|-----|---------|-------------------------------------|
| COLOR7RED | 75h | R/W | 00h | Color 7 Red |
| COLOR7GREEN | 76h | R/W | 00h | Color 7 Green |
| COLOR7BLUE | 77h | R/W | 00h | Color 7 Blue |
| OSD Control Registers | | | | |
| OSDCOLORSEL | 78h | R/W | 00h | OSD Color Select |
| BLINKTIME | 79h | R/W | 00h | OSD Blink Timer |
| OSDMODE | 80h | R/W | 00h | OSD Modes |
| FOREOP | 81h | R/W | 00h | Logic Operation 1 |
| FOREOP | 83h | R/W | 00h | Logic Operation 2 |
| FADEALPHA | 82h | R/W | 00h | Fading Alpha Value |
| OSD1 Registers | | | | |
| OSDCONTROL1 | 84h | R/W | 00h | OSD1 Control |
| ROMSTARTADDR1 | 85h | R/W | 00h | OSD1 ROM Start Address |
| FONTADDRUNIT1 | 86h | R/W | 00h | OSD1 Font Address Unit |
| OSDHSTART1 | 90h | R/W | 00h | OSD1 Horizontal Start |
| OSDVSTART1 | 91h | R/W | 00h | OSD1 Vertical Start |
| RAMADDRST1 | 92h | R/W | 00h | OSD1 RAM Start Address |
| RAMSTRIDE1 | 8Bh & 93h | R/W | 00h | OSD1 RAM Horizontal Stride |
| BMAPHSIZE1 | 95h & 94h | R/W | 00h | OSD1 Bitmap Horizontal Size |
| BMAPHTOTAL1 | 97h & 96h | R/W | 00h | OSD1 Bitmap Horizontal Total Pixels |
| BMAPVSIZE1 | 99h & 98h | R/W | 00h | OSD1 Bitmap Vertical Size |
| BMAPVTOTAL1 | 9Bh & 9Ah | R/W | 00h | OSD1 Bitmap Vertical total Lines |
| ICONHTOTAL1 | 9Ch | R/W | 00h | OSD1 Icon Horizontal Total |
| ICONVTOTAL1 | 9Dh | R/W | 00h | OSD1 Icon Vertical Total |
| FONTLINESIZE1 | AEh | R/W | 00h | OSD1 Font Line Size |
| OSD2 Registers | | | | |
| OSDCONTROL2 | 88h | R/W | 00h | OSD2 Control |
| ROMSTARTADDR2 | 89h | R/W | 00h | OSD2 ROM Start Address |
| FONTADDRUNIT2 | 8Ah | R/W | 00h | OSD2 Font Address Unit |
| OSDHSTART2 | A0h | R/W | 00h | OSD2 Horizontal Start |
| OSDVSTART1 | A1h | R/W | 00h | OSD2 Vertical Start |
| RAMADDRST2 | A2h | R/W | 00h | OSD2 RAM Start Address |

| Register Name | Address | R/W | Default | Function |
|--|-----------|-----|---------|---------------------------------------|
| RAMSTRIDE2 | 8Ch & A3h | R/W | 00h | OSD2 RAM Horizontal Stride |
| BMAPHSIZE2 | A5h & A4h | R/W | 00h | OSD2 Bitmap Horizontal Size |
| BMAPHTOTAL2 | A7h & A6h | R/W | 00h | OSD2 Bitmap Horizontal Total Pixels |
| BMAPVSIZE2 | A9h & A8h | R/W | 00h | OSD2 Bitmap Vertical Size |
| BMAPVTOTAL2L | ABh & AAh | R/W | 00h | OSD2 Bitmap Vertical Total Lines |
| ICONHTOTAL2 | ACh | R/W | 00h | OSD2 Icon Horizontal Total |
| ICONVTOTAL2 | ADh | R/W | 00h | OSD2 Icon Vertical Total |
| FONTLINESIZE2 | AFh | R/W | 00h | OSD2 Font Line Size |
| Desktop Color Registers | | | | |
| DESKR | B3h | R/W | 00h | Desktop Color Component Red |
| DESKG | B4h | R/W | 00h | Desktop Color Component Green |
| DESKB | B5h | R/W | 00h | Desktop Color Component Blue |
| Film Detection/ Motion Compensation Registers | | | | |
| MOTIONCNTTH | C5h & C4h | R/W | 00h | Motion Counter Threshold |
| LUMATH | C6h | R/W | 00h | Lumina(Y) Threshold |
| CHROMATH | C7h | R/W | 00h | Chroma(C) Threshold |
| MCCTRL | C8h | R/W | 00h | De-interlacing Control Register |
| FILMCTRL | C9h | R/W | 00h | Film Detection Control Register |
| PHASECTRL | CAh | R/W | 00h | Phase Detection Control Register |
| MVCNT | CFh & CEh | R | 00h | Motion Pixel Numbers |
| Keystone/Sharpness Registers | | | | |
| SHPKEYCTRL | CBh | R/W | 00h | Sharpness/Keystone Control Register |
| KEYADDR | C1h & C0h | R/W | 00h | Keystone Parameters Address |
| Tri-Level Sync Registers | | | | |
| TRISYNCA | D0h | W | 00h | Tri-Level Sync Parameter Period a |
| TRISYNCB | D1h | W | 00h | Tri-Level Sync Parameter Period b |
| TRISYNCD1 | D2h | W | 00h | Tri-Level Sync Parameter Delta 1 |
| TRISYNCD2 | D3h | W | 00h | Tri-Level Sync Parameter Delta 2 |
| TRISYNCLANK | D4h | W | 00h | Tri-Level Sync Parameter Period Blank |
| TRISYNCLEVEL | D7h | W | 00h | Tri-Level Sync Level |
| Display Parameter Registers | | | | |
| DISTUNEHS | C2h | R/W | | Tune Display Horizontal Sync Phase |

| Register Name | Address | R/W | Default | Function |
|----------------------|----------------|------------|----------------|---------------------------------------|
| DISTUNESCLK | CCh | R/W | | Tune Display Pixel Clock Phase |
| PHASECTRL | CAh | R/W | | Phase Detection Control Register |
| DISHTOTAL | D8h & D7h | R | | Display Horizontal Total Counter |
| DISVTOTAL | DAh & D9h | R | | Display Vertical Total Counter |
| PHASECNT | DCh & DBh | R | | Phase Counter |
| DISADJEN | F0h | R/W | 00h | Enable Brightness/Contrast/Saturation |
| BRIGHTNESS | F1h | R/W | 80h | Brightness Level |
| CONTRAST | F2h | R/W | 40h | Contrast Level |
| SATURATION | F3h | R/W | 40h | Saturation Level |

9.2 Register Description

➤ Base Control Group Registers

| INDEX | Register Description | | |
|-------|---------------------------------|-------|---|
| (HEX) | Register Name | BITS | Function Description |
| 00 | Company ID (R) [COMPANYID] | | |
| | CompanyID | <7:0> | Company ID (46h) |
| 02 | Interrupt Mask (R/W) [INTRMASK] | | |
| | DVsyncIntMask | <0> | Display VSYNC interrupt mask 0 Mask interrupt issued by VSYNC of display 1 Interrupt issued when display VSYNC is activated |
| | CAPVsyncIntMask | <1> | Capture VSYNC interrupt mask 0 Mask interrupt issued by VSYNC 1 Interrupt issued when VSYNC is activated |
| | Reserved | <2> | Reserved |
| | VBIMask | <3> | Display vertical blank interrupt mask 0 Mask interrupt issued by display vertical blank 1 Interrupt issued by display vertical blank |
| | FilmDetMask | <4> | H/W Film detected finished interrupt mask 0 Mask interrupt issued by film detection 1 Interrupt issued when HW film detected |
| | FullDetMask | <5> | FIFO full for directly memory write Interrupt Mask 0 Mask interrupt issued by FIFO full for directly write to SDRAM 1 Interrupt issued by FIFO full for directly write to SDRAM |
| | WCopyEndMask | <6> | Window copy finished interrupt mask 0 Mask interrupt issued by window copy 1 Interrupt issued by window copy |
| | FIFOFullMask | <7> | Arbiter FIFO full interrupt mask 0 Mask interrupt issued by FIFO index of arbiter 1 Interrupt issued when FIFO is full |

03 Interrupt Vector and Mode (R)(W) [INTRSTATUS]

| | | |
|-----------------|-------|---|
| DVsyncInt (R) | <0> | Display VSYNC interrupt |
| CAPVsyncInt (R) | <1> | Capture VSYNC interrupt |
| Reserved | <2> | Reserved |
| VBIInt (R) | <3> | Display vertical blank interrupt |
| FilmDet (R) | <4> | H/W Film detected finished interrupt |
| FullDet (R) | <5> | FIFO full for directly memory write interrupt |
| WCopyEnd (R) | <6> | Window copy finished interrupt |
| FIFOFull (R) | <7> | Arbiter FIFO full interrupt |
| IntMode(W) | <0> | 0 Triqaer mode |
| | | 1 Level mode |
| | <1> | 0 High active |
| | | 1 Low active |
| | <7:2> | Reserved |

04~05: Reserved

06 Capture Data Control (R/W) [CAPCTRL]

| | | |
|-------------|-------|--|
| CapVScaleDn | <0> | Capture vertical scale down enable |
| | | 0 Disable |
| | | 1 Enable |
| Reserved | <4:1> | Tie to "0000" |
| SoGo | <5> | Display timing strobe by capture VSYNC |
| Reserved | <6> | Tie to 1 |
| GO | <7> | Capture timing enable |
| | | 0 Disable |
| | | 1 Enable |

07 Display Data Control 1 (R/W) [DISCTRL1]

| | | |
|----------|-------|-------------------------------------|
| Reserved | <2:0> | Tie to "011" |
| CscEn | <3> | Capture data color space conversion |
| | | 0 Disable color space converter |
| | | 1 Enable color space converter |

| | | |
|-----------|-----|--|
| InvertOdd | <5> | Invert odd field signal |
| | 0 | Positive |
| | 1 | Negative |
| CSyncOut | <6> | Composite sync out |
| | 0 | Separate |
| | 1 | Composite |
| OPLLsel | <7> | Display reference clock source, refer to BAS#09<0> |
| | 0 | From external pin (OXIN1/OXIN2) |
| | 1 | From PLL |

0A Display Timing Control (R/W) [OTIMECTRL]

| | | |
|-----------------|-------|---|
| WinDisable | <0> | Display window diable |
| | 0 | Enable |
| | 1 | Disable |
| Reserved | <1> | Reserved |
| SlaveMode | <2> | Slave mode enable, refer to BAS#0A<3> |
| | 0 | Output timing driven by internal registers |
| | 1 | Output timing driven by external device(capture or external display device) |
| SlaveType | <3> | Slave mode type, refer to BAS#0A<2> |
| | 0 | Output timing is driven by capture timing |
| | 1 | Output timing is driven by external display device |
| CSYNCType | <5:4> | Compsit SYNC type |
| | 00 | XOR |
| | 01 | AND |
| | 10 | NXOR |
| | 11 | NAND |
| YPbPrAnalogOut | <6> | YPbPr analog output |
| | 0 | RGB output |
| | 1 | YpbPr output |
| YPbPrDigitalOut | <7> | YPbPr digital output |
| | 0 | RGB output |
| | 1 | YpbPr output |

0E Group Access ID (R/W) [GROUPACCESS]

| | | |
|---------------|-------|---|
| GroupAccessID | <1:0> | Group register access control |
| | 00 | Access only Base control registers |
| | 01 | Access Capture and Base control registers |
| | 10 | Access Memory and Base control registers |
| | 11 | Access Display and Base control registers |
| Reserved | <7:2> | Reserved |

11 Input Video Source Format (R/W) [INSRCFORMAT]

| | | |
|-------------|-------|---------------------------|
| CapInFormat | <1:0> | Capture data input format |
| | 00 | Reserved |
| | 01 | 16-bit |
| | 10 | 8-bit |
| | 11 | Reserved |
| Reserved | <5:2> | Reserved |
| Reserved | <6> | Tie to 0 |
| Reserved | <7> | Reserved |

12 Input Control (R/W) [INPUTCTRL]

| | | |
|----------|-------|--|
| Reserved | <2:0> | Tie to "000" |
| HsPol | <3> | Enable HS polarity detection |
| | 0 | Disable, when turn on auto position function |
| | 1 | Enable |
| VsPol | <4> | Enable VS polarity detection |
| | 0 | Disable, when turn on auto position function |
| | 1 | Enable |
| Reserved | <7:5> | Reserved |

13 Horizontal Reference Delay (R/W) [HREFDLY]

| | | |
|------------|-------|--------------------|
| CapHRefDly | <3:0> | Capture HRef delay |
| Reserved | <7:4> | Reserved |

14 Capture control 1 (R/W) [CAPCTRL1]

| | | |
|-------------|-----|--------------------------------------|
| CapHScaleDn | <0> | Enable horizontal capture scale down |
|-------------|-----|--------------------------------------|

| | | |
|---------------|-------|---------------------------------------|
| Reserved | <1> | Reserved |
| Cap656SyncSel | <2> | Capture SYNC source when ITU656 input |
| | | 0 From external SYNC input pin |
| | | 1 From decoded ITU656 data |
| CapSoftRef | <3> | Capture HREF source |
| | | 0 From external HREF input pin |
| | | 1 Software programmable |
| Reserved | <7:4> | Reserved |

16 Capture control 2 (R/W) [CAPCTRL2]

| | | |
|-------------|-------|---|
| Reserved | <1:0> | Tie to "00" |
| InvOddField | <2> | Invert internal detected capture odd field signal |
| Reserved | <3> | Reserved |
| Cap444En | <4> | Input data format |
| | | 0 YPbPr input format |
| | | 1 YCbCr input format |
| Cap656En | <5> | Enable input source is ITU656 format |
| DEdgeEn | <6> | Double edge sampling for ITU656 input |
| Reserved | <7> | Reserved |

17 Memory Access Control Register(R/W) [MEMACCR]

| | | |
|----------|-----|--|
| MemWEn | <0> | Directly write enable |
| MemREn | <1> | Directly read enable |
| HostMode | <2> | Host data mode |
| | | 0 2x16-bit per each host cycle |
| | | 1 1x24-bit per each host cycle |
| Reserved | <3> | Tie to "1" |
| DMAEn | <4> | Enable data output of directly memory |
| Reserved | <5> | Reserved |
| WCopyEn | <6> | Window copy enable |
| | | 0 Disable window copy |
| | | 1 Enable window copy |
| MclkSel | <7> | Memory clock select |
| | | 0 Memory clock from external PIN (XIN) |

1 Memory clock from internal PLL

18 Inverted MSB of Capture Data Format (R/W) [INVMSB]

| | | |
|----------|-------|-------------------------------|
| InvBit7 | <0> | Inverted bit 7 of input data |
| InvBit15 | <1> | Inverted bit 15 of input data |
| InvBit23 | <2> | Inverted bit 23 of input data |
| Reserved | <7:3> | Reserved |

Note: Please refer to General Application Note

PLL Registers

1B PLL Setting Register for Memory and Display(R/W) [PLLSETR]

| | | |
|---------|-----|---------------------------------|
| OPLLPd | <0> | Power Down for Display PLL |
| | | 0 PLL normal Operation |
| | | 1 PLL Power Down |
| OPLLVon | <1> | Reset for Display PLL |
| | | 0 PLL normal Operation |
| | | 1 Reset the PLL NF & NR Divider |
| OPLLBp | <2> | Bypass Mode for Display PLL |
| | | 0 PLL normal Operation |
| | | 1 Bypass the PLL & FOUT=FIN |
| OPLLOe | <3> | Output Control for Display PLL |
| | | 0 FOUT= Fck/NO |
| | | 1 FOUT=0 |
| MPLLPd | <4> | Power Down for Memory PLL |
| | | 0 PLL normal Operation |
| | | 1 PLL Power Down |
| MPLLVon | <5> | Reset for Memory PLL |
| | | 0 PLL normal Operation |
| | | 1 Reset the PLL NF & NR Divider |
| MPLLBp | <6> | Bypass Mode for Memory PLL |
| | | 0 PLL normal Operation |
| | | 1 Bypass the PLL & FOUT=FIN |
| MPLLOe | <7> | Output control for memory PLL |
| | | 0 FOUT= Fck/NO |

1 FOUT=0

Note: $FOUT = FIN * NF / (NR * NO) = FVCO / NO$, here FVCO is between 80MHz and 190Mhz

Here, FIN is input clock (example:14.31818MHz XTAL)

NF/NR, and NO are refer to BAS#1C~1F definition

1C LSB of NF Value for Memory PLL(R/W) [MPLLNF]

| | | |
|--------|-------|----------------------------------|
| MPLLNF | <7:0> | MPLLNF<7:0> Value for memory PLL |
|--------|-------|----------------------------------|

Note: NF is MPLLNF+2

1D MSB of NF/NR/NO Value for Memory PLL(R/W) [MPLLNRO]

| | | |
|--------|-------|----------------------------------|
| MPLLNR | <4:0> | MPLLNR<4:0> value for memory PLL |
| MPLLNO | <6:5> | MPLLNO<1:0> value for memory PLL |
| MPLLNF | <7> | MPLLNF<8> Value for memory PLL |

Note: NR is MPLLNR+2, NO is MPLLNO+1

1E LSB of NF Value for Display PLL(R/W) [OPLLNF]

| | | |
|--------|-------|-----------------------------------|
| OPLLNF | <7:0> | OPLLNF<7:0> Value for display PLL |
|--------|-------|-----------------------------------|

Note: NF is OPLLNF+2

1F MSB of NF/NR/NO Value for Display PLL(R/W) [OPLLNRO]

| | | |
|--------|-------|-----------------------------------|
| OPLLNR | <4:0> | OPLLNR<4:0> value for display PLL |
| OPLLNO | <6:5> | OPLLNO<1:0> value for display PLL |
| OPLLNF | <7> | OPLLNF<8> Value for display PLL |

Note: NR is OPLLNR+2, NO is OPLLNO+1

➤ **Capture Control Group Registers (Accessible when BAS#0E = 01h)**

I. Capture Timing

| INDEX | Register Description | | |
|-------|---|-------|--|
| (HEX) | Register Name | BITS | Function Description |
| 20 | Horizontal Capture Start LSB (R/W) [CAPHSTART] | | |
| | CapHStartL | <7:0> | Bits<7:0> of horizontal capture start position (Unit: 1 pixel) |
| 21 | Horizontal Capture Start MSB (R/W) [CAPHSTART] | | |
| | CapHStartH | <3:0> | Bits<11:8> of horizontal capture start position |
| | Reserved | <7:4> | Reserved |
| 22 | Horizontal Capture Source Size LSB (R/W) [CAPHSRCSIZE] | | |
| | CapHSrcSizeL | <7:0> | Bits<7:0> of horizontal capture source size (Unit: 1 pixel) |
| 23 | Horizontal Capture Source Size MSB (R/W) [CAPHSRCSIZE] | | |
| | CapHSrcSizeH | <3:0> | Bits<11:8> of horizontal capture source size |
| | Reserved | <7:4> | Reserved |
| 24 | Horizontal Capture Destination Size LSB (R/W) [CAPHDESTSIZE] | | |
| | CapHDestSizeL | <7:0> | Bits<7:0> of horizontal capture destination size (Unit: 1 pixel) |
| 25 | Horizontal Capture Destination Size MSB (R/W) [CAPHDESTSIZE] | | |
| | CapHDestSizeH | <3:0> | Bits<11:8> of horizontal capture destination size |
| | Reserved | <7:4> | Reserved |
| 26 | Vertical Capture Start LSB (R/W) [CAPVSTART] | | |
| | CapVStartL | <7:0> | Bits<7:0> of vertical capture start position (Unit: 1 line) |
| 27 | Vertical Capture Start MSB (R/W) [CAPVSTART] | | |
| | CapVStartH | <2:0> | Bits<10:8> of vertical capture start position |
| | Reserved | <7:4> | Reserved |

| | | | |
|---------------|---|--|--|
| 28 | Vertical Capture Source Size LSB (R/W) [CAPVSRCSIZE] | | |
| CapVSrcSizeL | <7:0> | Bits<7:0> of vertical capture source size (Unit: 1 line) | |
| 29 | Vertical Capture Source Size MSB (R/W) [CAPVSRCSIZE] | | |
| CapVSrcSizeH | <2:0> | Bits<10:8> of vertical capture source size | |
| Reserved | <7:4> | Reserved | |
| 2A | Vertical Capture Destination Size LSB (R/W) [CAPVDESTSIZE] | | |
| CapVDestSizeL | <7:0> | Bits<7:0> of vertical capture destination size (Unit: 1 line). | |
| 2B | Vertical Capture Destination Size MSB (R/W) [CAPVDESTSIZE] | | |
| CapVDestSizeH | <2:0> | Bits<10:8> of vertical capture destination size | |
| Reserved | <7:4> | Reserved | |
| 2E | Interlace Control (R/W) [INTERLACECTR] | | |
| InterlaceEn | <0> | Enable interlace timing input | |
| FieldCap | <2:1> | Field capture into memory | |
| | | 00 | Capture even and odd field into memory |
| | | 01 | Capture odd field only |
| | | 10 | Capture even field only |
| | | 11 | Reserved |
| Fieldoffset | <7:4> | Field capture offset | |
| 30 | Horizontal Scale Down Ratio LSB (R/W) [HDNRATIO] | | |
| HDnRatioL | <7:0> | Bits<7:0> of horizontal scale down ratio | |
| 31 | Horizontal Scale Down Ratio MSB (R/W) [HDNRATIO] | | |
| HDnRatioH | <0> | Bit<8> of horizontal scale down ratio | |
| Reserved | <7:1> | Reserved | |
| 32 | Vertical Scale Down Ratio LSB (R/W) [VDNRATIO] | | |
| VDnRatioL | <7:0> | Bits<7:0> of vertical scale down ratio | |
| 33 | Vertical Scale Down Ratio MSB (R/W) [VDNRATIO] | | |

| | | |
|-----------|-------|-------------------------------------|
| VDnRatioH | <0> | Bit<8> of vertical scale down ratio |
| Reserved | <7:1> | Reserved |

Note: HDNRATIO = CAPHDESTSIZE / CAPHSRCsize * 256

VDNRATIO = CAPVDESTSIZE / CAPVSRCSIZE * 256

II. VBI Input timing:

VBI captured data is always been stored in DRAM address, starting at 0.

To Disable VBI capture, set VBIVStart > VBIVEnd, and VBIHStart > VBIHEnd

34 VBI Vertical Start (R/W) [VBIVSTART]

| | | |
|-----------|-------|-------------------------------------|
| VBIVStart | <7:0> | VBI vertical capture start position |
|-----------|-------|-------------------------------------|

35 VBI Vertical End (R/W) [VBIVEND]

| | | |
|---------|-------|--------------------------|
| VBIVend | <7:0> | VBI vertical capture end |
|---------|-------|--------------------------|

36 VBI Horizontal Start (R/W) [VBIHSTART]

| | | |
|-----------|-------|---------------------------------------|
| VBIHStart | <7:0> | VBI horizontal capture start position |
|-----------|-------|---------------------------------------|

37 VBI Horizontal Size (R/W) [VBIVSIZE]

| | | |
|----------|-------|-----------------------------|
| VBIVSize | <7:0> | VBI horizontal capture size |
|----------|-------|-----------------------------|

III. ITU-656 Detection:

38 ITU-656 Hsync Start (R/W) [656HSTART]

| | | |
|-----------|-------|--|
| 656HStart | <7:0> | ITU656data horizontal sync start position, default value 20h |
|-----------|-------|--|

39 ITU-656 Hsync End (R/W) [656HEND]

| | | |
|---------|-------|--|
| 656HEnd | <7:0> | ITU656data horizontal sync end position, default value 80h |
|---------|-------|--|

3A ITU-656 Vsync Start (R/W) [656VSTART]

| | | |
|-----------|-------|--|
| 656VStart | <7:0> | ITU656data vertical sync start position, default value 02h |
|-----------|-------|--|

3B ITU-656 Vsync End (R/W) [656VEND]

656VEnd <7:0> ITU656data vertical sync end position, default value 04h

IV: Position Detection:

50 Data Threshold for Position Detection (R/W) [POSDATATH]

PosDataTh <7:0> Luma(brightness) threshold value

Note: CAP#50 is used to determine input non-blanking pixel for both horizontal and vertical direction. Any pixel luma value less than this value will be considered as blanking.

52 Horizontal Active Start LSB (R) [POSHDESTART]

PosHDEStartL <7:0> Bits<7:0> of detected horizontal active start position (Unit: 1 pixel)

53 Horizontal Active Start MSB (R) [POSHDESTART]

PosHDEStartH <2:0> Bits<10:8> of detected horizontal active start position

Reserved <7:3> Reserved

54 Horizontal Active End LSB (R) [POSHDEEND]

PosHDEEndL <7:0> Bits<7:0> of detected horizontal active start position (Unit: 1 pixel)

55 Horizontal Active End MSB (R) [POSHDEEND]

PosHDEEndH <2:0> Bits<10:8> of detected horizontal active end position

Reserved <7:3> Reserved

56 Vertical Active Start LSB (R) [POSVDESTART]

PosVDEStartL <7:0> Bits<7:0> of detected vertical active start line (Unit: 1 line)

57 Vertical Active Start MSB (R) [POSVDESTART]

PosVDEStartH <2:0> Bits<10:8> of detected vertical active start line

Reserved <7:3> Reserved

58 Vertical Active End LSB (R) [POSVDEEND]

PosVDEEndL <7:0> Bits <7:0> of detected vertical active end line (Unit: 1 line)

59 Vertical Active End MSB (R) [POSVDEEND]

| | | |
|------------|-------|---|
| PosVDEEndH | <2:0> | Bits<10:8> of detected vertical active end line |
| Reserved | <7:3> | Reserved |

V: Mode Detection:

62 Horizontal Capture Total Counter LSB (R) [CAPHTOTALCNT]

| | | |
|---------------|-------|---|
| CapHtotalCntL | <7:0> | Bits<7:0> of horizontal total count value |
|---------------|-------|---|

63 Horizontal Capture Total Counter MSB (R) [CAPHTOTALCNT]

| | | |
|---------------|-------|--|
| CapHtotalCntH | <2:0> | Bits<10:8> of horizontal total count value |
| Reserved | <7:3> | Reserved |

64 Vertical Capture Total Counter LSB (R) [CAPVTOTALCNT]

| | | |
|---------------|-------|---|
| CapVtotalCntL | <7:0> | Bits<7:0> of vertical total count value |
|---------------|-------|---|

65 Vertical Capture Total Counter MSB (R) [CAPVTOTALCNT]

| | | |
|---------------|-------|--|
| CapVtotalCntH | <2:0> | Bits<10:8> of vertical total count value |
| Reserved | <7:3> | Reserved |

73 Tune Input Clock Phase (R/W) [TUNEINCLK]

| | | | |
|-----------|-------|------------------------------|---------------------|
| TuneInclk | <2:0> | Phase delay number(8 steps) | |
| | <4:3> | Phase delay types | |
| | | 00 | Inclk |
| | | 01 | Inclk + delay phase |
| | | 10 | Inversed Inclk |
| | 11 | Inversed Inclk + delay phase | |
| Reserved | <7:5> | Reserved | |

➤ **Memory Control Group Registers (Accessible when BAS#0E = 02h)**

I.DRAM control

INDEX Register Description

(HEX) Register Name BITS Function Description

20 DRAM Access control (R/W) [DRAMACCESSCTRL]

| | | |
|---------------|-----|------------------------------|
| InputEnable | <0> | Enable input data to DRAM |
| Reserved | <1> | Reserved |
| PowerUp | <2> | Enable power up |
| OutputEnable | <3> | Enable output data from DRAM |
| Reserved | <4> | Reserved |
| RefreshEnable | <5> | Enable DRAM refresh |
| PowerDown | <6> | Enable power down |
| SetMode | <7> | Enable DRAM setmode cycle |

21 DRAM Write (R/W) [DRAMWRITE]

| | | |
|--------------|-------|--------------------------------------|
| PMCLKSel | <0> | Select DRAM read clock signal path |
| | 0 | Internal loop |
| | 1 | External loop from pad MCLK to PMCLK |
| WriteMask1 | <1> | Write mask of DRAM byte 0, 1 |
| WriteMask2 | <2> | Write mask of DRAM byte 2 |
| SoftRest | <3> | Software Reset |
| DataDelay | <5:4> | DRAM data delay |
| DataRdyDelay | <7:6> | DRAM data ready delay |

22 Output & FIFO Control (R/W) [OUTFIFOCTRL]

| | | |
|-------------|-------|---------------------------|
| OutputLevel | <3:0> | Output FIFO level control |
| Reserved | <7:4> | Reserved |

23 Input FIFO Control (R/W) [INFIFOCTRL]

| | | |
|------------|-------|--------------------------|
| InputLevel | <3:0> | Input FIFO level control |
| Reserved | <7:4> | Reserved |

Note: These are DRAM FIFO water mark, when FIFO reach this urgent level, the corresponding video source needs to be serviced(R/W or to/from DRAM)

24~27: Reserved

28 **DRAM Minimum Refresh (R/W) [DRAMMINREFRESH]**

| | | |
|------------|-------|---|
| MinRefresh | <7:0> | Minimum refresh requirement within the period of a output VSYNC, usually 1/60 sec |
|------------|-------|---|

29 **DRAM Control 0 (R/W) [DRAMCTRL]**

| | | |
|------|-------|-----------------------------|
| TRAS | <1:0> | DRAM RAS control signal |
| | | 00 5 memory clocks |
| | | 01 6 memory clocks |
| | | 01 7 memory clocks |
| | | 11 8 memory clocks |
| TRC | <4:2> | DRAM RC control signal |
| | | 000 7 memory clocks |
| | | 001 8 memory clocks |
| | | 001 9 memory clocks |
| | | 011 10 memory clocks |
| | | 100 11 memory clocks |
| | | 101 12 memory clocks |
| | | 101 13 memory clocks |
| | | 111 14 memory clocks |
| TRCD | <5> | DRAM RCD control signals |
| | | 0 No delay |
| | | 1 Delay 1 memory clock |
| TRP | <6> | DRAM RP control signal |
| | | 0 No delay |
| | | 1 Delay 1 memory clock |
| TRPD | <7> | DRAM RPD control signal |
| | | 0 No delay |
| | | 1 Delay 1 memory clock |

2A DRAM Control 1 (R/W) [DRAMCTRL]

| | | |
|------------|-------|-----------------------------------|
| TWR | <0> | DRAM WR control signal |
| | 0 | No delay |
| | 1 | Delay 1 memory clock |
| TCL | <1> | DRAM CL control signal |
| | 0 | No delay |
| | 1 | Delay 1 memory clock |
| TRW | <2> | DRAM RW control signal |
| | 0 | No delay |
| | 1 | Delay 1 memory clock |
| MemConfig | <4:3> | SDRAM Size |
| | 00 | 16Mb |
| | 01 | 64Mb |
| | 10 | Reserved |
| | 11 | Reserved |
| BankConfig | <5> | Bank selector |
| | 0 | A22, 0-4M = bank 0, 4-8M = bank 1 |
| | 1 | A21, 4-6M = bank 0, 6-8M = bank 1 |
| Reserved | <6> | Tie to 1 |
| TXSR | <7> | DRAM XSR control signal |

Note: MEM#29&2A is SDRAM timing parameters. Default value: MEM#29="ef", MEM#2A="4f"

2B DRAM Read Address 0 (R/W) [DRAMRADDR]

MemReadAddr0 <7:0> Bits<7:0> of DRAM read address. (unit: 2 pixels)

2C DRAM Read Address 1 (R/W) [DRAMRADDR]

MemReadAddr1 <7:0> Bits<15:8> of DRAM read address

2D DRAM Read Address 2 (R/W) [DRAMRADDR]

MemReadAddr2 <4:0> Bits<20:16> of DRAM read address

Reserved <7:5> Reserved

30 XY Mirror Input (R/W) [XYMIRRORIN]

| | | |
|------------|-------|--|
| InputFlipX | <0> | Enable X mirror capture (horizontally captured in the reversed direction) |
| InputFlipY | <1> | Enable Y mirror capture (vertically captured in the reversed direction, i.e. up side down capture) |
| Reserved | <7:2> | Reserved |

31 XY Mirror Output (R/W) [XYMIRROROUT]

| | | |
|-------------|-------|---|
| OutputFlipX | <0> | Enable X mirror display (horizontally display in the reversed direction) |
| OutputFlipY | <1> | Enable Y mirror display (vertically displayed in the reversed direction, i.e. up side down display) |
| Reserved | <7:2> | Reserved |

32 Skip Mode (R/W) [SKIPMODE]

| | | |
|--------------|-------|--|
| InputSkip | <1:0> | DRAM input address pointer incremental unit 00 2 fields/1 frame stockpile, even1, odd1, even1, odd1, Note: Stride >= size 01 Reserved 10 4 fields/2frames stockpile F1(1),F2(1),F3(1),F4(1),F1(2),F2(2),F3(2)... Note: Stride >= size * 4 11 Reserved |
| Reserved | <2> | Reserved |
| TwoField | <3> | Two field mode enable |
| Reserved | <4> | Reserved |
| MemControlEn | <5> | 0 Disable sdram controller 1 Enable sdram controller |
| DbufferEn | <6> | Dobule buffering enable |
| Reserved | <7> | Reserved |

II. DRAM input window control

33 DRAM Input Start (R/W) [DRAMINSTART]

| | | |
|-------------|-------|--|
| DRAMINStart | <7:0> | Input DRAM address start (Unit: 8192 pixels) |
|-------------|-------|--|

34 DRAM Input Horizontal Stride (R/W) [DRAMINHSTRIDE]

DRAMINHStride <7:0> Input DRAM horizontal stride (Unit: 4 pixels)

35 DRAM Input Horizontal Size (R/W) [DRAMINHSIZE]

DRAMINHSize <7:0> Input DRAM horizontal size (Unit: 4 pixels)

Note: Set stride value at 64/128/256 boundary, will better ease DRAM timing.

DRAMINHSIZE = CAPHDESTSIZE(CAP#25&24) / 4

III. DRAM window copy control

39 Window Copy Source Start LSB (R/W) [WCSRCSTART]

GSInputStart1 <7:0> Bits<7:0> of GS input DRAM address start. (Unit: 8192 pixels)

3A Window Copy Source Start (R/W) [WCSRCSTART]

GSInputStart2 <7:0> Bits<15:8> of GS input DRAM address start

3B Window Copy Source Start MSB (R/W) [WCSRCSTART]

GSInputStart3 <3:0> Bits<18:16> of GS input DRAM address start

Reserved <7:4> Reserved

3C Window Copy Source Stride (R/W) [GSDRAMINPUTSTRIDE]

GSIStride <7:0> GS input DRAM stride. (8 pixels)

3D Window Copy Size (R/W) [GSDRAMINPUTSIZE]

GSHSize <7:0> GS input DRAM size. (Unit: 8 pixels)

3E Direct Write Stride (R/W) [WCSTRIDE]

WCStride <7:0> DRAM window copy stride. (Unit: 8 pixels)

3F Window Copy Destination Start LSB (R/W) [WCDESTSTART]

WCsrcStart1 <7:0> Bits<7:0> of DRAM window copy source address start. (Unit: 8 pixels)

40 Window Copy Destination Start (R/W) [WCDESTSTART]
 WCDestStart2 <7:0> Bits<15:8> of DRAM window copy source address start

41 Window Copy Destination Start MSB (R/W) [WCDESTSTART]
 WCDestStart3 <3:0> Bits<20:16> of DRAM window copy source address start
 Reserved <7:4> Reserved

Note: After writing to MEM#41, the Window Copy operation will be carried out.

42 Direct Read/Write Address LSB (R/W) [DASTART]
 DAddrStart1 <7:0> Bits<7:0> of DRAM window copy source address start. (Unit: 8 pixels)

43 Direct Read/Write Address (R/W) [DASTART]
 DAddrStart2 <7:0> Bits<15:8> of DRAM window copy source address start

44 Direct Read/Write Address MSB (R/W) [DASTART]
 DAddrStart3 <3:0> Bits<20:16> of DRAM window copy source address start
 Reserved <7:4> Reserved

45 Window Copy Size (R/W) [WCSIZE]
 WCSize <7:0> DRAM Directly Write size. (Unit: 8 pixels) or DRAM window copy total lines [7:0] for Window Copy.

46 Window Copy Line Total (R/W) [WCLINETOTAL]
 WCLineTotal <7:0> DRAM window copy total lines[2:0]. (1 line)

IV. DRAM output window control

47 DRAM Output Start (R/W) [DRAMOUTSTART]
 DRAMOutStart <7:0> Output DRAM address start. (Unit: 8192 pixels)

48 DRAM Output Horizontal Stride (R/W) [DRAMOUTHSTRIDE]

DRAMOutHStride <7:0> Output DRAM horizontal stride. (Unit: 4/8/12 pixels)

49 DRAM Output Horizontal Size (R/W) [DRAMOUTHSIZE]

DRAMOutHSize <7:0> Output DRAM horizontal size. (Unit: 4/8/12 pixels)

DRAMOHSIZE = DISHSRCSIZE(DIS#41&40) / 4

4D VBI Start Address LSB (R/W) [VBISTART]

VBIAddrStart1 <7:0> Bit<7:0> of VBI starting address.

4E VBI Start Address (R/W) [VBISTART]

VBIAddrStart2 <7:0> Bit<15:8> of VBI starting address.

4F VBI Start Address MSB (R/W) [VBISTART]

VBIAddrStart3 <3:0> Bit<19:16> of VBI starting address.

Reserved <7:4> Reserved

50 Front Motion Detect Control (R/W) [FRONTM]

FrontMYth <6:0> Y threshold Value for Front Motion

EnFrontM <7> Enable Front Motion Detection

51 Tune Memory Write Clock Phase (R/W) [TUNEMCLK]

TuneMclk <2:0> Phase delay number(8 steps)

<4:3> Phase delay types

00 Mclk

01 Mclk + delay phase

10 Inversed Mclk

11 Inversed Mclk + delay phase

Reserved <7:5> Reserved

52 Tune Memory Read Clock Phase (R/W) [TUNEPMCLK]

TunePMclk <2:0> Phase delay number(8 steps)

<4:3> Phase delay types

00 PMclk

| | | | |
|----------|-------|----------|------------------------------|
| | | 01 | PMclk + delay phase |
| | | 10 | Inversed PMclk |
| | | 11 | Inversed PMclk + delay phase |
| Reserved | <7:5> | Reserved | |

V. DRAM data port

60 Read Status (R) [READSTATUS]

| | | |
|----------|-------|------------|
| Status | <0> | Data Ready |
| Reserved | <7:1> | Reserved |

61 Byte 0 (R)(W) [BYTE0]

| | | |
|-----------|-------|---|
| RByte0(R) | <7:0> | Bits<7:0> of DRAM for read-out |
| WByte0(W) | <7:0> | Bits<7:0> of Pixel 0 for 16-bit mode Write, or Dummy field for 24-bit mode Write |

62 Byte 1 (R)(W) [BYTE1]

| | | |
|-----------|-------|---|
| RByte1(R) | <7:0> | Bits<15:8> of DRAM read-out |
| WByte1(W) | <7:0> | Bits<15:8> of Pixel 0 for 16-bit mode Write, or Blue field for 24-bit mode Write |

63 Byte 2 (R)(W) [BYTE2]

| | | |
|-----------|-------|---|
| RByte2(R) | <7:0> | Bits<23:16> of DRAM read-out |
| WByte2(W) | <7:0> | Bits<7:0> of Pixel 1 for 16-bit mode Write, or Green field for 24-bit mode Write |

64 Byte 3 (R)(W) [BYTE3]

| | | |
|-----------|-------|--|
| RByte3(R) | <7:0> | Bits<31:24> of DRAM read-out |
| WByte3(W) | <7:0> | <15:8> of Pixel 1 for 16-bit mode Write, or Red field for 24-bit mode Write |

65 Byte 4 (R) [BYTE4]

| | | |
|--------|-------|------------------------------|
| RByte4 | <7:0> | Bits<39:32> of DRAM read-out |
|--------|-------|------------------------------|

66 Byte5 (R) [BYTE5]

RByte4 <7:0> Bits<47:40> of DRAM read-out

DRAM data read ports are defined in MEM#61~66. MemReadAddr is defined in MEM#42~44. After reading MEM#60, the read cycle will be strobe if bit-0 is 0. MEM#60 should be read until bit 0 is 1. Then, read MEM#61~66 for the data read from SDRAM.

➤ **Display Control Group Registers (Accessible when BAS#0E = 03h)**

I. Display Timing

| INDEX | Register Description | | |
|--|--|-------|--|
| (HEX) | Register Name | BITS | Function Description |
| 20 | Horizontal Display Total LSB (R/W) [DISHTOTAL] | | |
| | DisHTotalL | <7:0> | Bits<7:0> of display horizontal total (Unit: 1 pixel) |
| 21 | Horizontal Display Total MSB (R/W) [DISHTOTAL] | | |
| | DisHTotalH | <3:0> | Bits<11:8> of display horizontal total |
| | Reserved | <7:4> | Reserved |
| 22 | Horizontal Display Sync LSB (R/W) [DISHSEND] | | |
| | DishSEndL | <7:0> | Bits<7:0> of display horizontal sync end (Unit: 1 pixel) |
| 23 | Horizontal Display Sync MSB (R/W) [DISHSEND] | | |
| | DishSEndH | <3:0> | Bits<11:8> of display horizontal sync end |
| | Reserved | <7:4> | Reserved |
| Note: Horizontal sync start at position 1. | | | |
| 24 | Horizontal Display Start LSB (R/W) [DISHDESTART] | | |
| | DishDEStartL | <7:0> | Bits<7:0> of horizontal display start (Unit: 1 pixel) |
| 25 | Horizontal Display Start MSB (R/W) [DISHDESTART] | | |
| | DishDEStartH | <3:0> | Bits<11:8> of horizontal display start |
| | Reserved | <7:4> | Reserved |
| 26 | Horizontal Display End LSB (R/W) [DISHDEEND] | | |
| | DishDEEndL | <7:0> | Bits<7:0> of horizontal display end (Unit: 1 pixel) |
| 27 | Horizontal Display End MSB (R/W) [DISHDEEND] | | |
| | DishDEEndH | <3:0> | Bits<11:8> of horizontal display end |

| | | | |
|--------------------------------------|---|-------|--|
| | Reserved | <7:4> | Reserved |
| 28 | Display Vertical Total LSB (R/W) [DISVTOTAL] | | |
| | DisVTotalL | <7:0> | Bits<7:0> of display vertical total (Unit: 1 pixel) |
| 29 | Display Vertical Total MSB (R/W) [DISVTOTAL] | | |
| | DisVTotalH | <3:0> | Bits <11:8> of display vertical total |
| | Reserved | <7:4> | Reserved |
| 2A | Display Vertical Sync LSB (R/W) [DISVSEND] | | |
| | DisVSEndL | <7:0> | Bits<7:0> of display vertical sync end (Unit: 1 pixel) |
| 2B | Display Vertical Sync MSB (R/W) [DISVSEND] | | |
| | DisVSEndH | <3:0> | Bits<11:8> of display vertical sync end |
| | Reserved | <7:4> | Reserved |
| Note: Vertical sync start at line 1. | | | |
| 2C | Vertical Display Start LSB (R/W) [DISVDESTART] | | |
| | DisVDEStartL | <7:0> | Bits<7:0> of vertical display start (Unit: 1 pixel) |
| 2D | Vertical Display Start MSB (R/W) [DISVDESTART] | | |
| | DisVDEStartH | <3:0> | Bits<11:8> of vertical display start |
| | Reserved | <7:4> | Reserved |
| 2E | Vertical Display End LSB (R/W) [DISVDEEND] | | |
| | DisVDEEndL | <7:0> | Bits<7:0> of vertical display end (Unit: 1 pixel) |
| 2F | Vertical Display End MSB (R/W) [DISVDEEND] | | |
| | DisVDEEndH | <3:0> | Bits<11:8> of vertical display end |
| | Reserved | <7:4> | Reserved |

II. Window Output Timing

30 Horizontal Display Active Start LSB (R/W) [DISHDESTART]

DisHDEStartL <7:0> Bits<7:0> of horizontal display active start (Unit: 1 pixel)

31 Horizontal Display Active Start MSB (R/W) [DISHDESTART]

DisHDEStartH <3:0> Bits<11:8> of horizontal display active start

Reserved <7:4> Reserved

32 Horizontal Display Active End LSB (R/W) [DISHDEEND]

DisHDEEndL <7:0> Bits<7:0> of horizontal display active end (Unit: 1 pixel)

33 Horizontal Display Active End MSB (R/W) [DISHDEEND]

DisHDEEndH <3:0> Bits<11:8> of horizontal display active end

Reserved <7:4> Reserved

34 Vertical Display Active Start LSB (R/W) [DISVDESTART]

DisVDEStartL <7:0> Bits<7:0> of vertical display active start (Unit: 1 pixel)

35 Vertical Display Active Start MSB (R/W) [DISVDESTART]

DisVDEStartH <3:0> Bits<11:8> of vertical display active start

Reserved <7:4> Reserved

36 Vertical Display Active End LSB (R/W) [DISVDEEND]

DisVDEEndL <7:0> Bits<7:0> of vertical display active end (Unit: 1 pixel)

37 Vertical Display Active End MSB (R/W) [DISVDEEND]

DisVDEEndH <3:0> Bits<11:8> of vertical display active end

Reserved <7:4> Reserved

III. Zoom In Control Registers

40 Horizontal Display Source Size LSB (R/W) [DISHSRCSIZE]

DisHSrcSizeL <7:0> Bits<7:0> of horizontal display source size (Unit: 1 pixel)

41 Horizontal Display Source Size MSB (R/W) [DISHSRCSIZE]

| | | |
|--------------|-------|--|
| DisHSrcSizeH | <3:0> | Bits<11:8> of horizontal display source size |
| Reserved | <7:4> | Reserved |

42 Horizontal Display Destination Size LSB (R/W) [DISHDESTSIZE]

| | | |
|---------------|-------|---|
| DisHDestSizeL | <7:0> | Bits<7:0> of horizontal display destination size (Unit: 1 pixel). |
|---------------|-------|---|

43 Horizontal Display Destination Size MSB (R/W) [DISHDESTSIZE]

| | | |
|---------------|-------|---|
| DisHDestSizeH | <3:0> | Bits<11:8> of horizontal display destination size |
| Reserved | <7:4> | Reserved |

44 Vertical Display Source Size LSB (R/W) [DISVSRCSIZE]

| | | |
|--------------|-------|--|
| DisVSrcSizeL | <7:0> | Bits<7:0> of vertical display source size (Unit:1 pixel) |
|--------------|-------|--|

45 Vertical Display Source Size MSB (R/W) [DISVSRCSIZE]

| | | |
|--------------|-------|--|
| DisVSrcSizeH | <3:0> | Bits<11:8> of vertical display source size |
| Reserved | <7:4> | Reserved |

46 Vertical Display Destination Size LSB (R/W) [DISVDESTSIZE]

| | | |
|---------------|-------|--|
| DisVDestSizeL | <7:0> | Bits<7:0> of vertical display source size (Unit:1 pixel) |
|---------------|-------|--|

47 Vertical Display Destination Size MSB (R/W) [DISVDESTSIZE]

| | | |
|---------------|-------|---|
| DisVDestSizeH | <3:0> | Bits<11:8> of vertical display destination size |
| Reserved | <7:4> | Reserved |

Note : DISHDESTSIZE >= DISHSRCSIZE, DISVDESTSIZE >= DISVSRCSIZE

48 Zoom In Filter Control (R/W) [ZOOMFCTRL]

| | | |
|----------|-------|--------------------------------------|
| VZoomEn | <0> | Enable vertical scale-up filtering |
| HZoomEn | <1> | Enable horizontal scale-up filtering |
| Reserved | <7:2> | Reserved |

4A Horizontal Scale Up Ratio LSB (R/W) [HUPRATIO]

| | | |
|-----------|-------|--|
| HUpRatioL | <7:0> | Bits<7:0> of horizontal scale up ratio |
|-----------|-------|--|

4B Horizontal Scale Up Ratio MSB (R/W) [HUPRATIO]

HUpRatioH <7:0> Bits<15:8> of horizontal scale up ratio

4A Delta Horizontal Scale Up Ratio LSB (R/W) [DELTAHUPRATIO]

DeltaHUpRatioL <7:0> Bits<7:0> delta of horizontal scale up ratio for Keystone

4B Delta Horizontal Scale Up Ratio MSB (R/W) [DELTAHUPRATIO]

DeltaHUpRatioH <3:0> Bits<11:8> delta of horizontal scale up ratio for Keystone

HDEStartInc <5:4> Delta of starting point of horizontal DE for Keystone

00 Added by 0

01 Added by 1

10 Added by 0

11 Substrate by 1

HDEEndInc <7:6> Delta of Ending point of horizontal DE for Keystone

00 Added by 0

01 Added by 1

10 Added by 0

11 Substrate by 1

Note: This definition is valid when DIS#CB<4>='1' and used in Keystone

4C Vertical Scale Up Ratio LSB (R/W) [VUPRATIO]

VUpRatioL <7:0> Bits<7:0> of vertical scale up ratio

4D Vertical Scale Up Ratio MSB (R/W) [VUPRATIO]

VUpRatioH <7:0> Bits<15:8> of vertical scale up ratio

Note: HUPRATIO = DISHSRCSIZE / DISHDESTSIZE * 8192

Note: VUPRATIO = DISVSRCSIZE / DISVDESTSIZE * 8192

4E Horizontal Scale Up Initial Phase LSB (R/W) [HPHASE]

HUpPhaseL <7:0> Bit<7:0> of horizontal scale up initial phase

4F Horizontal Scale Up Initial Phase MSB (R/W) [HPHASE]

HUpPhaseH <7:0> Bit<15:8> of horizontal scale up initial phase

| | | | |
|----|--|-------|--|
| 50 | Vertical Scale Up Initial Phase LSB (R/W) [VPHASE] | | |
| | VUpPhaseL | <7:0> | Bit<7:0> of vertical scale up initial phase |
| 51 | Vertical Scale Up Initial Phase MSB (R/W) [VPHASE] | | |
| | VUpPhaseH | <7:0> | Bit<15:8> of vertical scale up initial phase |
| 54 | Output Mode (R/W) [OUTPUTMODE] | | |
| | OutputMode | <1:0> | Output enable |
| | | 00 | Enable |
| | | 01 | Reserved |
| | | 10 | Reserved |
| | | 11 | Disable, Zero output |
| | Reserved | <4:2> | Reserved |
| | DitherMode | <5> | Enable dither output |
| | | 0 | No dither |
| | | 1 | 8 bits to 6 bits |
| | Reserved | <6> | Reserved |
| | LutEn | <7> | Enable built-in LUT look-up table |
| 55 | LUT Write Index (R/W) [LUTWINDEX] | | |
| | LUTWIndex | <7:0> | LUT access index |
| 5C | LUT Red Color LSB (R/W) [LUTRED] | | |
| | LUTRed | <7:0> | LUT red color port |
| 5D | LUT Green Color LSB (R/W) [LUTGREEN] | | |
| | LUTGreen | <7:0> | LUT green color port |
| 5E | LUT Blue Color LSB (R/W) [LUTBLUE] | | |
| | LUTBlue | <7:0> | LUT blue color port |
| 5F | LUT Read/Write Trigger (R/W) [LUTWEN] | | |
| | Reserved | <5:0> | Reserved |

| | | |
|--------|-------|--------------------------------------|
| LUTWEn | <7:6> | Write color field enable |
| | 00 | Red, Green and Blue written into LUT |
| | 01 | Only Red is written into LUT |
| | 10 | Only Green written into LUT |
| | 11 | Only Blue written into LUT |

56 Pattern Generator and GPO (R/W) [PATTERNGEN]

| | | | |
|-------------|-------|----|-----------------------------|
| PatternMode | <1:0> | 00 | Fram line |
| | | 01 | Color bar |
| | | 10 | Gray level |
| | | 11 | Line moier |
| PatternEn | <4> | | Enable pattern generation |
| GPO | <7:5> | | General purpose output port |

Note: Set register GPO(DIS#56<7:5>) value will effect pin GPO2~0 output status in phase

IV. OSD Color Registers

58 OSD Write Address LSB (R/W) [OSDRAMWADDR]

| | | |
|--------------|-------|-----------------------------------|
| OSDRamWAddrL | <7:0> | Bit<7:0> of OSD ram write address |
|--------------|-------|-----------------------------------|

59 OSD Write Address MSB (R/W) [OSDRAMWADDR]

| | | |
|--------------|-------|------------------------------------|
| OSDRamWAddrH | <2:0> | Bit<10:8> of OSD ram write address |
| Reserved | <7:3> | Reserved |

5A OSD Write Data Port (W) [OSDRAMWDATA]

| | | |
|----------|-------|-------------------------|
| OSDWData | <7:0> | OSD ram write data port |
|----------|-------|-------------------------|

60 Color 0 Red (R/W) [COLOR0RED]

| | | |
|-----------|-------|-----------------------|
| Color0Red | <7:0> | Color 0 Red Component |
|-----------|-------|-----------------------|

61 Color 0 Green (R/W) [COLOR0GREEN]

| | | |
|-------------|-------|-------------------------|
| Color0Green | <7:0> | Color 0 Green Component |
|-------------|-------|-------------------------|

| | |
|-------------|-----------------------------------|
| 62 | Color 0 Blue (R/W) [COLOR0RED] |
| Color0Blue | <7:0> Color 0 Blue Component |
| 63 | Color 1 Red (R/W) [COLOR1RED] |
| Color1Red | <7:0> Color 1 Red Component |
| 64 | Color 1 Green (R/W) [COLOR1GREEN] |
| Color1Green | <7:0> Color 1 Green Component |
| 65 | Color 1 Blue (R/W) [COLOR1BLUE] |
| Color1Blue | <7:0> Color 1 Blue Component |
| 66 | Color 2 Red (R/W) [COLOR2RED] |
| Color2Red | <7:0> Color 2 Red Component |
| 67 | Color 2 Green (R/W) [COLOR2GREEN] |
| Color2Green | <7:0> Color 2 Green Component |
| 68 | Color 2 Blue (R/W) [COLOR2BLUE] |
| Color2Blue | <7:0> Color 2 Blue Component |
| 69 | Color 3 Red (R/W) [COLOR3RED] |
| Color3Red | <7:0> Color 3 Red Component |
| 6A | Color 3 Green (R/W) [COLOR3GREEN] |
| Color3Green | <7:0> Color 3 Green Component |
| 6B | Color 3 Blue (R/W) [COLOR3BLUE] |
| Color3Blue | <7:0> Color 3 Blue Component |
| 6C | Color 4 Red (R/W) [COLOR4RED] |
| Color4Red | <7:0> Color 4 Red Component |
| 6D | Color 4 Green (R/W) [COLOR0GREEN] |

Color4Green <7:0> Color 4 Green Component

6E Color 4 Blue (R/W) [COLOR4BLUE]

Color4Blue <7:0> Color 4 Blue Component

6F Color 5 Red (R/W) [COLOR5RED]

Color5Red <7:0> Color 5 Red Component

70 Color 5 Green (R/W) [COLOR5GREEN]

Color5Green <7:0> Color 5 Green Component

71 Color 5 Blue (R/W) [COLOR5BLUE]

Color5Blue <7:0> Color 5 Blue Component

72 Color 6 Red (R/W) [COLOR6RED]

Color6Red <7:0> Color 6 Red Component

73 Color 6 Green (R/W) [COLOR6GREEN]

Color6Green <7:0> Color 6 Green Component

74 Color 6 Blue (R/W) [COLOR6BLUE]

Color6Blue <7:0> Color 6 Blue Component

75 Color 7 Red (R/W) [COLOR7RED]

Color7Red <7:0> Color 7 Red Component

76 Color 7 Green (R/W) [COLOR7GREEN]

Color7Green <7:0> Color 7 Green Component

77 Color 7 Blue (R/W) [COLOR7BLUE]

Color7Blue <7:0> Color 7 Blue Component

V. OSD Control Register

78 OSD Color Select (R/W) [OSDCOLORSEL]

| | | |
|--------------|-------|--|
| Osd1ColorSel | <1:0> | OSD1 color selection, 8 colors only apply when Font2byte= '1' and PixDepth1= '1' |
| | 00 | select OSD1 colors from index 3..0 |
| | 01 | select OSD1 colors from index 7..4 |
| | 10 | select OSD1 colors from index 7..0 |
| | 11 | Reserved |
| Osd2ColorSel | <3:2> | OSD2 color selection, 8 colors only apply when Font2byte= '1' and PixDepth2= '1' |
| | 00 | select OSD2 colors from index 3..0 |
| | 01 | select OSD2 colors from index 7..4 |
| | 10 | select OSD2 colors from index 7..0 |
| | 11 | Reserved |
| Font2byte | <4> | Two-byte font charter code mode, effective only when RomMode = '1' |
| Reserved | <7:5> | Reserved |

79 Blink Time (R/W) [BLINKTIME]

| | | |
|------------|-------|-----------------------|
| BlinkTimer | <6:0> | Blinking timing value |
| BlinkType | <7> | 0 Reverse color |
| | | 1 Bypass |

Note: OSD Blinking frequency = Vsync frequency / BlinkTimer

80 OSD Modes (R/W) [OSDMODE]

| | | |
|----------|-------|--|
| RomMode | <0> | Enable ROM mode |
| | 0 | Internal RAM mode |
| | 1 | External ROM mode |
| Reserved | <1> | Tie to 0 |
| Number | <7:2> | Adjust rom address width to access external rom data |

Note: The method of select the Number value show on OSD application note

81 Logic Operation (R/W) [FOREOP]

| | | |
|----------|-------|---|
| Color0Op | <1:0> | Logic operation between color 0 and video |
| | 00 | NOP, show only OSD |
| | 01 | OR, video or color 0 |
| | 10 | AND, video and color 0 |
| | 11 | XOR, video xor color 0 |
| Color1Op | <3:2> | Logic operation between color 1 and video |
| | 00 | NOP, show only OSD |
| | 01 | OR, video or color 1 |
| | 10 | AND, video and color 1 |
| | 11 | XOR, video xor color 1 |
| Color2Op | <5:4> | Logic operation between color 2 and video |
| | 00 | NOP, show only OSD |
| | 01 | OR, video or color 2 |
| | 10 | AND, video and color 2 |
| | 11 | XOR, video xor color 2 |
| Color3Op | <7:6> | Logic operation between color 3 and video |
| | 00 | NOP, show only OSD |
| | 01 | OR, video or color 3 |
| | 10 | AND, video and color 3 |
| | 11 | XOR, video xor color 3 |

83 Logic Operation (R/W) [FOREOP]

| | | |
|----------|-------|---|
| Color4Op | <1:0> | Logic operation between color 4 and video |
| | 00 | NOP, show only OSD |
| | 01 | OR, video or color 4 |
| | 10 | AND, video and color 4 |
| | 11 | XOR, video xor color 4 |
| Color5Op | <3:2> | Logic operation between color 5 and video |
| | 00 | NOP, show only OSD |
| | 01 | OR, video or color 5 |
| | 10 | AND, video and color 5 |
| | 11 | XOR, video xor color 5 |
| Color6Op | <5:4> | Logic operation between color 6 and video |
| | 00 | NOP, show only OSD |

| | | | |
|----------|-------|----|---|
| | | 01 | OR, video or color 6 |
| | | 10 | AND, video and color 6 |
| | | 11 | XOR, video xor color 6 |
| Color7Op | <7:6> | | Logic operation between color 7 and video |
| | | 00 | NOP, show only OSD |
| | | 01 | OR, video or color 7 |
| | | 10 | AND, video and color 7 |
| | | 11 | XOR, video xor color 7 |

Note: Color 0 ~ 7 are defined in DIS#60~77.

82 Fading Alpha Value (R/W) [FADEALPHA]

| | | | |
|-----------|-------|--|--|
| FadeAlpha | <5:0> | | The alpha factor for fading effect ranging |
| Reserved | <7:6> | | Reserved |

Note: FADEALPHA range from 00h to 20h, there is 33-level of fade-in/fade-out effect.

Output = Image * FADEALPHA/32 + OSD * (1 - (FADEALPHA /32))

Show only OSD: FADEALPHA = "000000" --- minimum alpha value(00h)

Show only Image: FADEALPHA = "100000" --- maximum alpha value(20h)

VI. OSD 1 Registers

84 OSD1 Control (R/W) [OSDCONTROL1]

| | | | |
|-----------|-------|----|--|
| PixDepth1 | <0> | | Number of bits per pixel of OSD1 |
| | | 0 | One bit per pixel |
| | | 1 | Two bits per pixel |
| BlinkEn1 | <1> | | OSD1 blinking enable, effective when RomMode = '1' |
| | | 0 | Disable blinking |
| | | 1 | Enable blinking |
| HZoom1 | <3:2> | | OSD1 horizontal zoom factor |
| | | 00 | OSD1 pixel H size equals to 1X of video pixel |
| | | 01 | OSD1 pixel H size equals to 2X of video pixel |
| | | 10 | OSD1 pixel H size equals to 4X of video pixel |
| | | 11 | OSD1 pixel H size equals to 8X of video pixel |

| | | |
|---------------|--|---|
| VZoom1 | <5:4> | OSD1 vertical zoom factor |
| | 00 | OSD1 pixel V size equals to 1X of video pixel |
| | 01 | OSD1 pixel V size equals to 2X of video pixel |
| | 10 | OSD1 pixel V size equals to 4X of video pixel |
| | 11 | OSD1 pixel V size equals to 8X of video pixel |
| Reserved | <6> | Reserved |
| OsdEn1 | <7> | OSD1 enable |
| | 0 | Disable OSD1 |
| | 1 | Enable OSD1 |
| <hr/> | | |
| 85 | OSD1 ROM Start Address (R/W) [ROMSTARTADDR1] | |
| RomStAddr1H | <7:0> | Bits<11:4> of OSD1 ROM start address (Unit: 16 bytes) |
| <hr/> | | |
| 86 | OSD1 Font Address Unit (R/W) [FONTADDRUNIT1] | |
| RomStAddr1L | <3:0> | Bits<3:0> OSD1 ROM start address (Unit: 16 bytes) |
| FontAddrUnit1 | <7:4> | OSD1 font address unit (n), font address is multiple of 2(n+5) bytes, max. is 216 |
| <hr/> | | |
| 90 | OSD1 Horizontal Start (R/W) [OSDHSTART1] | |
| OsdHStart1 | <7:0> | On Screen Display horizontal start position (Unit: 8 video pixels) |
| <hr/> | | |
| 91 | OSD1 Vertical Start (R/W) [OSDVSTART1] | |
| OsdVStart1 | <7:0> | On Screen Display vertical start position (Unit: 4 video lines) |
| <hr/> | | |
| 92 | OSD1 RAM Start Address (R/W) [RAMADDRST1] | |
| RamAddrSt1 | <7:0> | OSD1 RAM start address (Unit: 8 bytes) |
| <hr/> | | |
| 8B | OSD1 RAM Horizontal Stride MSB (R/W) [RAMSTRIDE1] | |
| RamStride1H | <1:0> | Bits <9:8> of OSD1 RAM line stride (Unit: 1 bytes) |
| Reserved | <7:2> | Reserved |
| <hr/> | | |
| 93 | OSD1 RAM Horizontal Stride LSB (R/W) [RAMSTRIDE1] | |
| RamStride1L | <7:0> | Bits<7:0> of OSD1 RAM line stride(Unit: 1 bytes) |

| | | | |
|----|---|-------|---|
| 94 | OSD1 Bitmap Horizontal Size LSB (R/W) [BMAPHSIZE1] | | |
| | BmapHSize1L | <7:0> | Bits<7:0> of OSD1 horizontal bitmap size (Unit: 1 OSD pixel) |
| 95 | OSD1 Bitmap Horizontal Size MSB (R/W) [BMAPHSIZE1] | | |
| | BmapHSize1H | <1:0> | Bits<9:8> of OSD1 bitmap horizontal size |
| | Reserved | <7:2> | Reserved |
| 96 | OSD1 Bitmap Horizontal Total Pixels LSB (R/W) [BMAPHTOTAL1] | | |
| | BmapHTotal1L | <7:0> | Bits<7:0> of OSD1 bitmap horizontal total (Unit: 1 OSD pixel) |
| 97 | OSD1 Bitmap Horizontal Total Pixels MSB (R/W) [BMAPHTOTAL1] | | |
| | BmapHTotal1H | <1:0> | Bits<9:8> of OSD1 bitmap horizontal total |
| | Reserved | <7:2> | Reserved |
| 98 | OSD1 Bitmap Vertical Size LSB (R/W) [BMAPVSIZE1] | | |
| | BmapVSize1L | <7:0> | Bits<7:0> of OSD1 bitmap vertical size (Unit: 1 OSD line) |
| 99 | OSD1 Bitmap Vertical Size MSB (R/W) [BMAPVSIZE1] | | |
| | BmapVSize1H | <1:0> | Bits<9:8> of OSD1 bitmap vertical size |
| | Reserved | <7:2> | Reserved |
| 9A | OSD1 Bitmap Vertical total Lines LSB (R/W) [BMAPVTOTAL1] | | |
| | BmapVTotal1L | <7:0> | Bits<7:0> of OSD1 bitmap vertical total (Unit: 1 OSD line) |
| 9B | OSD1 Bitmap Vertical Total Lines MSB (R/W) [BMAPVTOTAL1] | | |
| | BmapVTotal1H | <1:0> | Bits<9:8> of OSD1 bitmap vertical total |
| | Reserved | <7:2> | Reserved |
| 9C | OSD1 Icon Horizontal Total (R/W) [ICONHTOTAL1] | | |
| | IconHtotal1 | <7:0> | OSD1 horizontal icon total (Unit: 1 icon) |
| 9D | OSD1 Icon Vertical Total (R/W) [ICONVTOTAL1] | | |
| | IconVTotal1 | <7:0> | OSD1 vertical icon total (Unit: 1 icon) |

AE OSD1 Font Line Size (R/W) [FONTLINESIZE1]

Fontlinesize1 <7:0> memory size of a line of font (Unit: 1 byte)

VII. OSD 2 Registers

88 OSD2 Control (R/W) [OSDCONTROL2]

| | | |
|-----------|-------|--|
| PixDepth2 | <0> | Number of bits per pixel of OSD2 |
| | 0 | One bit per pixel |
| | 1 | Two bits per pixel |
| BlinkEn2 | <1> | OSD2 blinking enable, effective when RomMode = '1' |
| | 0 | Disable blinking |
| | 1 | Enable blinking |
| Hzoom2 | <3:2> | OSD2 horizontal zoom factor |
| | 00 | OSD pixel H size equals to 1X of video pixel |
| | 01 | OSD pixel H size equals to 2X of video pixel |
| | 10 | OSD pixel H size equals to 4X of video pixel |
| | 11 | OSD pixel H size equals to 8X of video pixel |
| Vzoom2 | <5:4> | OSD2 vertical zoom factor |
| | 00 | OSD pixel V size equals to 1X of video pixel |
| | 01 | OSD pixel V size equals to 2X of video pixel |
| | 10 | OSD pixel V size equals to 4X of video pixel |
| | 11 | OSD pixel V size equals to 8X of video pixel |
| Reserved | <6> | Reserved |
| OsdEn2 | <7> | OSD2 enable |
| | 0 | Disable OSD2 |
| | 1 | Enable OSD2 |

89 OSD2 ROM Start Address (R/W) [ROMSTARTADDR2]

RomStAddr1H <7:0> Bits<11:4> of OSD2 ROM start address (Unit: 16 bytes)

8A OSD2 Font Address Unit (R/W) [FONTADDRUNIT2]

| | | |
|---------------|-------|---|
| RomStAddr2L | <3:0> | Bits<3:0> OSD2 ROM start address (Unit: 16 bytes) |
| FontAddrUnit2 | <7:4> | OSD1 font address unit (n), font address is multiple of 2(n+5) bytes, max. is 216 |

| | |
|--------------|--|
| A0 | OSD2 Horizontal Start (R/W) [OSDHSTART2] |
| OsdHStart2 | <7:0> On Screen Display horizontal start position (Unit: 8 video pixels) |
| A1 | OSD2 Vertical Start (R/W) [OSDVSTART1] |
| OsdVStart2 | <7:0> On Screen Display vertical start position (Unit: 4 video lines) |
| A2 | OSD2 RAM Start Address (R/W) [RAMADDRST2] |
| RamAddrSt2 | <7:0> OSD2 RAM start address (Unit: 8 bytes) |
| 8C | OSD2 RAM Horizontal Stride MSB (R/W) [RAMSTRIDE2] |
| RamStride2H | <1:0> Bits <9:8> of OSD2 RAM line stride (Unit: 1 bytes) |
| Reserved | <7:2> Reserved |
| A3 | OSD2 RAM Horizontal Stride LSB (R/W) [RAMSTRIDE2] |
| RamStride2L | <7:0> Bits<7:0> of OSD2 RAM line stride (Unit: 1 bytes) |
| A4 | OSD2 Bitmap Horizontal Size LSB (R/W) [BMAPHSIZE2] |
| BmapHSize2L | <7:0> Bits<7:0> of OSD1 horizontal bitmap size (Unit: 1 OSD pixel) |
| A5 | OSD2 Bitmap Horizontal Size MSB (R/W) [BMAPHSIZE2] |
| BmapHSize2H | <1:0> Bits<9:8> of OSD1 bitmap horizontal size |
| Reserved | <7:2> Reserved |
| A6 | OSD2 Bitmap Horizontal Total Pixels LSB (R/W) [BMAPHTOTAL2] |
| BmapHTotal2L | <7:0> Bits<7:0> of OSD2 bitmap horizontal total (Unit: 1 OSD pixel) |
| A7 | OSD2 Bitmap Horizontal Total Pixels MSB (R/W) [BMAPHTOTAL2] |
| BmapHTotal2H | <1:0> Bits<9:8> of OSD2 bitmap horizontal total |
| Reserved | <7:2> Reserved |
| A8 | OSD2 Bitmap Vertical Size LSB (R/W) [BMAPVSIZE2] |
| BmapVSize2L | <7:0> Bits<7:0> of OSD2 bitmap vertical size (Unit: 1 OSD line) |

| | |
|---------------|---|
| A9 | OSD2 Bitmap Vertical Size MSB (R/W) [BMAPVSIZE2] |
| BmapVSize2H | <1:0> Bits<9:8> of OSD2 bitmap vertical size |
| Reserved | <7:2> Reserved |
| AA | OSD2 Bitmap Vertical total Lines LSB (R/W) [BMAPVTOTAL2] |
| BmapVTotal2L | <7:0> Bits<7:0> of OSD2 bitmap vertical total(Unit: 1 OSD line) |
| AB | OSD2 Bitmap Vertical Total Lines MSB (R/W) [BMAPVTOTAL2] |
| BmapVTotal2H | <1:0> Bits<9:8> of OSD2 bitmap vertical total |
| Reserved | <7:2> Reserved |
| AC | OSD2 Icon Horizontal Total (R/W) [ICONHTOTAL2] |
| IconHtotal2 | <7:0> OSD2 horizontal icon total (Unit: 1 icon) |
| AD | OSD2 Icon Vertical Total (R/W) [ICONVTOTAL2] |
| IconVTotal2 | <7:0> OSD2 vertical icon total (Unit: 1 icon) |
| AF | OSD2 Font Line Size (R/W) [FONTLINESIZE2] |
| Fontlinesize2 | <7:0> memory size of a line of font (Unit: 1 byte) |

VIII. Desktop Color Registers

| | |
|----------------|--|
| B3 | Desktop Color Component Red (R/W) [DESKR] |
| DeskColorRed | <7:0> Desktop color red |
| B4 | Desktop Color Component Green (R/W) [DESKG] |
| DeskColorGreen | <7:0> Desktop color green |
| B5 | Desktop Color Component Blue (R/W) [DESKB] |
| DeskColorBlue | <7:0> Desktop color blue |

IX. Film Detection/Motion Adaptive Registers

| | |
|-----------|--|
| C4 | Motion Pixels Threshold LSB (R/W) [MOTIONCNTTH] |
|-----------|--|

| | | | |
|-----------|--|-------|--|
| | MvCntThL | <7:0> | Bit<7:0> of motion counter threshold |
| <hr/> | | | |
| C5 | Motion Pixels Threshold MSB (R/W) [MOTIONCNTTH] | | |
| | MvCntThH | <7:0> | Bit<15:8> of motion counter threshold |
| <hr/> | | | |
| C6 | Lumina(Y) Threshold (R/W) [LUMATH] | | |
| | YThL | <6:0> | Y threshold for film & motion compensation |
| | Reserved | <7> | Reserved |
| <hr/> | | | |
| C7 | Chroma(C) Threshold (R/W) [CHROMATH] | | |
| | CThH | <6:0> | C threshold for film & motion compensation |
| | Reserved | <7> | Reserved |
| <hr/> | | | |
| C8 | De-interlacing Control Register(R/W) [MCCTRL] | | |
| | MCEn | <0> | Motion Compensation Enable |
| | | 0 | Field Merge De-interlace Mode |
| | | 1 | Motion Adaptive De-interlace Mode |
| | MvMode | <1> | Motion Estimation Type |
| | | 0 | Y/C Comparison |
| | | 1 | Y Comparison Only |
| | Reserved | <2> | Reserved |
| | TestMv | <3> | Display Motion Part |
| | Reserved | <7:4> | Reserved |
| <hr/> | | | |
| C9 | Film Detection Control Register(R/W) [FILMCTRL] | | |
| | FilmDetEn | <0> | Film detection enable |
| | | 0 | Disable |
| | | 1 | Enable |
| | ResetType | <1> | Non-Film Detection Type |
| | | 0 | H/W Auto Detection |
| | | 1 | S/W Reset to Non-Film after Film Detected |
| | FilmReset | <2> | Reset Film Detection, depending on bit1 |
| | | 0 | Disable Reset |
| | | 1 | Reset when bit 1 is turn on |

| | | |
|----------|-------|---------------------------------|
| Reserved | <3> | Reserved |
| PdMatch | <7:4> | Number of film sequence matched |

CE Motion Pixel Numbers LSB (R) [MVCNT]

| | | |
|----------|-------|--|
| MvCountL | <7:0> | Bit<7:0> of pixels numbers of difference between 2-field/frame |
|----------|-------|--|

CF Motion Pixel Numbers MSB (R) [MVCNT]

| | | |
|----------|-------|---|
| MvCountH | <7:0> | Bit<15:8> of pixels numbers of difference between 2-field/frame |
|----------|-------|---|

X. Keystone/Sharpness Registers

CB Keyston/Sharpness Control Register(R/W) [SHPKEYCTRL]

| | | |
|-----------|-----|-------------------------------------|
| ShapEn | <0> | Sharpness enable |
| | | 0 Disable |
| | | 1 Enable |
| KeyEn | <4> | Keystone enable |
| | | 0 Disable |
| | | 1 Enable |
| Interlace | <5> | Interlace output enable |
| EvenField | <6> | Even field mode |
| TriLevel | <7> | Tri level analog data output enable |

C0 Keystone Parameters Address LSB (R/W) [KEYADDR]

| | | |
|----------|-------|-----------------------------------|
| KeyAddrL | <7:0> | Bit<7:0> of keystone FIFO address |
|----------|-------|-----------------------------------|

C1 Keystone Parameters Address MSB (R/W) [KEYADDR]

| | | |
|------------|-------|------------------------------------|
| KeyAddrH | <3:0> | Bit<11:8> of keystone FIFO address |
| Reserved | <6:4> | Reserved |
| KeyWriteEn | <7> | Keystone fifo write enable |
| | | 0 Disable |
| | | 1 Enable |

Note: Keystone parameter for each scan line is stored into 1280x32 SRAM inside AL310. KeyAddr is the address of read/write pointer of this SRAM.

XI. Tri-Level Sync Registers

| | | | |
|-----------|---|--|--|
| D0 | Tri Level Sync Parameter (W) [TRISYNCA] | | |
| PeriodA | <7:0> | Tri level sync parameter Period_a | |
| D1 | Tri Level Sync Parameter (W) [TRISYNCB] | | |
| PeriodB | <7:0> | Tri level sync parameter Period_a | |
| D2 | Tri Level Sync Parameter (W) [TRISYNCD1] | | |
| Delta1 | <6:0> | Bit<6> is sign bit ex. 60h means from blank_level , - 32 every unit | |
| Reserved | <7> | Reserved | |
| D3 | Tri Level Sync Parameter (W) [TRISYNCD2] | | |
| Delta2 | <6:0> | Bit<6> is sign bit ex. 20h means from sync_level, + 32 every unit | |
| Reserved | <7> | Reserved | |
| D4 | Tri Level Sync Parameter (W) [TRISYNBLANK] | | |
| BlankData | <7:0> | Data of blanking period | |
| D7 | Tri Level Sync Parameter (W) [TRISYNCLEVEL] | | |
| SyncLevel | <7:0> | Sync level value | |

XIII. Display Parameter Registers

| | | | |
|------------|--|---|--|
| C2 | Tune Display Horizontal Sync Phase (R/W) [DISTUNEHS] | | |
| DisHsDelay | <4:0> | Output horizontal sync delay (Unit: 1 oclk) | |
| CC | Tune Display Pixel Clock Phase (R/W) [DISTUNESCLK] | | |
| TuneSclk | <2:0> | Phase delay number(8 steps) | |
| | <4:3> | Phase delay types | |
| | 00 | Sclk | |

| | | | |
|----------|-------|----|-----------------------------|
| | | 01 | Sclk + delay phase |
| | | 10 | Inversed Sclk |
| | | 11 | Inversed Sclk + delay phase |
| Reserved | <7:5> | | Reserved |

CA Phase Detection Control Register(R/W) [PHASECTRL]

| | | | |
|-----------|-------|----|---------------------------|
| PhaseEn | <0> | | Phase detection Enable |
| | | 0 | Disable |
| | | 1 | Enable |
| PhaseMode | <2:1> | | Phase detection precision |
| | | 00 | 8-bit comparison |
| | | 01 | 7-bit comparison |
| | | 10 | 6-bit comparison |
| | | 11 | 5-bit comparison |
| Reserved | <7:3> | | Tie to "00110" |

D7 Display Horizontal Total Counter LSB (R) [DISHTOTALCNT]

| | | | |
|------------|-------|--|--|
| HTotalCntL | <7:0> | | Bit<7:0> of display horizontal total count |
|------------|-------|--|--|

D8 Display Horizontal Total Counter MSB (R) [DISHTOTALCNT]

| | | | |
|------------|-------|--|---|
| HTotalCntH | <2:0> | | Bit<10:8> of display horizontal total count |
| Reserved | <7:3> | | Reserved |

D9 Display Vertical Total Counter LSB (R) [DISVTOTALCNT]

| | | | |
|----------|-------|--|--|
| VTotCntL | <7:0> | | Bit<7:0> of display vertical total count |
|----------|-------|--|--|

DA Display Vertical Total Counter MSB (R) [DISVTOTALCNT]

| | | | |
|----------|-------|--|---|
| VTotCntH | <2:0> | | Bit<10:8> of display vertical total count |
| Reserved | <7:3> | | Reserved |

DB Phase Counter LSB (R) [PHASECNT]

| | | | |
|-----------|-------|--|-------------------------------|
| PhaseCntL | <7:0> | | Bit<7:0> of phase count value |
|-----------|-------|--|-------------------------------|

DC Phase Counter MSB (R) [PHASECNT]

| | | |
|-----------|-------|--------------------------------|
| PhaseCntH | <4:0> | Bit<12:8> of phase count value |
| Reserved | <7:5> | Reserved |

F0 **Enable Brightness/Contrast/Saturation (W) [DISADJEN]**

| | | |
|------------|-------|---------------------------------------|
| PanelAdjEn | <0> | Enable brightness/contrast/saturation |
| Reserved | <7:1> | Reserved |

F1 **Brightness Value (W) [BRIGHTNESS]**

| | | |
|------------|-------|---------------------------------|
| Brightness | <7:0> | Brightness value, Default: "80" |
|------------|-------|---------------------------------|

F2 **Contrast Value (W) [CONTRAST]**

| | | |
|----------|-------|-------------------------------|
| Contrast | <7:0> | Contrast value, Default: "40" |
|----------|-------|-------------------------------|

F3 **Saturation Value (W) [SATURATION]**

| | | |
|------------|-------|---------------------------------|
| Saturation | <7:0> | Saturation value, Default: "40" |
|------------|-------|---------------------------------|

10 Electrical Characteristics

10.1 Absolute Maximum Ratings

(Excessive ratings are harmful to the lifetime. Only for user guidelines, not tested.)

| Parameter | | 3.3V Rating | Unit |
|-------------------|---|--------------------------------|------|
| V _{DD} | Supply Voltage | -0.3 ~ +3.8 | V |
| V _P | Input Pin Voltage | -0.3 ~ +(V _{DD} +0.3) | V |
| I _O | Output Current | -20 ~ +20 | mA |
| T _{AMB} | Ambient Op. Temperature | 0 ~ +85 | °C |
| T _{stg} | Storage Temperature | -40 ~ +125 | °C |
| T _{VSOL} | Vapor Phase Soldering Temperature (15 Sec.) | 220 | °C |

10.2 Recommended Operating Conditions

| Parameter | | 3.3V Rating | | | Unit |
|------------------|--------------------------|---------------------|---------|---------------------|------|
| | | Min. | Typical | Max. | |
| V _{DD} | Supply Voltage | +3.0 | +3.3 | +3.6 | V |
| V _{IH} | High Level Input Voltage | 0.7 V _{DD} | | V _{DD} | V |
| V _{IL} | Low Level Input Voltage | 0 | | 0.3 V _{DD} | V |
| T _{AMB} | Ambient Op. Temperature | 0 | | +70 | °C |

10.3 DC Characteristics

(V_{DD} = 3.3V, V_{SS}=0V. T_{AMB} = 0 to 70°C; Some parameters are guaranteed by design only, not production tested)

| Parameter | | 3.3V Rating | | | Unit |
|-----------|--|-------------|---------|------|------|
| | | Min. | Typical | Max. | |

| Parameter | | 3.3V Rating | | | Unit |
|-----------|-------------------------|--------------|---------|--------------|---------|
| | | Min. | Typical | Max. | |
| V_{IH} | Hi-level Input Voltage | $0.7 V_{DD}$ | - | V_{DD} | V |
| V_{IL} | Lo-level Input Voltage | 0 | | $0.3 V_{DD}$ | V |
| V_{OH} | Hi-level Output Voltage | 2.4 | - | V_{DD} | V |
| V_{OL} | Lo-level Output Voltage | - | - | +0.4 | V |
| I_{LI} | Input Leakage Current | -5 | - | +5 | μA |
| I_{LO} | Output Leakage Current | -5 | - | +5 | μA |

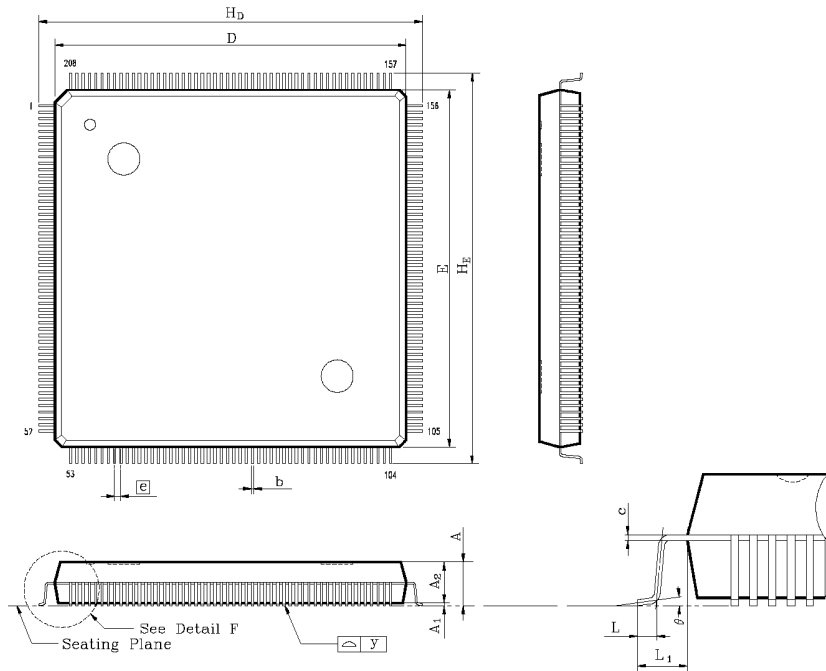
10.4 AC Characteristics

($V_{DD} = 3.3V$, $V_{SS} = 0V$, $T_{AMB} = 0$ to $70^{\circ}C$; Some parameters are guaranteed by design only, not production tested)

11 Timing Diagrams

TBD.

12 Mechanical Drawing- PQFP-208



| Symbol | Dimension in inch | | | Dimension in mm | | |
|----------------------|-------------------|-------|-------|-----------------|--------------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.136 | 0.144 | 0.152 | 3.45 | 3.65 | 3.85 |
| A₁ | 0.004 | 0.010 | 0.036 | 0.10 | 0.25 | 0.91 |
| A₂ | 0.119 | 0.128 | 0.136 | 3.02 | 3.24 | 3.46 |
| b | 0.004 | 0.008 | 0.012 | 0.10 | 0.20 | 0.30 |
| c | 0.002 | 0.006 | 0.010 | 0.04 | 0.15 | 0.26 |
| D | 1.093 | 1.102 | 1.112 | 27.75 | 28.00 | 28.25 |
| E | 1.093 | 1.102 | 1.112 | 27.75 | 28.00 | 28.25 |
| e | 0.012 | 0.020 | 0.031 | 0.30 | 0.50 | 0.80 |
| H_b | 1.169 | 1.205 | 1.240 | 29.70 | 30.60 | 31.50 |
| H_e | 1.169 | 1.205 | 1.240 | 29.70 | 30.60 | 31.50 |
| L | 0.010 | 0.020 | 0.030 | 0.25 | 0.50 | 0.75 |
| L₁ | 0.041 | 0.051 | 0.061 | 1.05 | 1.30 | 1.55 |
| y | - | - | 0.004 | - | - | 0.10 |
| θ | 0° | - | 12° | 0° | - | 12° |

Note:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

| | | | |
|--|--|----------|---|
| TITLE : 208L QFP (28x28 mm**2) FOOTPRINT 2.6mm | | | |
| PACKAGE OUTLINE DRAWING | | | |
| LEADFRAME MATERIAL: | | | |
| APPROVE | | DOC. NO. | |
| | | VERSION | 1 |
| | | PAGE | |
| CHECK | | DWG. NO. | |
| | | DATE | |

CONTACT INFORMATION

Averlogic Technologies Corp.
4F, No. 514, Sec. 2, Cheng Kung Rd., Nei-Hu Dist., Taipei, Taiwan
Tel: +886 2-27915050
Fax: +886 2-27912132
E-mail: sales@averlogic.com.tw
URL: <http://www.averlogic.com.tw>

Averlogic Technologies, Inc.
90 Great Oaks Blvd. #204, San Jose, CA 95119, U.S.A.
Tel: 1 408 361-0400
Fax: 1 408 361-0404
E-mail: sales@averlogic.com
URL: <http://www.averlogic.com>