ADVANCED
LINEAR
DEVICES, INC.

DUAL EPAD™ OPERATIONAL AMPLIFIER

KEY FEATURES

- **5V single supply operation**
- **EPAD (Electrically Programmable Analog Device)**
- **User programmable V_{OS} trimmer**
- **Computer-assisted trimming**
- **Rail-to-rail input/output**
- **Compatible with standard EPAD Programmer**
- **Each amplifier V_{OS} can be trimmed to a different Vos level**
- **High precision through in-system circuit trimming**
- **Reduces or eliminates V_{OS}, PSRR, CMRR and TCV_{OS} errors**
- **System level "calibration" capability**
- **Application Specific Programming mode**
- **In-System Programming mode**
- **Electrically programmable to compensate for external component tolerances**
- **Achieves 0.01pA input bias current and 25µV input offset voltage**

GENERAL DESCRIPTION

The ALD2722E/ALD2722 is a dual monolithic rail-to-rail precision CMOS operational amplifier with integrated user programmable EPAD (Electrically Programmable Analog Device) based offset voltage adjustment. The ALD2722E/ALD2722 is a dual version of the ALD1722E/ALD1722 operational amplifier. Each ALD2722E/ALD2722 operational amplifier features individual, user-programmable offset voltage trimming resulting in significantly enhanced total system performance and user flexibility. EPAD technology is an exclusive ALD design which has been refined for analog applications where precision voltage trimming is necessary to achieve a desired performance. It utilizes CMOS FETs as in-circuit elements for trimming of offset voltage bias characteristics with the aid of a personal computer under software control. Once programmed, the set parameters are stored indefinitely. EPAD offers the circuit designer a convenient and cost-effective trimming solution for achieving the very highest amplifier/ system performance.

The ALD2722E/ALD2722 dual operational amplifier features rail-to-rail input and output voltage ranges, tolerance to overvoltage input spikes of 300mV beyond supply rails, high capacitive loading up to 4000pF, extremely low input currents of 0.01pA typical, high open loop voltage gain, useful bandwidth of 1.5MHz, slew rate of 1.9V/µs, and low typical supply current of 2mA for both amplifiers.

ORDERING INFORMATION

Operating Temperature Range		
-55°C to +125°C	0°C to +70°C	0°C to +70°C
14-Pin CERDIP Package	14-Pin Small Outline Package (SOIC)	14-Pin Plastic Dip Package
ALD2722E DB ALD2722 DB	ALD2722E SB ALD2722 SB	ALD2722E PB ALD2722 PB

* Contact factory for industrial temperature range

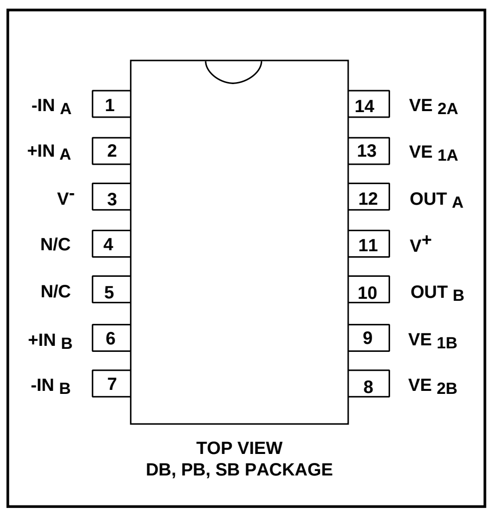
BENEFITS

- Eliminates manual and elaborate system trimming procedures
- Remote controlled automated trimming
- In-System Programming capability
- No external components
- No internal clocking noise source
- Simple and cost effective
- Small package size
- Extremely small total functional volume size
- Low system implementation cost
- Micropower

APPLICATIONS

- Sensor interface circuits
- Transducer biasing circuits
- Capacitive and charge integration circuits
- Biochemical probe interface
- Signal conditioning
- Portable instruments
- High source impedance electrode amplifiers
- Precision Sample and Hold amplifiers
- Precision current to voltage converter
- Error correction circuits
- Sensor compensation circuits
- Precision gain amplifiers
- Periodic In-system calibration
- System output level shifter

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The ALD2722E/ALD2722 utilizes EPADs as in-circuit elements for trimming of offset voltage bias characteristics. Each ALD2722E/ALD2722 operational amplifier has a pair of EPAD-based circuits connected such that one circuit is used to adjust V_{OS} in one direction and the other circuit is used to adjust V_{OS} in the other direction. While each of the basic EPAD device is a monotonically adjustable (offset voltage trimming) programmable device, the V_{OS} of the ALD2722E can be adjusted many times in both directions. Once programmed, the set V_{OS} levels are stored permanently, even when the device is removed.

Functional Description of ALD2722E

The ALD2722E is pre-programmed at the factory under standard operating conditions for minimum equivalent input offset voltage. It also has a guaranteed offset voltage program range, which is ideal for applications that require electrical offset voltage programming.

The ALD2722E is an operational amplifier that can be trimmed stand-alone, with user application-specific programming or in-system programming conditions. User application-specific circuit programming refers to a situation where the Total Input Offset Voltage of the ALD2722E can be trimmed with the actual intended operating conditions.

Take the example of an application circuit that uses + 5V and -5V power supplies, an operational amplifier input biased at +1V, and an average operating temperature at +85°C; the circuit can be wired up to these conditions within an environmental chamber with the ALD2722E inserted into a test socket while it is being electrically trimmed. Any error in V_{OS} due to these bias conditions can be automatically zeroed out. The Total V_{OS} error, V_{OST}, is now limited only by the adjustable range and the stability of V_{OS}, and the input noise voltage of the operational amplifier. This Total Input Offset Voltage now includes V_{OS}, as V_{OS} is traditionally specified; plus the V_{OS} error contributions from PSRR, CMRR, TCV_{OS}, and noise. Typically, V_{OST} ranges approximately ±25µV for the ALD2722E.

In-System Programming refers to the condition where the EPAD adjustment is made after the ALD2722E has been inserted into a circuit board. In this case, the circuit design must provide for the ALD2722E to operate in both normal mode and in programming mode. One of the benefits of in-system programming is that not only the ALD2722E offset voltage from operating bias conditions has been accounted for, any residual errors introduced by other circuit components, such as resistor or sensor induced voltage errors, can also be programmed and corrected. In this way, the "in-system" circuit output can be adjusted to a desired level eliminating need for another trimming function.

Functional Description of ALD2722

The ALD2722 is pre-programmed at the factory under standard operating conditions for minimum equivalent input offset voltage. The ALD2722 offers similar programmable features as the ALD2722E, but with more limited offset voltage program range. It is intended for standard operational amplifier applications where little or no electrical programming by the user is necessary.

USER PROGRAMMABLE V_{OS} FEATURE

Each ALD2722E/ALD2722 has four additional pins, compared to a conventional dual operational amplifier which has eight pins. These four additional pins are named VE1A, VE2A for op amp A and VE1B, VE2B for op amp B. Each of these pins VE1A, VE2A, VE1B, VE2B (represented by VExx) are connected to a separate, internal offset bias circuit. VExx pins have initial internal bias voltage values of approximately 1 to 2 Volts. The voltage on these pins can be programmed using the ALD E100 EPAD Programmer and the appropriate Adapter Module. The useful programming range of voltages on VExx pins are 1 Volt to 4 Volts.

VExx pins are programming pins, used during electrical programming mode to inject charge into the internal EPADs. Increasing voltage on VE1A/VE1B decreases the offset voltage whereas increasing voltage on VE2A/VE2B increases the offset voltage of op amp A and op amp B, respectively. The injected charge is then permanently stored. After programming, VExx pins must be left open in order for these voltages to remain at the programmed levels.

During programming, voltages on VExx pins are increased incrementally to program the offset voltage of the operational amplifier to the desired V_{OS}. Note that desired V_{OS} can be any value within the offset voltage programmable ranges, and can be either equal zero, a positive value or a negative value. This V_{OS} value can also be reprogrammed to a different value at a later time, provided that the useful VE1x or VE2x programming voltage range has not been exceeded. VExx pins can also serve as capacitively coupled input pins.

Internally, VE1 and VE2 are programmed and connected differentially. Temperature drift effects between the two internal offset bias circuits cancel each other and introduce less net temperature drift coefficient change than offset voltage trimming techniques such as offset adjustment with an external trimmer potentiometer.

While programming, V+, VE1 and VE2 pins may be alternately pulsed with 12V (approximately) pulses generated by the EPAD Programmer. In-system programming requires the ALD2722E application circuit to accommodate these programming pulses. This can be accomplished by adding resistors at certain appropriate circuit nodes. For more information, see Application Note AN1700.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V^+		13.2V
Differential input voltage range		-0.3V to V^+ +0.3V
Power dissipation		600 mW
Operating temperature range	PB,SB package	0°C to +70°C
	DB package	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature, 10 seconds		+260°C

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	2722E Min	2722E Typ	2722E Max	2722 Min	2722 Typ	2722 Max	Unit	Test Conditions
Supply Voltage	V_S V^+	±2.0 4.0		±5.0 10.0	±2.0 4.0		±5.0 10.0	V V	 Single Supply
Initial Input Offset Voltage [1]	$V_{OS\,i}$		25	75		40	120	µV	R_S ≤ 100KΩ
Offset Voltage Program Range [2]	ΔV_{OS}	±5	±7		±0.5	±2		mV	
Programmed Input Offset Voltage Error [3]	V_{OS}		25	75		40	120	µV	At user specified target offset voltage
Total Input Offset Voltage [4]	V_{OST}		25	75		40	120	µV	At user specified target offset voltage
Input Offset Current [5]	I_{OS}		0.01	10 240		0.01	10 240	pA pA	T_A = 25°C 0°C ≤ T_A ≤ +70°C
Input Bias Current [5]	I_B		0.01	10 240		0.01	10 240	pA pA	T_A = 25°C 0°C ≤ T_A ≤ +70°C
Input Voltage Range [6]	V_{IR}	-0.3 -2.8		5.3 +2.8	-0.3 -2.8		5.3 +2.8	V V	V^+ = +5V V_S = ±2.5V
Input Resistance	R_{IN}		10^{14}			10^{14}		Ω	
Input Offset Voltage Drift [7]	TCV_{OS}		7			7		µV/°C	R_S ≤ 100KΩ
Initial Power Supply Rejection Ratio [8]	$PSRR_i$		85			85		dB	R_S ≤ 100KΩ
Initial Common Mode Rejection Ratio [8]	$CMRR_i$		90			90		dB	R_S ≤ 100KΩ
Large Signal Voltage Gain	A_V	15 10	100		15 10	100		V/mV V/mV	R_L =10KΩ 0°C ≤ T_A ≤ +70°C
Output Voltage Range	V_O low V_O high	 4.99	0.002 4.998	0.01	 4.99	0.002 4.998	0.01	V V	R_L =1MΩ V =5V 0°C ≤ T_A ≤ +70°C
	V_O low V_O high	 2.40	-2.44 2.44	-2.40	 2.40	-2.44 2.44	-2.40	V V	R_L =10KΩ 0°C ≤ T_A ≤ +70°C
Output Short Circuit Current	I_{SC}		8			8		mA	

* NOTES 1 through 9, see section titled "Definitions and Design Notes".

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)
T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	2722E Min	2722E Typ	2722E Max	2722 Min	2722 Typ	2722 Max	Unit	Test Conditions
Supply Current	I_S		2.0	3.0		2.0	3.0	mA	V_{IN} = 0V No Load
Power Dissipation	P_D		10	15		10	15	mW	V_S = ±2.5V
Input Capacitance	C_{IN}		1			1		pF	
Maximum Load Capacitance	C_L		400 4000			400 4000		pF pF	Gain = 1 Gain = 5
Equivalent Input Noise Voltage	e_n		26			26		nV/√Hz	f = 1KHz
Equivalent Input Noise Current	i_n		0.6			0.6		fA/√Hz	f =10Hz
Bandwidth	B_W		1.5			1.5		MHz	
Slew Rate	S_R		1.9			1.9		V/µs	A_V = +1 R_L = 10KΩ
Rise time	t_r		0.2			0.2		µs	R_L = 10KΩ
Overshoot Factor			10			10		%	R_L=10KΩ C_L=50pF
Settling Time	t_S		3			3		µs	0.1% A_V = -1 R_L = 5KΩ C_L = 50pF
Channel Separation	CS		140			140		dB	A_V = 100

T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	2722E Min	2722E Typ	2722E Max	2722 Min	2722 Typ	2722 Max	Unit	Test Conditions
Average Long Term Input Offset Voltage Stability [9]	$\frac{\Delta V_{OS}}{\Delta \text{time}}$		0.02			0.02		µV/ 1000 hrs	
Initial VE Voltage	$VE1_i$, $VE2_i$		1.4			2.5		V	
Programmable Change of VE Range	ΔVE1, ΔVE2	1.5	2.0			0.5		V	
Programmed VE Voltage Error	e(VE1-VE2)		0.1			0.1		%	
VE Pin Leakage Current	i_{eb}		-5			-5		µA	

* NOTES 1 through 9, see section titled "Definitions and Design Notes".

$V_S = \pm 2.5V$ $-55°C \leq T_A \leq +125°C$ unless otherwise specified

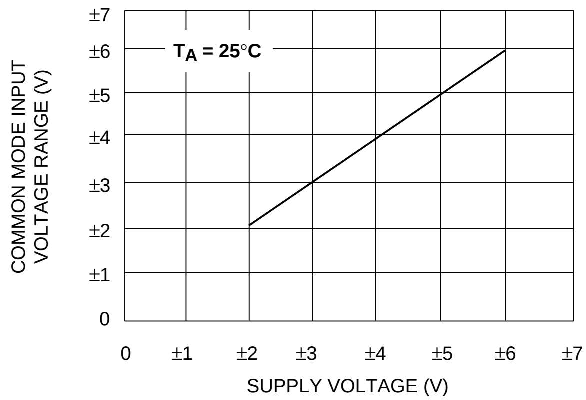
Parameter	Symbol	2722E Min	2722E Typ	2722E Max	2722 Min	2722 Typ	2722 Max	Unit	Test Conditions
Initial Input offset Voltage	$V_{OS\,i}$		0.7			0.7		mV	$R_S \leq 100K\Omega$
Input Offset Current	I_{OS}			2.0			2.0	nA	
Input Bias Current	I_B			2.0			2.0	nA	
Initial Power Supply Rejection Ratio [8]	$PSRR_i$		85			85		dB	$R_S \leq 100K\Omega$
Initial Common Mode Rejection Ratio [8]	$CMRR_i$		97			97		dB	$R_S \leq 100K\Omega$
Large Signal Voltage Gain	A_V	10	25		10	25		V/mV	$R_L = 10K\Omega$
Output Voltage Range	V_O low V_O high	 2.3	-2.4 2.4	-2.3	 2.3	-2.4 2.4	-2.3	V V	 $R_L = 10K\Omega$

$T_A = 25°C$ $V_S = \pm 5.0V$ unless otherwise specified

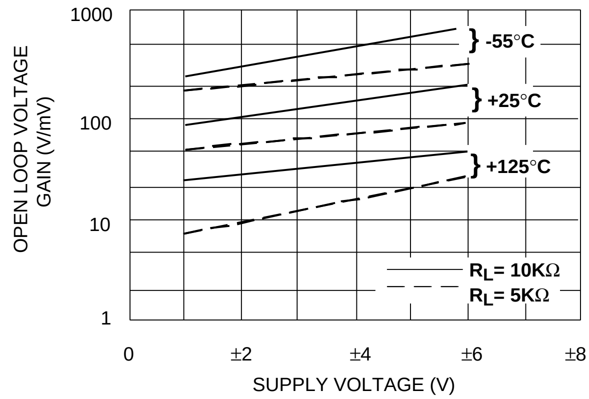
Parameter	Symbol	2722E Min	2722E Typ	2722E Max	2722 Min	2722 Typ	2722 Max	Unit	Test Conditions
Initial Power Supply Rejection Ratio [8]	$PSRR_i$		85			85		dB	$R_S \leq 100K\Omega$
Initial Common Mode Rejection Ratio [8]	$CMRR_i$		97			97		dB	$R_S \leq 100K\Omega$
Large Signal Voltage Gain	A_V		250			250		V/mV	$R_L = 10K\Omega$
Output Voltage Range	V_O low V_O high	 4.8	-4.9 4.9	-4.8	 4.8	-4.9 4.9	-4.8	V	$R_L = 10K\Omega$
Bandwidth	B_W		1.7			1.7		MHz	
Slew Rate	S_R		2.8			2.8		V/µs	$A_V = +1$, $C_L = 50pF$

TYPICAL PERFORMANCE CHARACTERISTICS

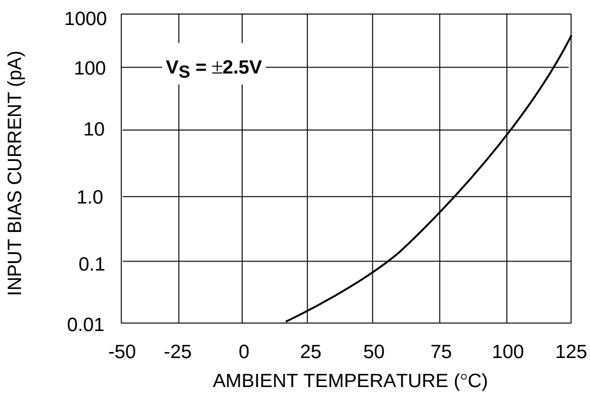
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



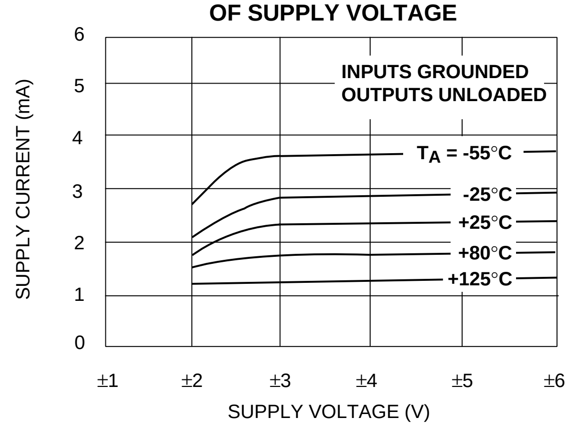
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



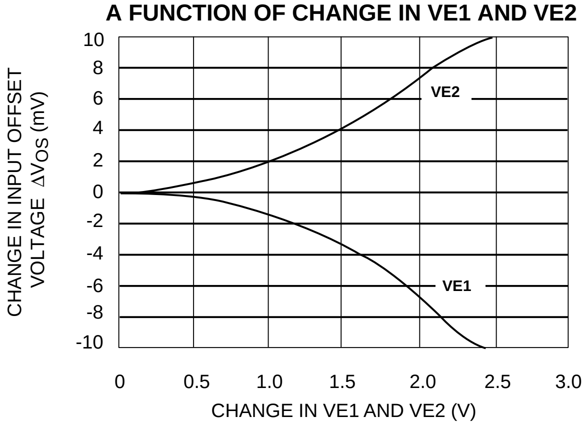
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



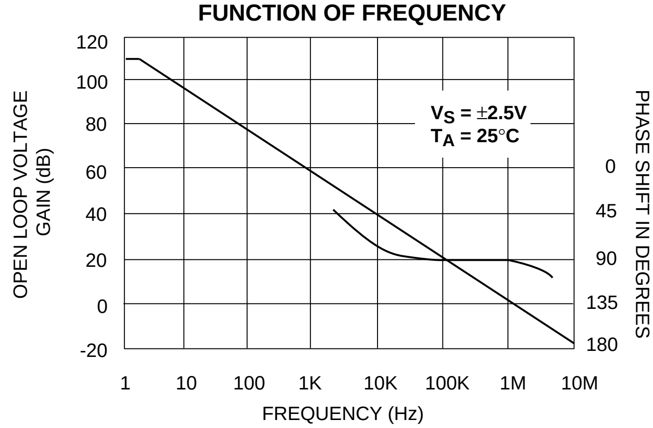
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF CHANGE IN VE1 AND VE2

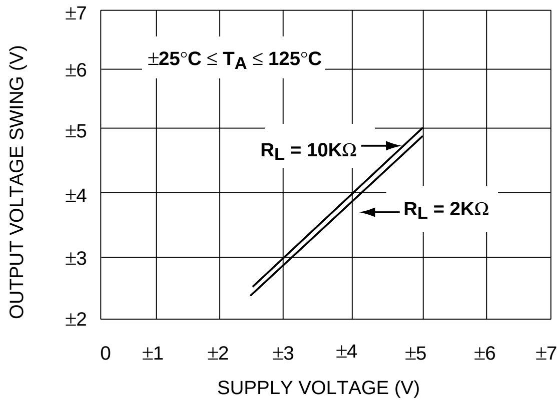


OPEN LOOP VOLTAGE AS A FUNCTION OF FREQUENCY

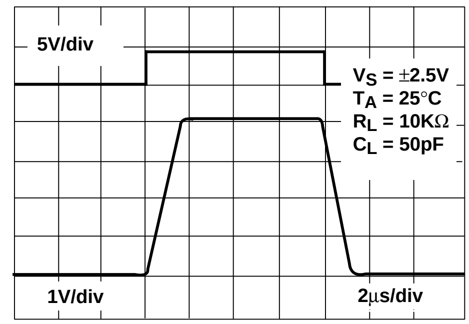


TYPICAL PERFORMANCE CHARACTERISTICS

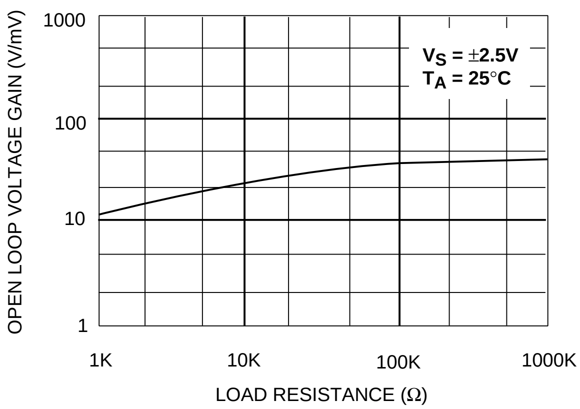
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



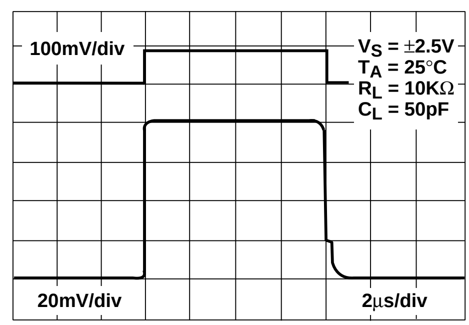
LARGE - SIGNAL TRANSIENT RESPONSE



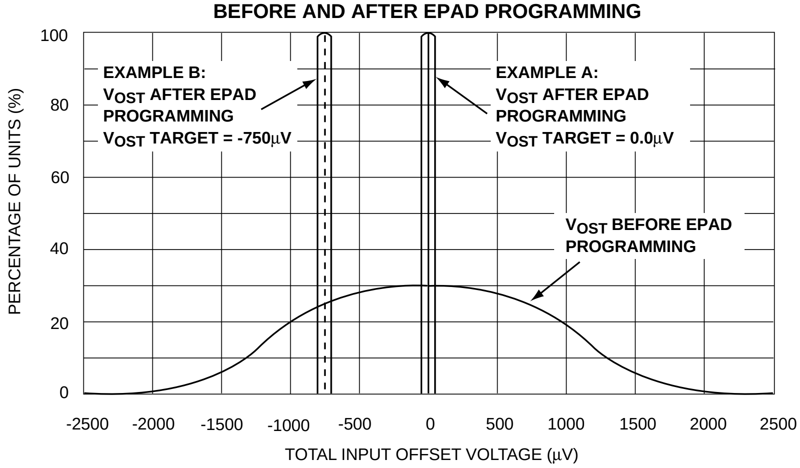
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



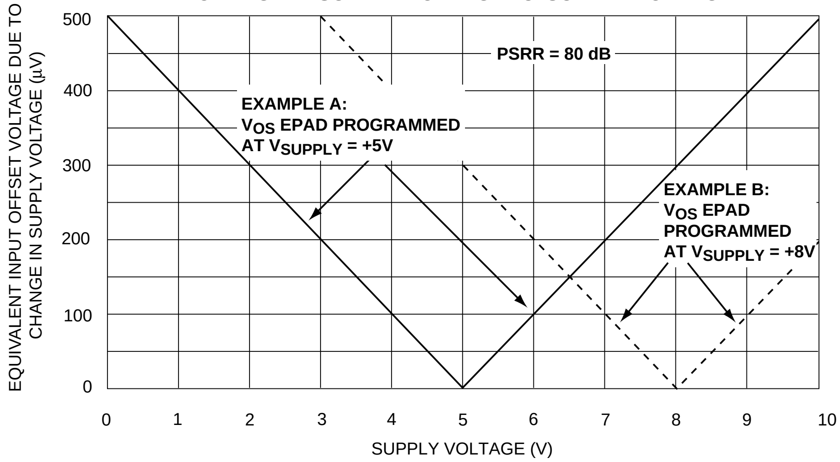
SMALL - SIGNAL TRANSIENT RESPONSE



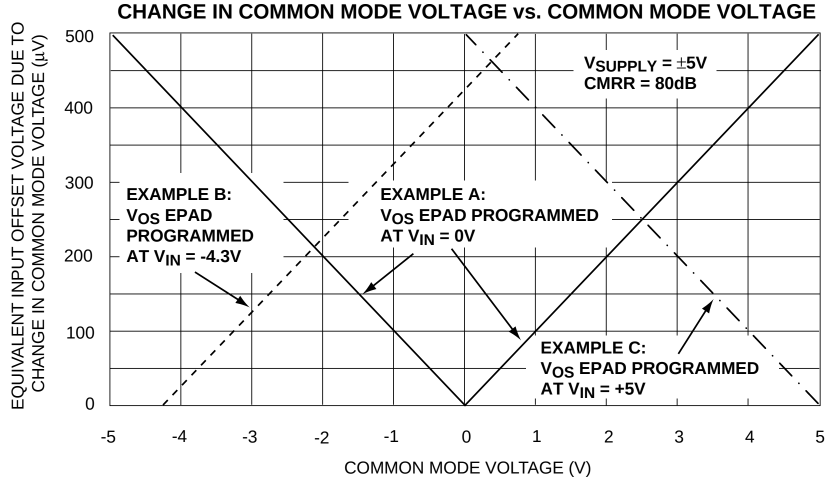
DISTRIBUTION OF TOTAL INPUT OFFSET VOLTAGE BEFORE AND AFTER EPAD PROGRAMMING



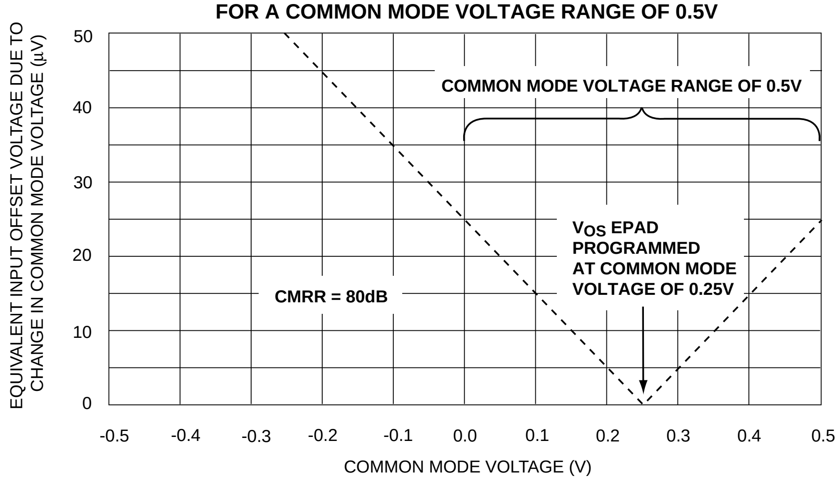
TWO EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN SUPPLY VOLTAGE vs. SUPPLY VOLTAGE



THREE EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN COMMON MODE VOLTAGE vs. COMMON MODE VOLTAGE

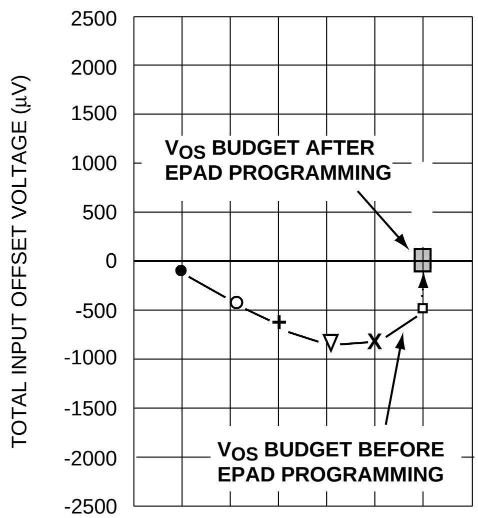


EXAMPLE OF MINIMIZING EQUIVALENT INPUT OFFSET VOLTAGE FOR A COMMON MODE VOLTAGE RANGE OF 0.5V

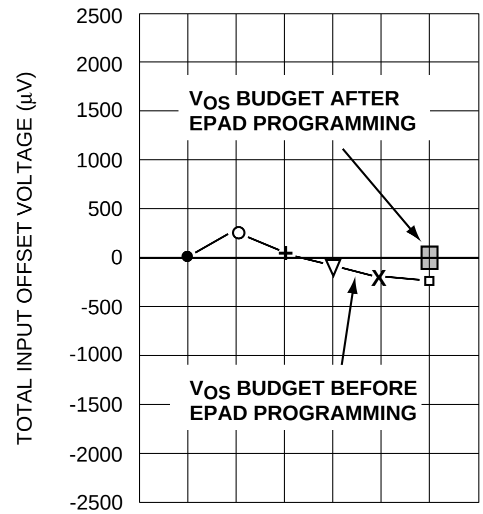


APPLICATION SPECIFIC / IN-SYSTEM PROGRAMMING

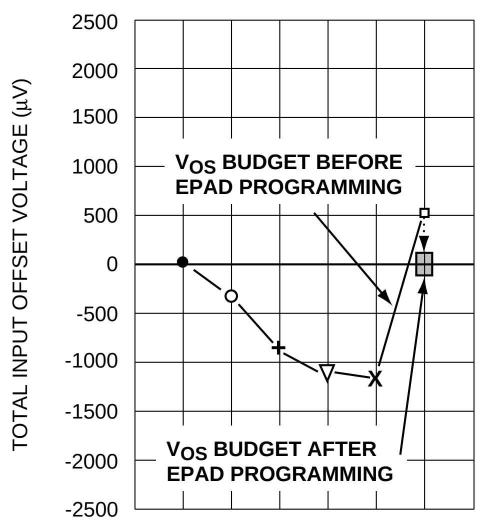
Examples of applications where accumulated total input offset voltage from various contributing sources is minimized under different sets of user-specified operating conditions



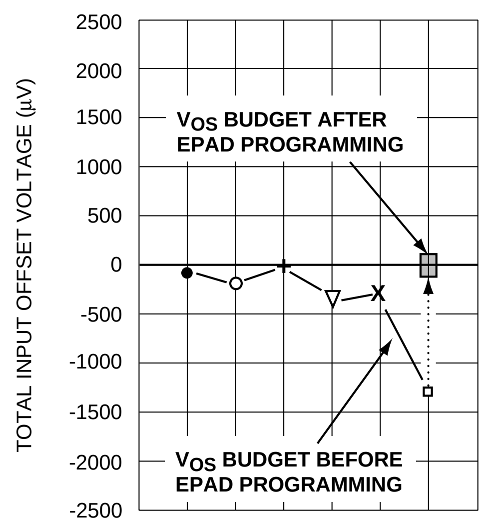
EXAMPLE A



EXAMPLE B



EXAMPLE C



EXAMPLE D

- ● **Device input V_{OS}**
- ○ **PSRR equivalent V_{OS}**
- + **CMRR equivalent V_{OS}**
- ▽ **T_A equivalent V_{OS}**
- X **Noise equivalent V_{OS}**
- ▫ **External Error equivalent V_{OS}**
- ■ **Total Input V_{OS} after EPAD Programming**

DEFINITIONS AND DESIGN NOTES:

1. Initial Input Offset Voltage is the initial offset voltage of the ALD2722E/ALD2722 operational amplifier when shipped from the factory. The device has been pre-programmed and tested for programmability.

2. Offset Voltage Program Range is the range of adjustment of user specified target offset voltage. This is typically an adjustment in either the negative or positive direction of the input offset voltage from an initial input offset voltage. The input offset programming pins, VE1A/VE1B or VE2A/VE2B change the input offset voltages in the negative or positive direction, for each of the amplifier A or B, respectively. User specified target offset voltage can be any offset voltage within this programming range.

3. Programmed Input Offset Voltage Error is the final offset voltage error after programming when the Input Offset Voltage is at target Offset Voltage. This parameter is sample tested.

4. Total Input Offset Voltage is the same as Programmed Input Offset Voltage, corrected for system offset voltage error. Usually this is an all inclusive system offset voltage, which also includes offset voltage contributions from input offset voltage, PSRR, CMRR, TCV_{OS} and noise. It can also include errors introduced by external components, at a system level. Programmed Input Offset Voltage and Total Input Offset Voltage is not necessarily zero offset voltage, but an offset voltage set to compensate for other system errors as well. This parameter is sample tested.

5. The Input Offset and Bias Currents are essentially input protection diode reverse bias leakage currents. This low input bias current assures that the analog signal from the source will not be distorted by it. For applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

6. Input Voltage Range is determined by two parallel complementary input stages that are summed internally, each stage having a separate input offset voltage. While Total Input Offset Voltage can be trimmed to a desired target value, it is essential to note that this trimming occurs at only one user selected input bias voltage. Depending on the selected input bias voltage relative to the power supply voltages, offset voltage trimming may affect one or both input stages. For the ALD2722E/ALD2722, the switching point between the two stages occur at approximately 1.5V above negative supply voltage.

7. Input Offset Voltage Drift is the average change in Total Input Offset Voltage as a function of ambient temperature. This parameter is sample tested.

8. Initial PSRR and initial CMRR specifications are provided as reference information. After programming, error contribution to the offset voltage from PSRR and CMRR is set to zero under the specific power supply and common mode conditions, and becomes part of the Programmed Input Offset Voltage Error.

9. Average Long Term Input Offset Voltage Stability is based on input offset voltage shift through operating life test at 125°C extrapolated to T_A = 25 °C, assuming activation energy of 1.0eV. This parameter is sample tested.

ADDITIONAL DESIGN NOTES:

A. The ALD2722E/ALD2722 is internally compensated for unity gain stability using a novel scheme which produces a single pole role off in the gain characteristics while providing more than 70 degrees of phase margin at unity gain frequency. A unity gain buffer using the ALD2722E/ALD2722 will typically drive 400pF of external load capacitance.

B. The ALD2722E/ALD2722 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail-to-rail input common mode voltage range. The switching point between the two differential stages is 1.5V above negative supply voltage. For applications such as inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), the common mode voltage does not make excursions below this switching point. However, this switching does take place if the operational amplifier is connected as a rail-to-rail unity gain buffer and the design must allow for input offset voltage variations.

C. The output stage consists of class AB complementary output drivers. The oscillation resistant feature, combined with the rail-to-rail input and output feature, makes the ALD2722E/ALD2722 an effective analog signal buffer for high source impedance sensors, transducers, and other circuit networks.

D. The ALD2722E/ALD2722 has static discharge protection. Care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. The user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages not to exceed 0.3V of the power supply voltage levels.

E. VExx are high impedance terminals, as the internal bias currents are set very low to a few microamperes to conserve power. For some applications, these terminals may need to be shielded from external coupling sources. For example, digital signals running nearby may cause unwanted offset voltage fluctuations. Care during the printed circuit board layout to place ground traces around these pins and to isolate them from digital lines will generally eliminate such coupling effects. In addition, optional decoupling capacitors of 1000pF or greater value can be added to VExx terminals.

F. The ALD2722E/ALD2722 is designed for use in low voltage, micropower circuits. The maximum operating voltage during normal operation should remain below 10 Volts at all times. Care should be taken to insure that the application in which the device is used do not experience any positive or negative transient voltages that will cause any of the terminal voltages to exceed this limit.

G. All inputs or unused pins except VExx pins should be connected to a supply voltage such as Ground so that they do not become floating pins, since input impedance at these pins is very high. If any of these pins are left undefined, they may cause unwanted oscillation or intermittent excessive current drain. As these devices are built with CMOS technology, normal operating and storage temperature limits, ESD and latchup handling precautions pertaining to CMOS device handling should be observed.