1.0 General Description

The AMIS-710205-A4 (PI205MC-A4-R) and AMIS-710206-A4 (PI206MC-A4-R) are a family of contact image sensor (CIS) modules. As a family group they are called AMIS-710205/206 modules. They are long contact image sensor modules, using MOS image sensor technology for high-speed performance and high sensitivity. They contain their own complete optical system including the light source; accordingly, they make a very compact imaging system. The four parallel video outputs give this family of CIS modules their high speed performance. They all possess identical electrical circuit components, as well as the same mechanical and optical components, except for their LED light sources. They differ in their specification, however, because the different light sources impact the efficacy of the high speed performance.

The two modules are suitable for scanning A4 size (216mm) documents with eight dots per millimeter (dpm) resolution. Applications include document scanning, mark readers, gaming and office automation equipment.

2.0 Key Features

- Light source, lens and sensor are integrated into a single module
- Ultra high-speed
- Four parallel analog video outputs clocked at 5.0MHz
- 90μsec/line scanning speed @ 5.0MHz clock rate with optional light sources, selected from the option of two above modules
- 8dpm resolution, 216mm scanning length
- Wide dynamic range
- LED light source (selectable among the two above modules)
- Standard A4 size $\cong$ 14mm x 19mm x 232mm
- Low power
- Light weight

3.0 Functional Description

Each of the two modules in the family AMIS-710205/206 consists of four major components. The first of them is the printed circuit board (PCB) on which the 27 imaging chips, AMIS-720233 (PI3033), are bonded. These sensor chips, produced by AMI Semiconductor, are monolithic devices with 64 photo sensing elements. Each of 27 chips are completely self-contained scanning chips with their control circuits integrated within the chips, so that they can be cascaded to provide a 1728 photo-elements module. The AMIS-720233 chips are integrated with the photo sensors' associated multiplex switches, a digital shift register and the chip selection switch. The chip's shift register sequentially clocks out the integrated image charges from each sensing element and passes them through the chip-select switch and out onto the video line. The chip-select switches are sequentially switched as each of the predecessor chips completes its scan. These 27 sensors, bonded on a PCB, are grouped into four sub-cascaded sections. Each contiguously cascaded chip section is connected on separate video lines, providing four video outputs, VOUT1, VOUT2, VOUT3, and VOUT4. Before the signal charges from the four video lines appear at their respective outputs, they are converted to signal voltages by four on-board buffer amplifiers; one for each of its corresponding video section. The first three sections, VOUT1, VOUT2 and VOUT3 have seven sensor chips, while the VOUT4 has six sensor chips. Since each sensor chip has 64 pixels, there are a total of 1728 pixels (see Figure 1).

Mounted in the module housing, along with the PCB, is the second major component. It is a one-to-one graded indexed micro lens array, which focuses the image of the scanned documents onto the sensing line of the sensor chips. The third major component mounted in the module is the LED light source (see Figure 2). This pictorial cross section shows the LED bar light source and its illumination path as it reflects the image from the document and focuses through the ROD lens on to the image sensing line of the sensing chips. All components are housed in a small plastic housing and covered with the fourth major component, a glass window. This cover glass not only serves to protect all of the critical components within the housing from dust, but it also serves a minor role in the optical system. Together with rest of the module's optical system, the module is adjusted to obtain the optimum depth-of-focus.
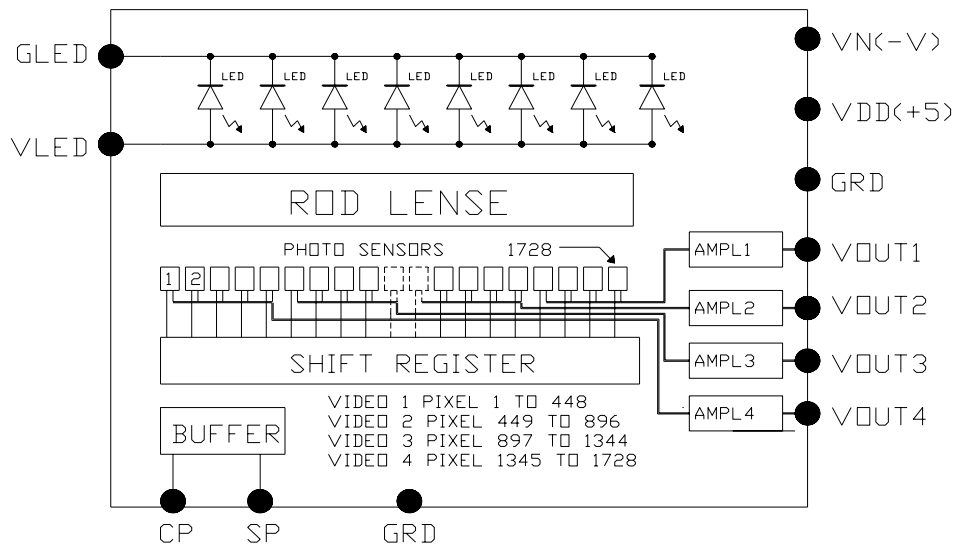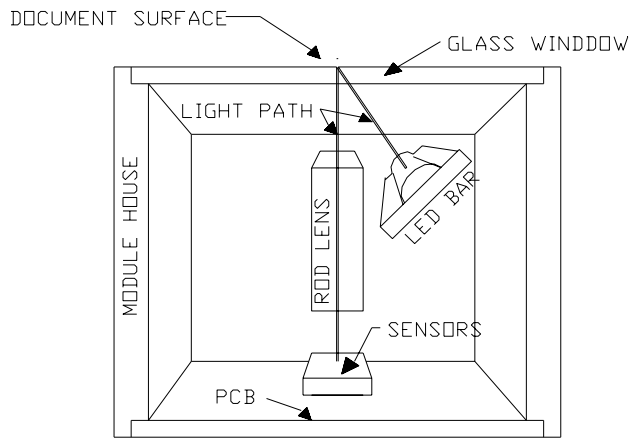
Figure 1: AMIS-710205/206 Module Block Diagram (See Table 1 for Pin Out Designation)

Figure 2: AMIS-710205/206's Cross Section

4.0 I/O Designation

I/O to the module is a 12-pin connector located on one end of the module (see Figure 5). Table 1 lists the pin numbers and their designations for the I/O connector. It is an ECE manufacturer EBW-PK23-P012L2-3Z connector.

Table 1: Pin Configuration

Pin Number	Symbol	Names and Functions
1	VOUT1	Analog video output 1
2	VOUT2	Analog video output 2
3	GND	Ground; 0V
4	VOUT3	Analog video output 3
5	VOUT4	Analog video output 4
6	Vdd	Positive power supply
7	SP (START)	Shift register start pulse
8	GND	Ground; 0V
9	CP (CLOCK)	Sampling clock pulse
10	Vn	Negative power supply
11	GLED	Ground for the light source; 0V
12	VLED	Supply for the light source

5.0 Module vs. LED Light Source

Table 2 lists the module's model and its corresponding LED light source.

Table 2: Module vs. LED Light Source

Module	LED Light Source
AMIS-710205-A4	880nm IR SMD LED bar
AMIS-710206-A4	630nm Red SMD LED bar

6.0 Absolute Maximum Rating

Table 3 shows the absolute maximum ratings. The parameters are common to all the modules. Table 4 shows the absolute maximum ratings that are different among the three modules.

Table 3: Electrical Absolute Maximum Rating

Parameter	Symbols	Maximum Rating	Units
Power supply	Vdd	7	V
	Idd	100	ma
	Vn	-15	V
	In	35	ma
Input clock pulse (high level)	Vih	Vdd – 0.5V	V
Input clock pulse (low level)	Vil	-0.5	V

Note: These parameters are absolute maximums. Do not operate under these conditions.

Table 4: LED Power Absolute Maximum Rating

Parameter	Symbols	Maximum Rating		Units
Power supply: LED light source	Module	AMIS-710205-A4	AMIS-710206-A4	
	VLED	6.0	6.0	V
	ILED	0.6	0.6	A

Note: These parameters are absolute maximums. Do not operate under these conditions.

7.0 Environmental Specifications

Table 5: Operating and Storage Environment

Parameter	Symbols	Range	Units
Operating temperature[1]	Top	0 to 50	°C
Operating humidity[1]	Hop	10 to 90	%
Storage temperature[1]	Tstg	-20 to +75	°C
Storage humidity[1]	Hstg	10 to 90	%

Note:
    (1)   These are standard specifications for the CIS modules.

8.0 Electro-Optical Characteristics (25°C)

Table 6 is the electro-optical characteristics common to all three modules. Table 7 shows the characteristics for each of the two LED light sources.

Table 6: Common Electro-Optical Characteristics

Parameter	Symbol	Value	Units	Notes
Total number of photo detectors		1728	Elements	
Section 1, 2 & 3 number of photo detectors		448	Elements	
Section 4 number of detectors		384	Elements	
Pixel-to-pixel spacing		125	μm	

Table 7: AMIS-710205/206-A4 Electro-Optical Characteristics

	AMIS-710205-A4	IR LED (880nm)		
	AMIS-710206-A4	Red LED (630nm)		
Parameter	**Symbol**	**Value**	**Units**	**Note**
Line scanning rate	Tint[1]	90	μsec	@ 5.0MHz clock frequency
Clock frequency[2]	Fclk	5.0	MHz	
Bright output voltage[3]	Video output	1.0	Volt	
Bright output non-uniformity[4]	Up	<+/-30	%	
Dark non-uniformity[5]	Ud	<40	mV	
Dark output voltage[6]	Dark level (DL)	<200	mV	
Modulation transfer function[7]	MTF	>40	%	

Notes:
    (1)   Tint is the line scanning rate or integration time. Tint is determined by the interval between two start pulses (SP).
    (2)   Fclk: main clock frequency also equals the video sampling frequency.
    (3)   Video output level is controlled with a voltage adjustment as well as the Integration time and the LED light power.
    (4)   Up = {[Vp(max) –Vp(min)]/Vp(max)}x100%
            Where Vp(max) = maximum peak pixel and Vp(min) = minimum pixel.
    (5)   Ud = Vdmax – Vdmin
            Vdmin is the minimum output voltage with the LED off.
            Vdmax is maximum output voltage with the LED on.
    (6)   See Section.9.0.

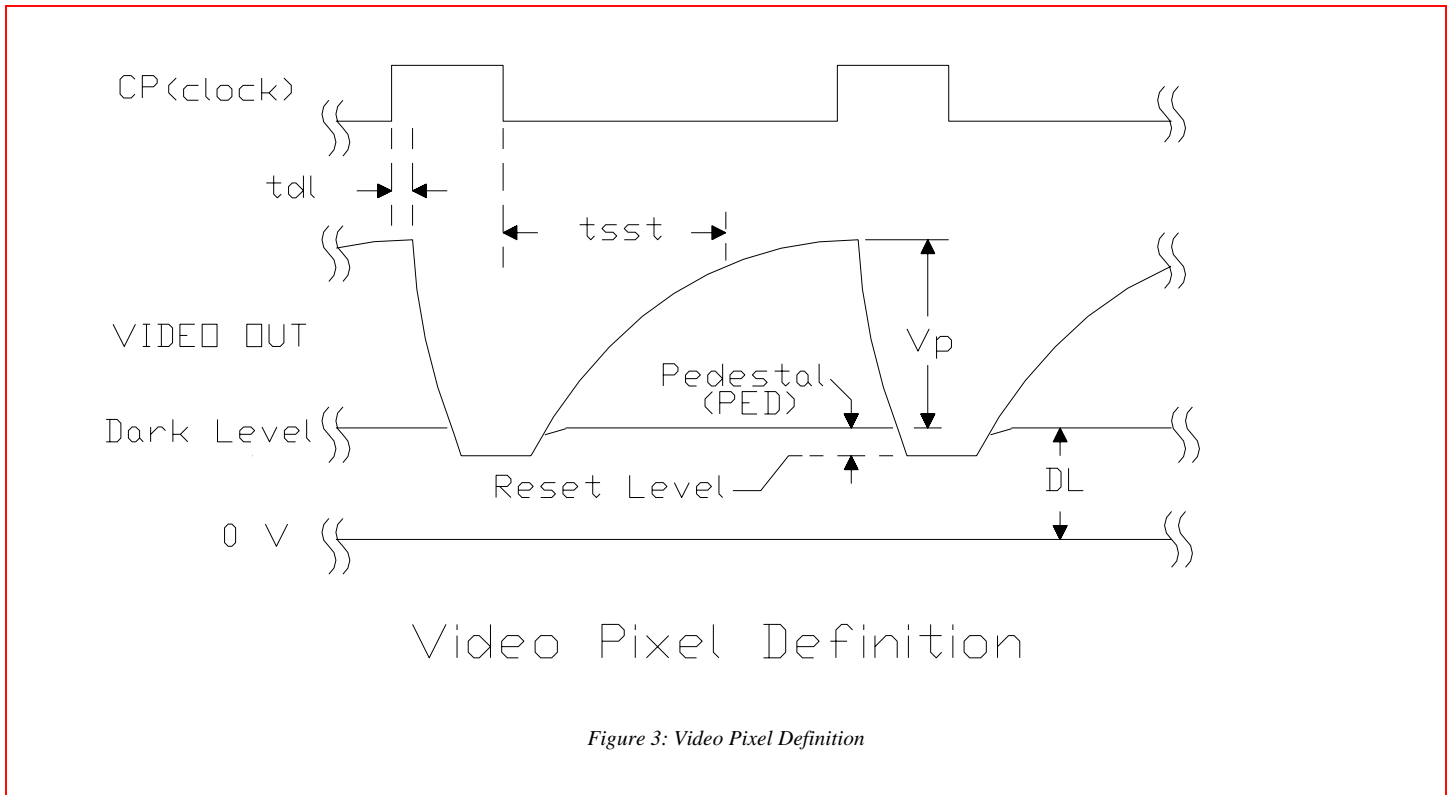## 9.0 Reset Level and Video Sampling Time

Figure 3: Video Pixel Definition

Figure 3 graphically shows the video signal waveform and defines the single video pixel structure. The signal output waveform is shown relative to the input clock waveform, as well as the symbols and terminologies used to define the performance specifications. Figure 3 explains the terminology used to characterize the dark signal levels and the recommended video pixel sampling times.

Note 6, under Table 7, specifies the dark level (DL). This is the level seen during the dark read out; for example, either the module sits on a black target or the light source is turned off. It is measured from ground or 0V. The reset level is a reference level for the reset switch, which is not necessarily on ground because after the reset occurs, the signal is passed through an amplifier. The difference between the dark level and the reset level is called the pedestal (PED). In most cases, the offset control of the amplifier is used to adjust the dark level to 0V or ground. Hence, the reset level will sit below ground.

The video pixels demonstrated in this graph emanate from an ideal CIS module with a phototransistor imaging structure. The video output at high speeds, such as 5.0MHz, does not instantly rise to its final value, although given enough time; it would asymptotically approach its steady state value. But, at high speeds it is impractical to wait for the final stable value. Accordingly, as Figure 3 indicates, the output signal continues to rise towards its steady state value. Consistent with the forgoing comments, under Table 7, instead of the conventional signal sampling time, tst is defined to substitute the conventional settling time definition. This definition is used because the output signal continues to rise asymptotically to the final stable value but not within a practical time in high speed applications. This is true even when the video rises to its peak value, Vp, defined in the algorithm used in the measurements described by the following equation:

$MTF=\{[Vp(n)+Vp(n+1)]/2-[Vp(n+2)+Vp(n+3)]/2\}/\{[Vp(n)+Vp(n+1)]/2+[Vp(n+2)+Vp(n+3)]/2\}$
Where n is 1, 2, ...1728th, Vp(n) is the signal amplitude of the nth pixel.

10.0 Operating Conditions (25°C)

Table 8: Recommended Operating Conditions (25°C)

Item	Symbol	Min.	Typ.	Max.	Units
Power supply	Vdd (positive)	4.5	5.0	5.5	V
	Vn (negative)	-10	-5	-4.0	V
	Idd (positive)	60	66	75	ma
	In (negative)[1]	20	20	20	ma
Input voltage at digital high	Vih	Vdd-1.0	Vdd-0.5	Vdd	V
Input voltage at digital low	Vil	0		0.6	V
Clock frequency	Fclk	0.2 [2]		5.5[3]	MHz
Clock pulse high duty cycle			25		%
Clock pulse high duration		45.5	50		ns
Integration time	Tint	82	150		μs
Operating temperature[4]	Top		25	50	°C
AMIS-710205-A4					
Parameter	**Min.**	**Typ.**	**Max.**		
VLED		5.0	5.5	V	
ILED		480	550	ma	
AMIS-710206-A4					
	Min.	**Typ.**	**Max.**		
VLED		5.0	5.5	V	
ILED		480	550	ma	

Notes:

(1) Current is essential constant current with supply voltage.
(2) This is determined by the longest tolerable integration time. Because of leakage current build up, the integration time is recommended to be no greater than 10ms.
(3) The maximum call out is for the modules' electrical speed. The light source still dictates the highest speed performance.
(4) This specification is a standard used by the CIS makers for the fax industry.

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11.0 Switching Characteristics (25°C)

The switching characteristics at 25°C for the I/O clocks are shown in Figure 4. Each switch timing characteristic for each waveform is represented by its symbolic acronym. Each corresponding switching time is defined in Table 9.

MODULE TIMING DIAGRAM

Figure 4: Module Timing Diagram
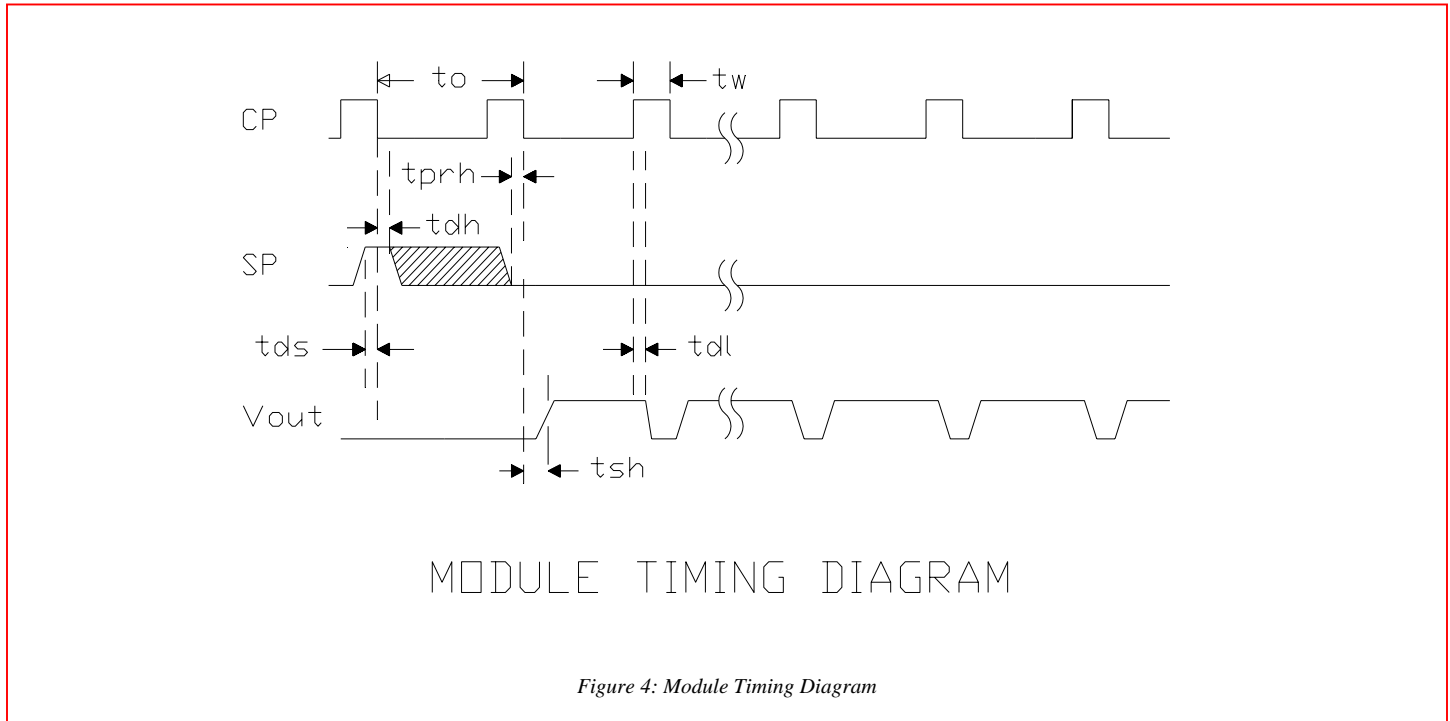
Note: Only one video output is shown because all four videos have identical electrical characteristics. The only physical difference between the outputs is in the Section 4 output, VOUT4. Section 4 has only six sensor chips; hence, its active scan is shorter by 64 pixels (see Figure 4).

Table 9: Timing Symbol's Definitions and Timing Values

Item	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	to	0.20		4.0	μs
Clock pulse width	tw	50			ns
Clock duty cycle		25		75	%
Prohibit crossing time of Start Pulse[1]	tprh	0			ns
Data setup time	tds	20			ns
Data hold time	tdh	0			ns
Signal delay time	tdl	20			ns
Signal settling time	tsh	100			ns

Note:
(1)   "Prohibit crossing of start pulse" is used to indicate that the start pulse should not be active high between any two consecutive clock pulses; specifically, between two consecutive low going clock pulses (see the Figure 4). All falling clock edges under an active high start pulse load the internal shift register, therefore the start pulse must be active over only one falling clock edge. A high start pulse over all rising clock edges is ignored by the shift register. One simple way to ensure that the start pulse will not be actively high during two consecutive falling clock edges is to generate the start pulse on a rising clock edge and terminate it on the following rising clock edge.

12.0 Mechanical Drawing of the Module

Figure 5 depicts the isometric sketch of the module housing, showing the connector location, the approximate overall dimensions of the module and its general geometric layout. It is not intended for use as a design reference. Detailed drawings for the AMIS-710205/206 modules are available upon request.
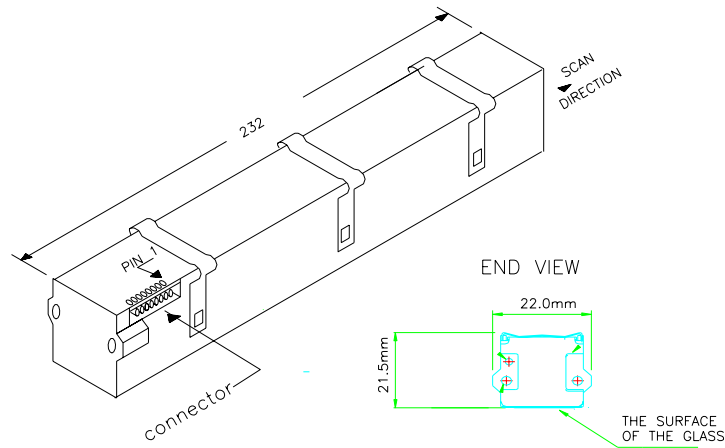

Figure 5: AMIS-710205/206 Module Mechanical Overview

13.0 Company or Product Inquiries

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