1.0 Description

AMI Semiconductor's HSN series is family of self-scanning photodiode solid-state linear imaging arrays. These photodiode sensors employ AMI Semiconductor's proprietary CMOS image sensing technology to integrate the sensors into a single monolithic chip. These sensors are optimally designed for applications in spectroscopy. Accordingly, these sensors contain a linear array of photodiodes with an optimized geometrical aspect ratio (25µm aperture pitch x 2500µm aperture width) for helping to maintain mechanical stability in spectroscopic instruments and for providing a large light-capturing ability. The family of sensors consists of photodiode arrays of various lengths, 256, 512, and 1024 pixels.

The HSN photodiode arrays are mounted in 22-pin ceramic side-brazed dual-in-line packages, which fit in standard DIP sockets. A diagram of its pin-out configuration is seen in Figure 1.

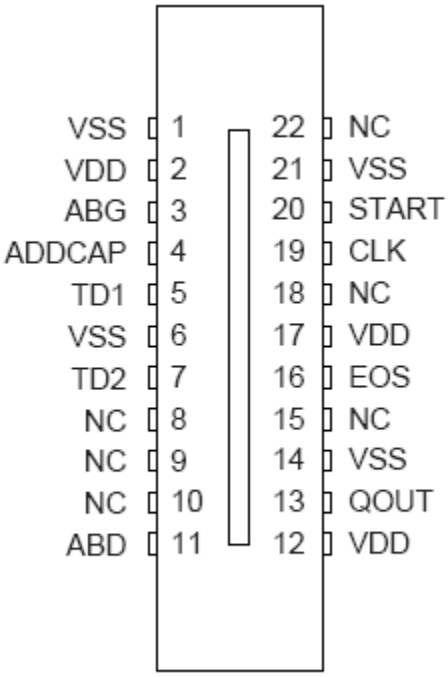


Figure 1: Pin Out Configuration

2.0 Key Features

- Selectable saturation charge capacities: 65pC capacity for wider dynamic range and 25pC for lower noise readout
- Wide spectral response (180 – 1000nm) for UV and IR response
- NP junction photodiodes with superior resistance to UV damage
- Low dark current
- Integration time up to 11 seconds at room temperature
- Integration time extended to hours by cooling
- Anti-blooming circuitry
- High linearity
- Low power dissipation (less than 1mW)
- Geometrical structure for enhanced stability and registration
- Standard 22-lead dual-in-line IC package

3.0 Sensor Characteristics

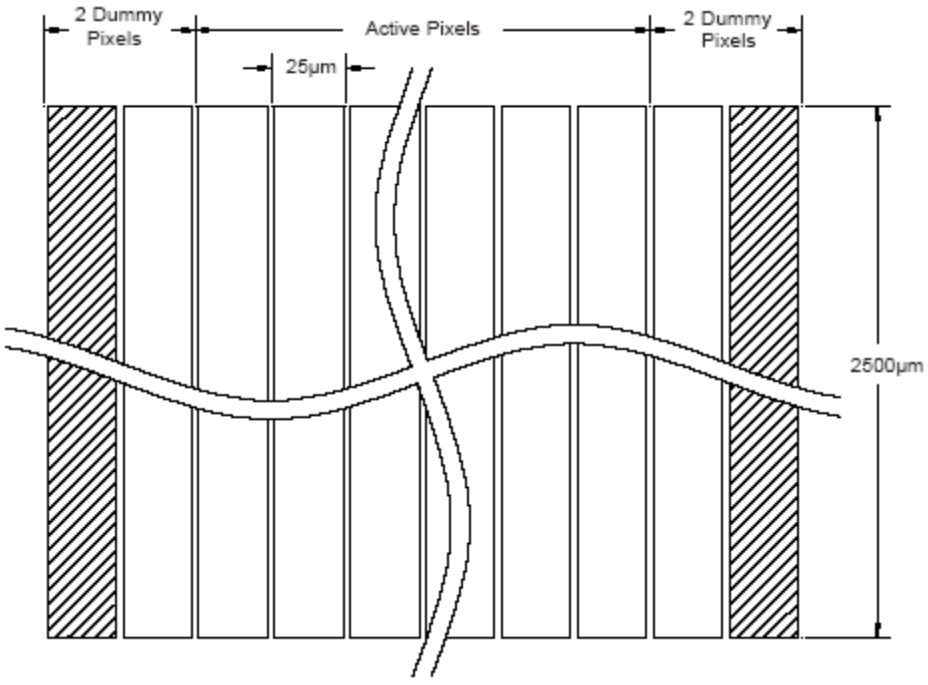


Figure 2: Geometry and Layout of Photodiode Pixels

During normal operation, the photons incident in or near the NP photodiode junction generate free charges, which are collected and stored on the junction's depletion capacitance. The number of collected charges is proportional to the light exposure. Figure 3 shows the stored signal charge as function of light exposure at a wavelength of 575nm. The exposure is the product of the light intensity in nW/cm2 and integration time in seconds. The charge accumulates linearly until reaching the saturation charge and the corresponding exposure is the saturation exposure. There are two saturation limits which are described in Section 4.0.

The responsivity may be calculated as the saturation charge divided by the saturation exposure. The predicted typical responsivity of a photodiode is 1.5×10^{-4} C/J/cm^2 at 575nm. Figure 4 shows the predicted responsivity of the photodiodes as a function of wavelength.

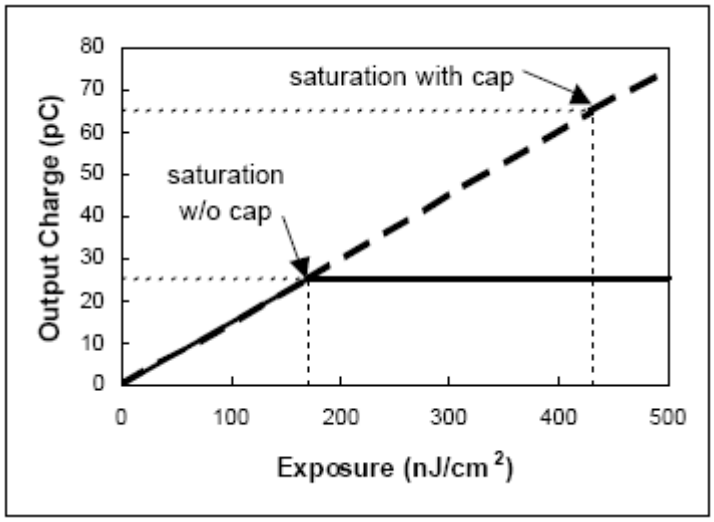


Figure 3: Stored Signal Charge as a Function of Exposure at a Wavelength of 575nm

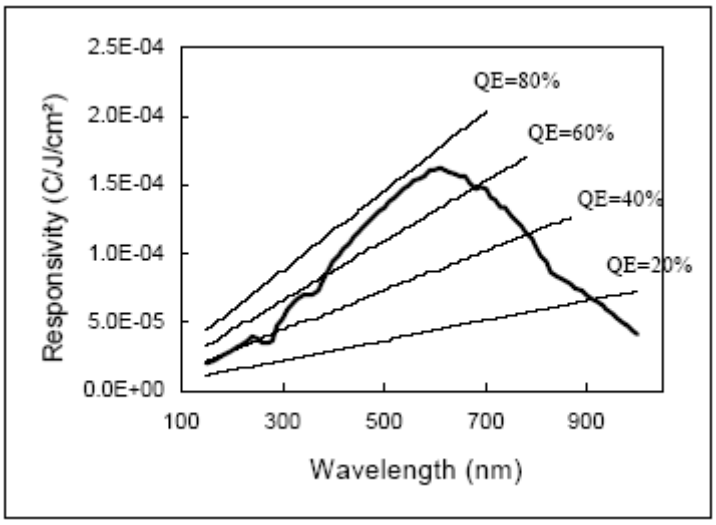


Figure 4: Predicted Spectral Response

The quantum efficiency (QE) can be calculated by dividing the responsivity by the area of the sensor's element and multiplying the resulting ratio by the energy per photon in electron volts (eV).

The dark current is typically 0.2pA at 25°C and varies as function of temperature. The dark current will contribute dark-signal charges and these charges will increase linearly with integration time. The dark signal and the photo-generated signal combined result in the total signal charge.

4.0 Selectable Charge Capacity

The HSN devices have the unique feature of having a selectable charge capacity. There is a bank of capacitors with one capacitor for each photodiode pixel. When the capacitors are connected to the photodiodes, they give the photodiodes a charge capacity of typically 65pC. This large charge capacity is useful in applications that demand high dynamic range and high signal-to-noise ratios. With the capacitors disconnected, the photodiodes typically have an intrinsic charge capacity of 25pC. With a reduced capacitance, the photodiode array can operate with a lower reset (kTC) noise.

The ADDCAP pin is provided to control the connection of the capacitors. When ADDCAP is high, all the capacitors are connected. When ADDCAP is low, all the capacitors are disconnected. It is advised that all the photodiodes are reset after each toggle of ADDCAP. This is simply done by clocking one line scan of the photodiode array.

5.0 Anti-Blooming Circuit

Each photodiode pixel has a built-in anti-blooming circuit structure. Without an anti-blooming circuit, it is possible that a fraction of the excess charge from one pixel will flow into neighboring pixels. The anti-blooming circuit prevents this by redirecting the excess current into the anti-blooming drain before the photodiode is too full. A self-biased anti-blooming gate sets the level at which the charge begins to flow into the drain. Think of it this way. If the photodiode were your bathroom sink, then the anti-blooming circuit would be your sink's overflow drain.

The anti-blooming circuit may be disabled by grounding the anti-blooming gate. This would, in effect, raise the drain level.

6.0 Self-Scanning Circuit

Figure 5 shows a simplified electrically equivalent circuit diagram of the photodiode array. A MOS read switch connects every photodiode in the array to a common output video line. Incident photons generate an electron charge, which is collected on each imaging photodiode while the switch is open. The shift register is activated by the start pulse. A pulse propagates through each shift register stage and activates the MOS read switches sequentially. As the shift register sequentially closes each read switch, the negative stored charge, which is proportional in amount to the light exposure from the corresponding photodiode, is readout onto the video line, QOUT. Typically, an external charge-integrating amplifier senses the negative output charge on the video line from each photodiode pixel. The shift register continues scanning the photodiodes in sequence, until the last shift register stage is reached, at which time the fourth and last dummy pixel is read out and end-of-scan (EOS) output is held high for one clock cycle. The next start pulse can then restart the shift register.

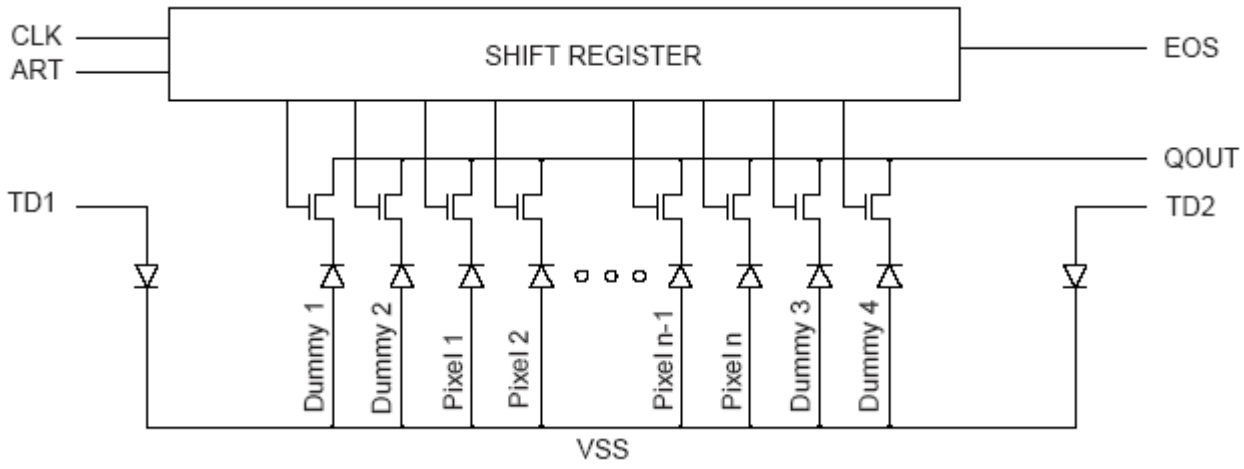


Figure 5: Simplified Circuit Diagram of an HSN Photodiode Array

The diagram in Figure 5 does not include the capacitor bank and the anti-blooming circuitry.

7.0 I/O Pins

Besides the VSS and VDD supply pins, there are nine functionally active I/O pins. Only two clocks, CLK and START, are required for controlling the timing of the sensor's video readout. One additional digital input, ADDCAP controls the bank of capacitors as described in the Section 6.0. The digital output, EOS, marks the end of the line-scan. The charge output pin, QOUT, is typically connected to a charge-integrating amplifier, which is biased to Vbias (see Section 8.0). For normal anti-blooming operation, the ABG requires a 0.1µF capacitor connected to VSS and the ABD is also biased to Vbias. Each temperature diode is operated with a small constant current, which forward biases its PN junction. By measuring the forward-bias voltage, one can track the silicon die temperature. The temperature diodes may be disabled by connecting their anodes to VSS. These I/Os are listed with their acronym designators and functional descriptions in Table 1.

Table 1: Symbols and Functions and I/O Pins

Symbol	Function and Description
VSS	Ground
VDD	+5.0V
START	Start pulse: input to start the line scan
CLK	Clock pulse: input to clock the shift register
ADDCAP	Add capacitors: input that selects the bank of capacitors to increase charge capacity
EOS	End of scan: output from the shift register to indicate the completion of one line scan
QOUT	Video charge output: output from the photodiodes pixels
ABG	Anti-blooming gate: self-biased gate for setting anti-blooming level. Requires 0.1-µF connected to VSS
ABD	Anti-blooming drain: bias for anti-blooming drain, set to Vbias
TD1	Temperature Diode 1: anode of temperature Diode 1
TD2	Temperature Diode 2: anode of temperature Diode 2
NC	No connection

8.0 Clock and Voltage Requirements

The clocking requirements are relatively simple. As it was indicated in Figure 5 and Table 1, there are only two input signals that require clocked inputs. They are CLK, the clock for the shift register, and START, the shift register start pulse. The timing specifications and the symbol definition for Figure 6 are listed in Table 2. The control clock amplitudes for I/Os are compatible with the 5V CMOS devices.

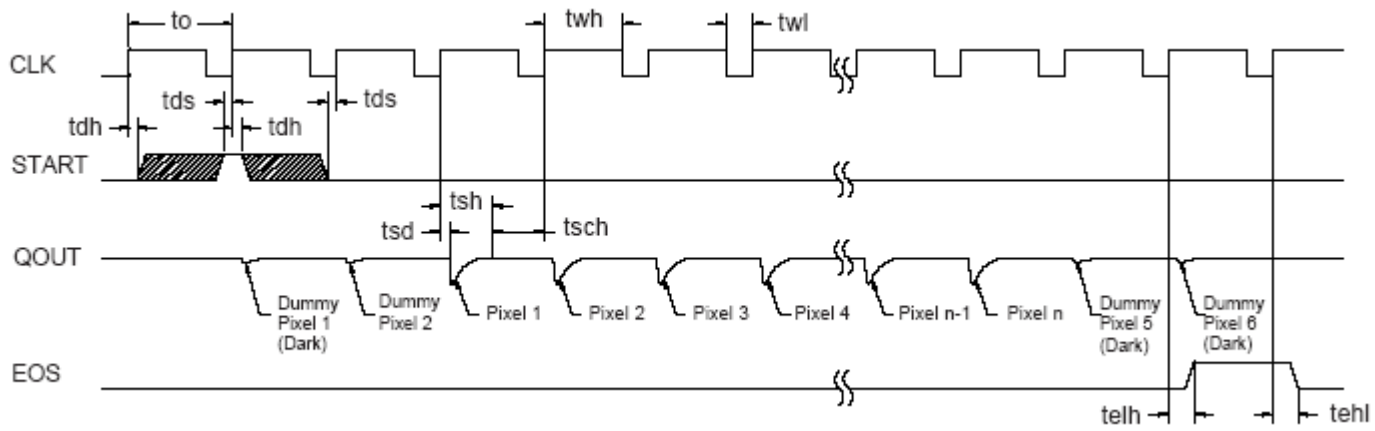


Figure 6: Timing Diagram

Table 2: Symbol Definitions and Timing Specifications for Timing Diagram

Item	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	to	1000	10000		ns
Clock high pulse width	twh	900			ns
Clock low pulse width	twl	100			ns
Clock duty cycle		1	50	99	%
Data setup time	tds	100			ns
Data hold time	tdh	100			ns
EOS low-to-high delay	telh			400	ns
EOS high-to-low delay	tehl			400	ns
Signal delay time	tsd	50			ns
Signal settling time	tsh			900	ns
Signal settle to clock edge	tsch	0			ns

9.0 Recommended Operating Conditions

Table 3 lists the recommended operating conditions.

Table 3: Recommended Operating Conditions at 25°C

Parameters	Symbol	Min.	Typ.	Max.	Units
Power supply	VDD	4.5	5.0	5.5	Volts
Input clock pulses high level (1)	Vih	VDD – 0.8	VDD	VDD	Volts
Input clock pulse low level (1)	Vil	0.0	0.0	0.8	Volts
Video charge output external bias	Vbias	VDD – 0.5	VDD – 0.5	VDD	Volts
Clock frequency	Fclk		0.1	1.0	MHz
Integration time (2)	Tint	0.26 (734256) 0.52 (734512) 1.03 (734024)		11000 (w/ cap)	ms

Notes:

(1) Applies to all control-clock inputs.

(2) Integration time is specified at room temperature such that the maximum dark current charge build up in each pixel is less than 10 percent of the minimum saturation charge. Accordingly, it may be as long as 11 seconds at room temperature with the added capacitors. Longer integration times may be achieved by cooling the device. An appropriate clock frequency must be chosen so that the shift register completes its operation within the desired integration time.

10.0 Electro-Optical Characteristics

Table 4 lists the electro-optical characteristics.

Table 4: Electro-Optical Characteristics at 25°C

Parameters	Symbol	Min.	Typ.	Max.	Units
Center-to-center spacing			25		µm
Aperture width			2500		µm
Pixel area	A		6.25×10^{-4}		cm^2
Fill factor (1)	FF		72		%
Quantum efficiency (1)(2)	QE		70		%
Responsivity (1)(2)	R		1.5×10^{-4}		$C/J/cm^2$
Non-uniformity of response (3)			2		+/-%
Saturation exposure (2)	Esat	370 (w/cap) 130 (w/o cap)	430 (w/ cap) 170 (w/o cap)		nJ/cm^2
Saturation charge (4)	Qsat	55 (w/cap) 20 (w/o cap)	65 (w/cap) 25 (w/o cap)		pC
Average dark current (5)			0.2		pA
Spectral response peak	λ		600		nm
Spectral response range (6)			180 - 1000		nm

Notes:

(1) Fill factor, quantum efficiency and responsivity are related by the equation R = (qel/hc).QE.FF.A, where qe is the charge of an electron and hc/l is the energy of a photon at a given wavelength. Responsivity is therefore given per pixel.

(2) At wavelength of 575nm (Yellow-Green) and with no window.

(3) Measured at 50 percent Vsat with an incandescent tungsten lamp filtered with an Schott KG-1 heat-absorbing filter.

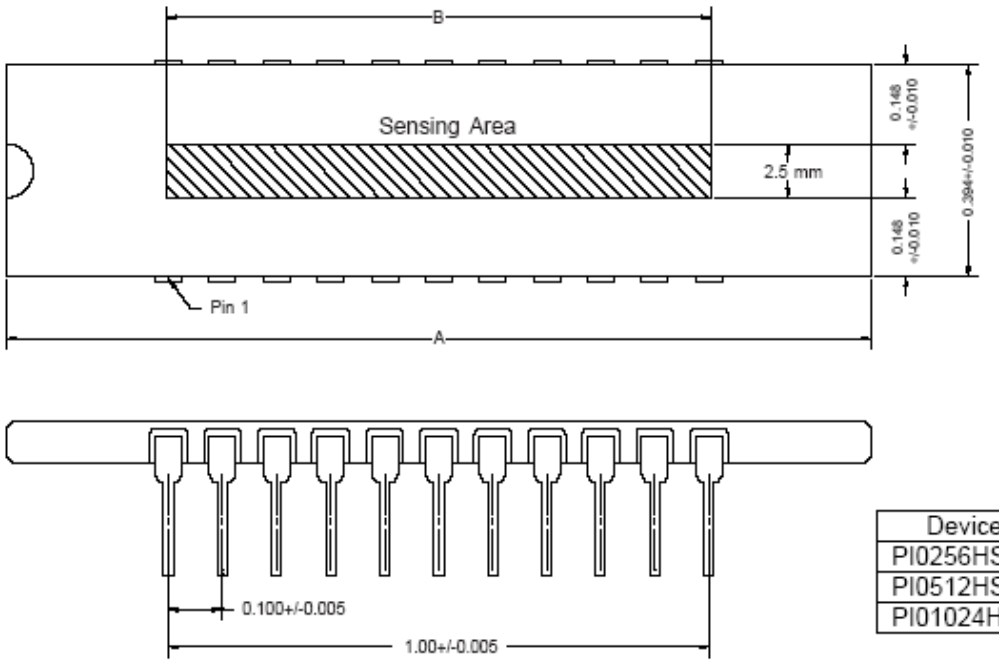
(4) Saturation charge specified for a video output bias of 4.5V.

(5) Max dark leakage £ 1.5 x average dark leakage measured with an integration period of 500ms at 25°C.

(6) From 250-1000nm, responsivity ³ 20 percent of its peak value.

11.0 Package Dimensions

Figure 7 provides the package dimensions.



Device	A	B
PI0256HSN	1.080±0.010	6.4 mm
PI0512HSN	1.080±0.010	12.8 mm
PI01024HSN	1.600±0.010	25.6 mm

Figure 7: Package Dimensions

12.0 Company or Product Inquiries

For more information about AMI Semiconductor, our technology and our product, visit our Web site at: http://www.amis.com

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