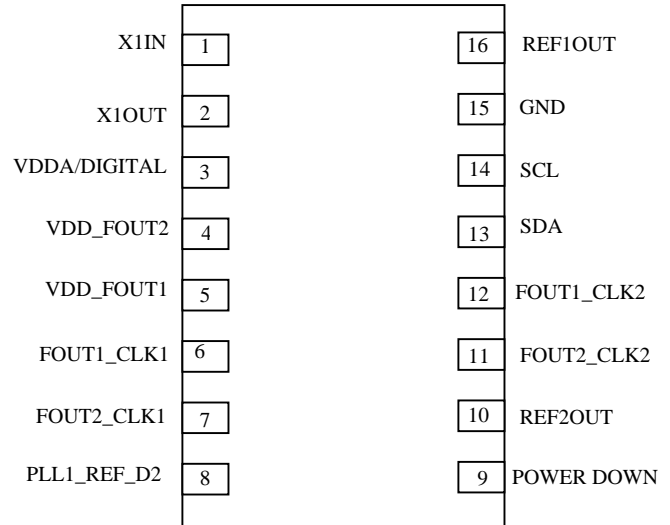




## Features

- Two on chip PLLs.
- Generates an EMI optimized clocking signal at output.
- Non Spread spectrum mode available
- Input Frequency Range 2MHz– 200Mhz in Non Spread mode
- Input Frequency Range 6Mhz – 80Mhz in Spread mode.
- Output Frequency Range 4Mhz – 140Mhz.
- Four frequency outputs; two per PLL.
- Programmable spread range and type of modulation ( center or down) and type of profile.
- Power down feature is incorporated.
- Both the PLL have reference frequency output.
- Supply voltage range 3.3 V ( $\pm$  0.3)
- Software is available for configuring all the parameters of the Chip, through I2C .

## Pin Configuration



## Product Description

The AS80M2516A is dual phase lock loop clock chip. The AS80M2516A is a versatile spread spectrum frequency modulator design specifically for a wide range of clock frequencies.

The AS80M2516A reduces electromagnetic interference (EMI) at clock source. The AS80M2516A allows significant system cost savings by reducing the number of circuit board layers and shielding that are required to pass EMI regulations.

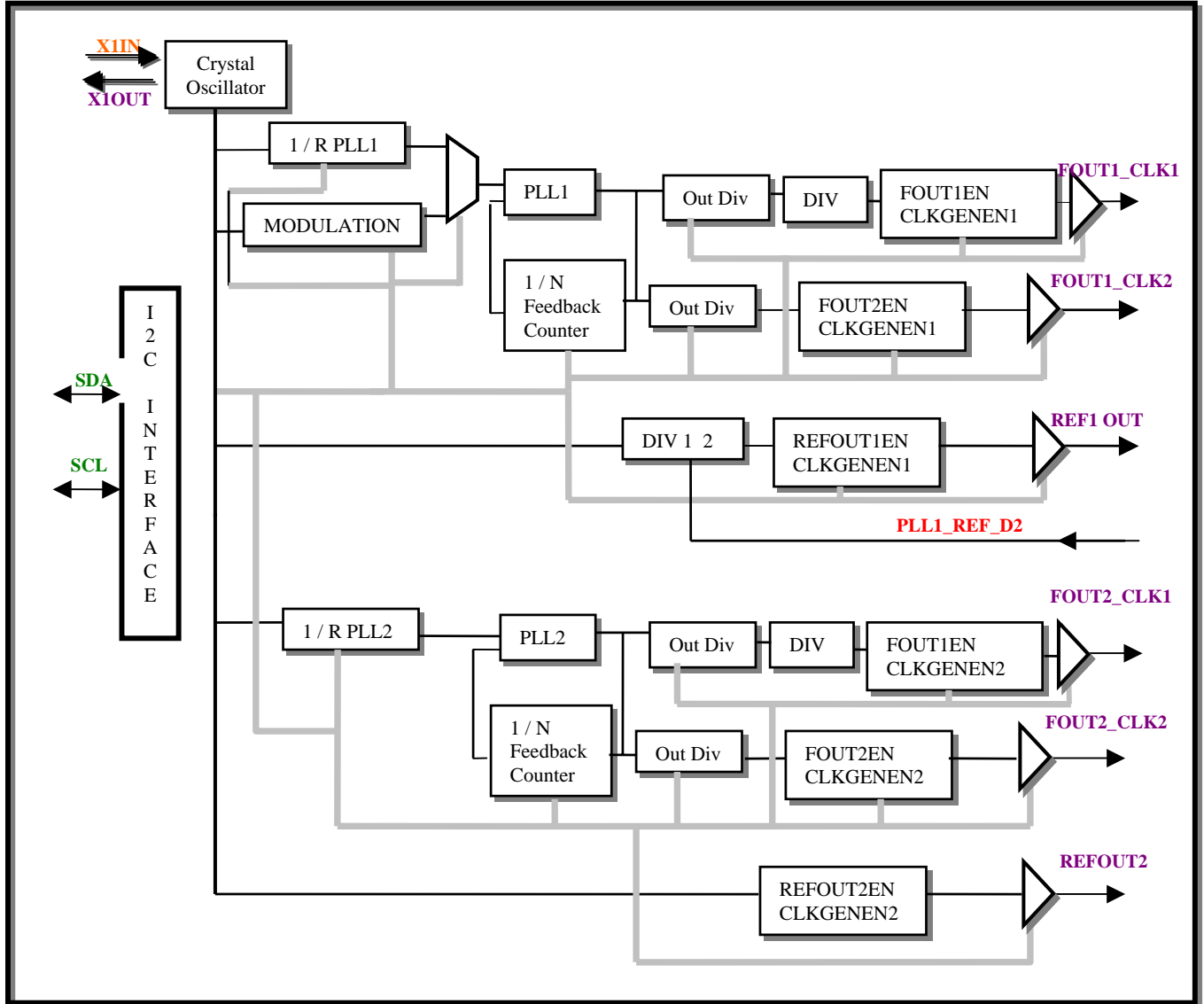
The AS80M2516A is I2C configurable. All the

functional parameters of the AS80M2516A can be configured from external I2C master unit through I2C bus.

The AS80M2516A modulates the output of PLL in order to spread the bandwidth of a synthesized clock, thereby decreasing the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillator and most clock generators. Lowering EMI by increasing a signal's bandwidth is called spread spectrum clock generation.



Block Diagram





### Pin Description

Pin No	Pin Name	Pin Type	Description
1	X1IN	IN	Connection to Crystal-1
2	X1OUT	OUT	Connection to Crystal-1
3	VDDA/DIGITAL	PWR	Power supply to Analog and Digital blocks except the Output Buffers
4	VDD_FOUT2	PWR	Variable Output Voltage Control for FOUT2 . The minimum voltage is 1.8V.
5	VDD_FOUT1	PWR	Variable Output Voltage Control for FOUT1 . The minimum voltage is 1.8V.
6	FOUT1_CLK1	OUT	Tristatable Clock Output-1 of Clock Generator-1
7	FOUT2_CLK1	OUT	Tristatable Clock Output-2 of Clock Generator-1
8	PLL1_REF_D2	IN	Set High to divide the REF_IN(X1IN) by 2
9	POWERDOWN	IN	Powers the entire chip down
10	REF2OUT	OUT	Buffered and Divide by 2 Output of X1IN
11	FOUT2_CLK2	OUT	Tristatable Clock Output-2 of Clock Generator-2
12	FOUT1_CLK2	OUT	Tristatable Clock Output-1 of Clock Generator-2
13	SDA	IN/OUT	Serial Data I/O for I2C
14	SCL	IN	Serial Clock Input for I2C
15	GND	PWR	Ground to entire chip
16	REF1OUT	OUT	Buffered Output of X1IN

Note:- All the Pin types IN have CMOS pull-up resistors.



rev 1.0

### Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality and reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage, dc ( $V_{SS} = \text{ground}$ )	$V_{DD}$	$V_{SS}-0.5$	7	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{IK}$	-50	50	mA
Output Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{OK}$	-50	50	mA
Storage Temperature Range (non condensing)	$T_S$	-65	150	°C
Ambient Temperature Range, Under Bias	$T_A$	-55	125	°C
Junction Temperature	$T_J$		150	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL – STD 883E, Method 3015.7)			2	kV



#### **CAUTION: ELECTROSTATIC SENSITIVE DEVICE**

Permanent damage resulting in loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.



### Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD}$	$3.3V \pm 10\%$	3	3.3	3.6	V
Ambient Operating Temperature Range	$T_A$		0		70	°C
Crystal Resonator Frequency	$F_{XIN}$		2		200	MHz
Serial Data Transfer Rate		Standard mode	10		100	kb/s
Output Driver Load Capacitance	$C_L$				15	pF



rev 1.0

### DC Electrical Specifications

Unless otherwise stated,  $V_{DD}=3.3V \pm 10\%$ , no load on any output, and ambient temperature range  $T_A=0^\circ\text{C}$  to  $70^\circ\text{C}$ . Parameters with an asterisk (\*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are  $\pm 3\sigma$  from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/ DESCRIPTION	MIN	TYP	MAX	UNIT
<b>Overall</b>						
Supply Current, Dynamic	$I_{DD}$	$V_{DD}=3.3V$ , $F_{CLK}=50\text{MHz}$ , $C_L=15\text{pF}$		43		mA
Supply Current, Static	$I_{DDL}$	$V_{DD} = 3.3V$ , powered down via Power Down pin		0.3		mA
<b>All input pins</b>						
High-Level Input Voltage	$V_{IH}$	$V_{DD}=3.3V$	2.0		$V_{DD}+0.3$	V
Low-Level Input Voltage	$V_{IL}$	$V_{DD}=3.3V$	$V_{SS}-0.3$		0.8	V
High-Level Input Current	$I_{IH}$		-1		1	$\mu\text{A}$
Low-Level Input Current (pull-up)	$I_{IL}$		-20	-36	-80	$\mu\text{A}$
High-Level Output Source Current	$I_{xOH}$	$V_{DD}=V(XIN) = 3.3V$ , $V_O=0V$	10	21	30	mA
Low-Level Output Source Current	$I_{xOL}$	$V_{DD}=3.3V$ , $V(XIN)=V_O=5.5V$	-10	-21	-30	mA
<b>Clock Outputs (CLK1, CLK2)</b>						
High-Level Output Source Current	$I_{OH}$	$V_O=2.4V$		-20		mA
Low-Level Output Sink Current	$I_{OL}$	$V_O=0.4V$		23		mA
Output Impedance	$Z_{OH}$	$V_O=0.5V_{DD}$ ; output driving high		29		$\Omega$
	$Z_{OL}$	$V_O=0.5V_{DD}$ ; output driving low		27		



## AC Timing Specifications

Unless otherwise stated,  $V_{DD} = 3.3.0V \pm 10\%$ , no load on any output, and ambient temperature range  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ . Parameters denoted with an asterisk (\*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are  $\pm 3\sigma$  from typical.

PARAMETER	SYMBOL	CONDITIONS/ DESCRIPTION	CLOCK (MHz)	MIN	TYP	MAX	UNIT
<b>Overall</b>							
Output Frequency	$f_o$	$V_{DD} = 3.3V$		4		140	MHz
Rise Time	$t_r$	$V_O = 0.3V$ to $3.0V$ ; $CL = 15pF$			2.1		ns
Fall Time	$T_f$	$V_O = 3.0V$ to $0.3V$ ; $CL = 15pF$			1.9		ns
<b>Clock Outputs (PLL A clock via FOUT1_CLK1/FOUT2_CLK1 pins)</b>							
Duty Cycle		Ratio of pulse width (as measured from rising edge to next falling edge at 2.5V) to one clock period	100	45		55	%
Jitter, Long Term ( $\sigma(\tau)$ )*	$T_{j(LT)}$	On rising edges 500 $\mu\text{s}$ apart at 2.5V relative to an ideal clock, $C_L = 15pF$ , $f_{XIN}=14.318\text{MHz}$ , $F_{OUT} = 50\text{MHz}$ , PLL-B inactive.	100		45		
		On rising edges 500 $\mu\text{s}$ apart at 2.5V relative to an ideal clock, $C_L = 15pF$ , $f_{XIN}=14.318\text{MHz}$ , $F_{OUT} = 50\text{MHz}$ , PLL -B active (60MHz)	50		165		
Jitter, Period (peak-peak)	$T_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, $C_L = 15pF$ , $f_{XIN}=14.318\text{MHz}$ , $F_{OUT} = 50\text{MHz}$ PLL-B inactive.	100		110		ps
		From rising edge to the next rising edge at 2.5V, $CL = 15pF$ , $f_{XIN}=14.318\text{MHz}$ , $F_{OUT} = 50\text{MHz}$ PLL-B active (60MHz)	50		390		



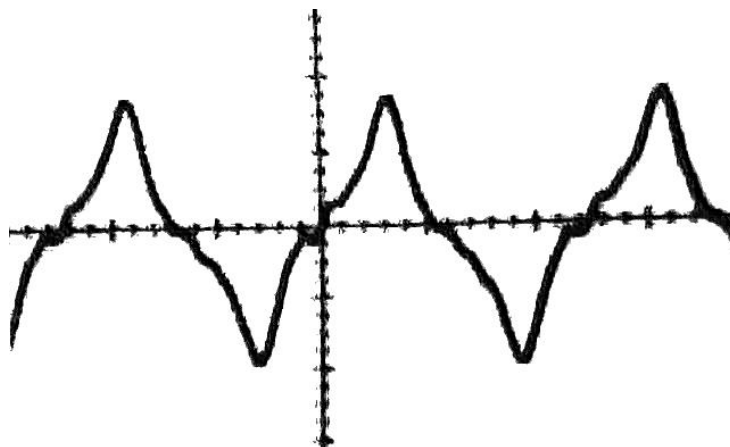
rev 1.0

**AC Timing Specifications (Continued)**

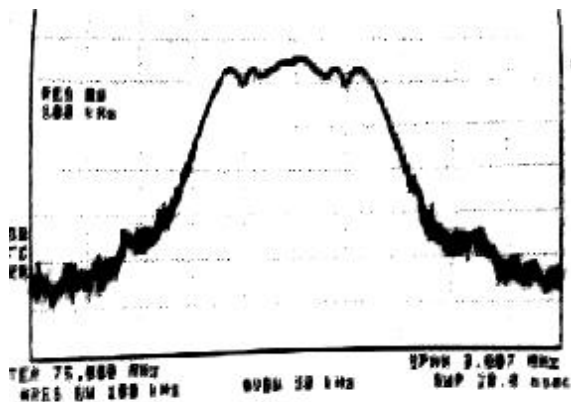
Unless otherwise stated, VDD = 3.3.0V ± 10%, no load on any output, and ambient temperature range TA = 0°C to 70°C. Parameters denoted with an asterisk (\*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/ DESCRIPTION	CLOCK (MHz)	MIN	TYP	MAX	UNIT
<i>Clock Outputs (PLL B clock via FOUT1_CLK2/FOUT2_CLK2 pins)</i>							
Duty Cycle		Ratio of pulse width (as measured from rising edge to next falling edge at 2.5V) to one clock period	100	45		55	%
Jitter, Long Term ( $\sigma_y(\tau)$ )*	$T_{j(LT)}$	On rising edges 500 μs apart at 2.5V relative to an ideal clock, C <sub>L</sub> = 15pF, f <sub>XIN</sub> =14.318MHz, F <sub>OUT</sub> = 50MHz, PLL -A inactive.	100		45		ps
		On rising edges 500 μs apart at 2.5V relative to an ideal clock, C <sub>L</sub> = 15pF, f <sub>XIN</sub> =14.318MHz, F <sub>OUT</sub> = 50MHz, PLL -A active (60MHz)	60		75		
Jitter, Period (peak-peak)	$T_{j(\Delta P)}$	From rising edge to the next rising edge at 2.5V, C <sub>L</sub> = 15pF, f <sub>XIN</sub> =14.318MHz, F <sub>OUT</sub> = 50MHz PLL-B inactive.	100		120		ps
		From rising edge to the next rising edge at 2.5V, C <sub>L</sub> = 15pF, f <sub>XIN</sub> =14.318MHz, F <sub>OUT</sub> = 50MHz PLL-A active (50MHz)	60		400		
Clock Stabilization Time	t <sub>STB</sub>	Output active from power up, RUN Mode via Power Down pin			100		ns





**Modulation Domain Analyser**  
*Snapshot of 75MHz 0.75% Deviation Clock*



**Spectrum Analyser**  
*Snapshot of 75MHz 0.75% Deviation Clock*



rev 1.0

## General I2C Serial Interface Information

The information in this section assumes familiarity with I2C programming.

### How to Write through I2C :

- Master (host) sends a start bit.
- Master (host) sends the write address XX (H)
- AS80M2516A device will acknowledge
- Master (host) sends a dummy command code
- AS80M2516A device will acknowledge
- Master (host) sends a dummy byte count
- AS80M2516A device will acknowledge
- Master (host) starts sending first byte (Byte 0) through byte N - 1
- AS80M2516A device will acknowledge each byte one at a time.
- Master (host) sends a Stop bit

### How to Read through I2C:

- Master (host) will send start bit.
- Master (host) sends the read address XX (H)
- AS80M2516A device will acknowledge
- AS80M2516A device will send the byte count
- Master (host) acknowledges
- AS80M2516A device sends first byte (Byte 0) through byte N - 1
- Master (host) will need to acknowledge each byte
- Master (host) will send a stop bit  
(\* N is the number of bytes)

Controller (Host)	AS80M2516A (slave/receiver)
Start Bit	
Slave Address XX(H)	
	ACK
Dummy Command Code	
	ACK
Dummy byte count	
	ACK
First byte (Byte 0)	
	ACK
Second Byte (Byte 1)	
	ACK
-----	
	---
Last Byte (Bye N-1)	
	ACK
Stop Bit	

Controller (Host)	AS80M2516A (slave/receiver)
Start Bit	
Slave Address XX(H)	
	ACK
	Date Byte Count
ACK	
	First byte (Byte 0)
ACK	
	Second Byte (Byte 1)
ACK	
	----
-----	
	Last Byte (Bye N-1)
Not Acknowledge Stop Bit	



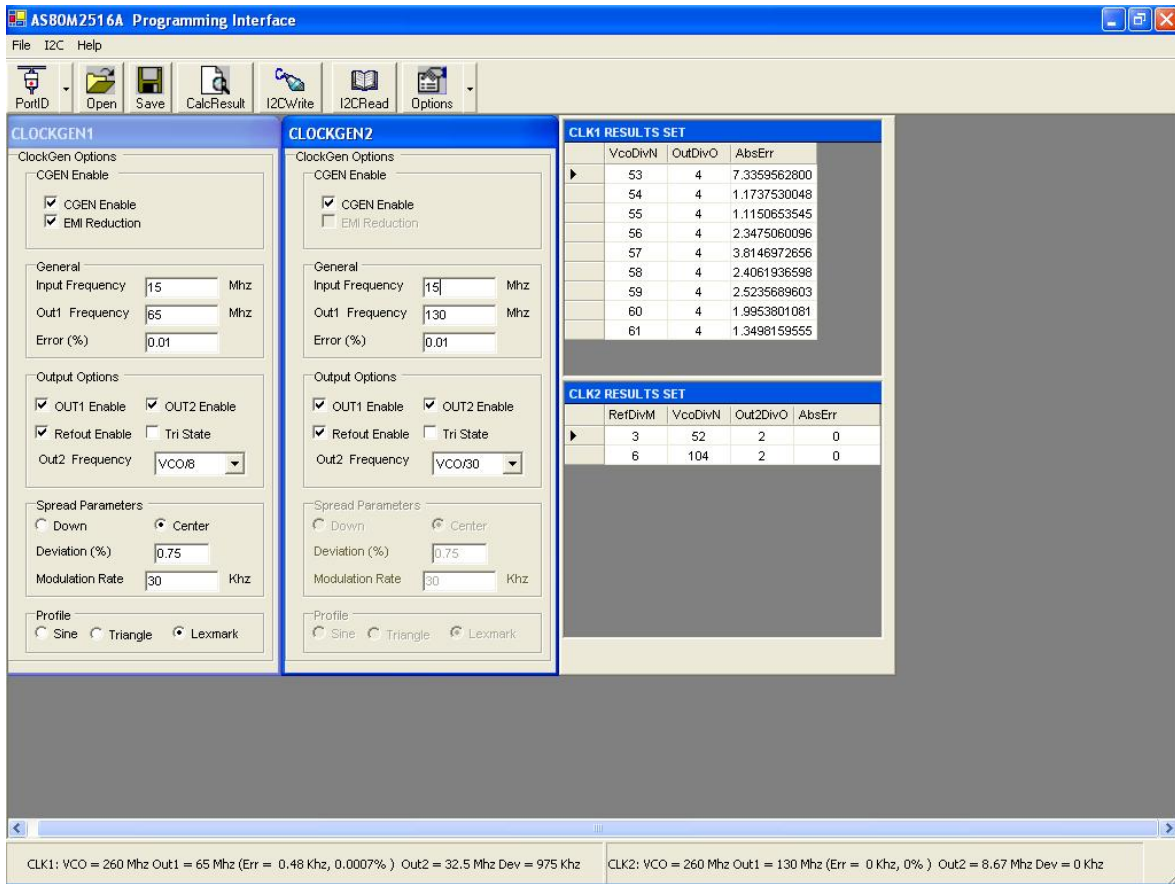
rev 1.0

Software

A demonstration board and software is available for the AS80M2516A. The software can operate under Windows 95 and Windows NT. The opening screen of the software is shown in figure 2.

By pressing the drop down arrow of **Port ID** toolbar button ,any of the three parallel ports ( LPT1 LPT2 or LPT3 ) can be selected. The selected parallel port is used for the I2C data transfer.

Opening screen





## rev 1.0

## Programming the PLLs:-

Select the **CGEN check box** to enable the PLL and the EMI reduction check box to enable the spread spectrum on. Enter the input frequency (in Mhz) , output frequency (Mhz) , percentage error and modulation rate (Khz) in the respective input boxes.

To enable the OUT1 OUT2 and REFOUT click the respective check box. To tristate all the outputs click the tristate check box. Select the type of the modulation between the center or down and enter the deviation (percentage ) in the respective input box. Profile type can be selected between the sine triangular or lexmark.

EMI reduction enable/disable option is only available for the PLL1.

## Writing the data to the chip :-

There are two different ways of writing data to the chip.

1. Writing through the file.
2. Enter the required data in the respective forms and calculate and then write.

For Example:

1. Enter the input freq say 15 Mhz, in the **input frequency** box.
2. Enter the required output frequency say 65 Mhz, in the **out1 frequency** box.
3. Enter the percentage error say 0.01 in the **error** box.
4. Enter the modulation rate say 30 khz in the **modulation rate** box.
5. Select the second output frequency by pressing the pull down menu of the out2 frequency.

The value of OUT2 frequency can be selected as vco/2 , vco/3 , vco/4 , vco/5 , vco/6 , vco/8 , vco/9 , vco/10 , vco/12 , vco/15 , vco/18 , vco/24 or vco/30.

6. Select the type of the deviation , percentage deviation and type of the profile.
7. Enter the data for PLL2 in a similar manner.

8. Press the **CalcResult** button to load the data in the ROM data panel.
9. To write this data to the chip press the **I2CWrite** button.



### Results Window

CLK1 RESULTS SET			
	VcoDivN	OutDivO	AbsErr
▶	53	4	7.3359562800
	54	4	1.1737530048
	55	4	1.1150653545
	56	4	2.3475060096
	57	4	3.8146972656
	58	4	2.4061936598
	59	4	2.5235689603
	60	4	1.9953801081
	61	4	1.3498159555

### Reading the data from the Chip

1. To read the data from the chip through I2C , press the **I2CRead** button.
2. The data can be seen in the rom data field.
3. This data which is read from the chip can be saved in the file by clicking the **Save** button .

CLK2 RESULTS SET				
	RefDivM	VcoDivN	Out2DivO	AbsErr
▶	3	52	2	0
	6	104	2	0

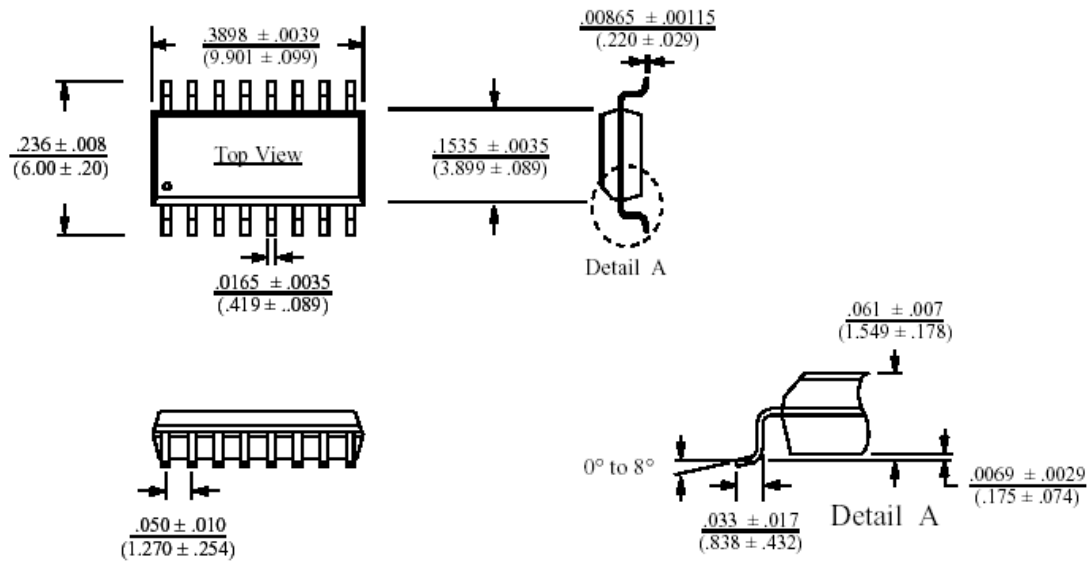


rev 1.0

## Package Information

### 16-PIN PLASTIC SMALL OUTLINE (SOIC) - NB (Narrow Body)

Package Type: 16HN





Alliance Semiconductor Corporation  
2595, Augustine Drive,  
Santa Clara, CA 95054  
Tel# 408-855-4900  
Fax: 408-855-4999  
www.alsc.com

Copyright © Alliance Semiconductor  
All Rights Reserved  
Preliminary Information  
Part Number: AS80M2516A  
Document Version: v1.0

© Copyright 2003 Alliance Semiconductor Corporation. All rights reserved. Our three-point logo, our name and Intelliwatt are trademarks or registered trademarks of Alliance. All other brand and product names may be the trademarks of their respective companies. Alliance reserves the right to make changes to this document and its products at any time without notice. Alliance assumes no responsibility for any errors that may appear in this document. The data contained herein represents Alliance's best data and/or estimates at the time of issuance. Alliance reserves the right to change or correct this data at any time, without notice. If the product described herein is under development, significant changes to these specifications are possible. The information in this product data sheet is intended to be general descriptive information for potential customers and users, and is not intended to operate as, or provide, any guarantee or warranty to any user or customer. Alliance does not assume any responsibility or liability arising out of the application or use of any product described herein, and disclaims any express or implied warranties related to the sale and/or use of Alliance products including liability or warranties related to fitness for a particular purpose, merchantability, or infringement of any intellectual property rights, except as express agreed to in Alliance's Terms and Conditions of Sale (which are available from Alliance). All sales of Alliance products are made exclusively according to Alliance's Terms and Conditions of Sale. The purchase of products from Alliance does not convey a license under any patent rights, copyrights; mask works rights, trademarks, or any other intellectual property rights of Alliance or third parties. Alliance does not authorize its products for use as critical components in life-supporting systems where a malfunction or failure may reasonably be expected to result in significant injury to the user, and the inclusion of Alliance products in such life-supporting systems implies that the manufacturer assumes all risk of such use and agrees to indemnify Alliance against all claims arising from such use.