

# Two-Wire True Zero Speed Miniature Differential Peak-Detecting Gear Tooth Sensor

## Features and Benefits

- Fully optimized differential digital gear tooth sensor
- Single chip IC for high reliability
- Internal current regulator for 2-wire operation
- Small mechanical size (8 mm diameter x 5.5 mm depth)
- Air gap independent switchpoints
- Digital output representing gear profile
- Precise duty cycle signal over operating temperature range
- Large operating air gaps
- Automatic Gain Control (AGC)

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## Packages: 4 pin SIP (suffix SH)



*Not to scale*

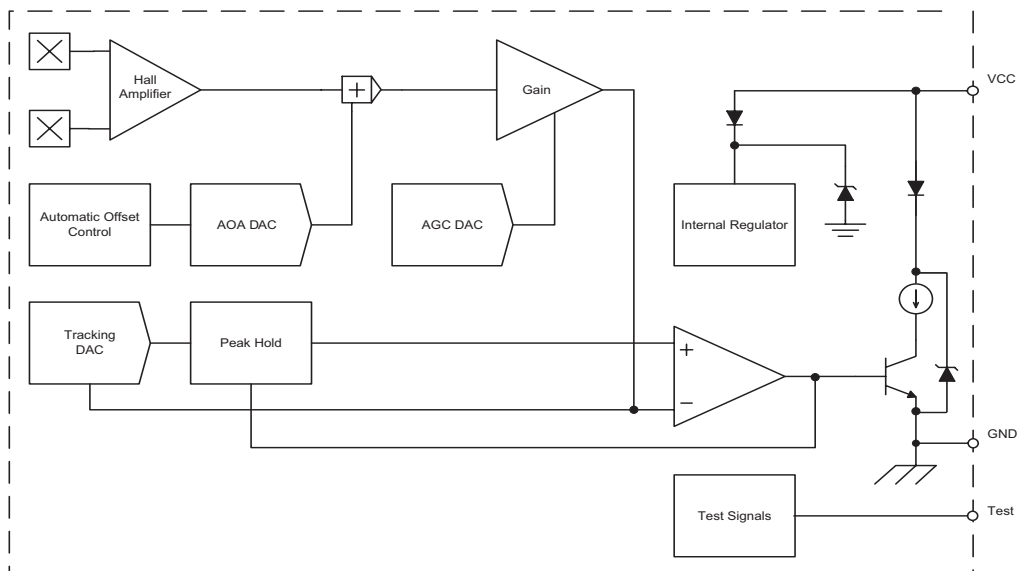
## Description

The components in speed sensing applications continue to diminish in size to meet spatial constraints and weight reduction requirements. As the geometries of gears become smaller, this can compromise the capabilities of a gear speed sensor. The ATS645 Hall-element-to-Hall-element spacing of only 1.5 mm makes this device uniquely capable of accommodating very fine-pitch gears. In addition, the ATS645 signal peak-detecting algorithm supports consistent switching at relatively large air gaps, where the peak-to-peak amplitude is small. These features make the ATS645 the ideal solution to detect the speed of fine-pitch targets such as those found in ABS (antilock braking) systems.

The ATS645 combines a Hall-effect sensing integrated circuit and magnet to provide a manufacturer-friendly solution for true zero-speed digital gear-tooth sensing in two-wire applications. The device consists of a single-shot molded plastic package that includes a samarium cobalt magnet, a pole piece, and a Hall-effect integrated circuit that has been optimized to the magnetic circuit. This small package can be easily assembled and used in conjunction with a wide variety of gear shapes and sizes.

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## Functional Block Diagram



## Features and Benefits (continued)

- Automatic Offset Adjustment (AOA)
- True zero-speed operation
- Undervoltage lockout
- Wide operating voltage range
- Defined power-on state

## Description (continued)

The integrated circuit incorporates a dual-element Hall effect sensor as well as signal processing that switches the output state in response to changes in the magnetic gradients created by ferrous gear teeth. The circuitry contains a sophisticated digital circuit to eliminate magnet and system offsets and to achieve true zero speed operation (U.S. Patent 5,917,320). A-D and D-A converters are used to adjust the device gain at power-on and to allow switching independent of the breadth of the air gap.

The regulated current output is configured for two wire applications, requiring one less wire for operation than do switches with the more traditional open-collector output. The package is available in a lead (Pb) free version, with 100% matte tin leadframe plating.

Part Number	Pb-free <sup>1</sup>	Packing <sup>2</sup>	I <sub>CC</sub> Typical
ATS645LSHTN-I1-T	Yes	Tape and Reel 13-in. 800 pcs./reel	6.0 Low to 14.0 High mA
ATS645LSHTN-I2-T	Yes	Tape and Reel 13-in. 800 pcs./reel	7.0 Low to 14.0 High mA

<sup>1</sup>Pb-based variants are being phased out of the product line.

a. Certain variants cited in this footnote are in production but have been determined to be LAST TIME BUY. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: October 31, 2006. Deadline for receipt of LAST TIME BUY ORDERS: April 27, 2007. These variants include: ATS645LSHTN-I1.

b. Certain variants cited in this footnote are in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 1, 2006. These variants include: ATS645LSHTN-I2.

<sup>2</sup>Contact Allegro for additional packing options.

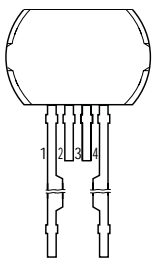
<sup>3</sup>Some restrictions may apply to certain types of sales. Contact Allegro for details.



## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V <sub>CC</sub>		28	–
Reverse-Supply Voltage	V <sub>RCC</sub>		–18	V
Operating Ambient Temperature	T <sub>A</sub>	Range L	–40 to 150	°C
Maximum Junction Temperature	T <sub>J(max)</sub>		165	°C
Storage Temperature	T <sub>stg</sub>		–65 to 170	°C

## Pin-out Diagram



## Terminal List

Name	Description	Number
VCC	Connects power supply to chip	1
NC	No connection	2
TEST	For Allegro use, float or tie to GND	3
GND	Ground terminal	4

OPERATING CHARACTERISTICS using reference target 60-0, $T_A$ and $V_{CC}$ within specification, unless otherwise noted						
CHARACTERISTIC	Symbol	Test Conditions	Min.	Typ. <sup>1</sup>	Max.	Units
<b>ELECTRICAL CHARACTERISTICS</b>						
Supply Voltage <sup>2</sup>	$V_{CC}$	Operating; $T_J < 165\text{ }^\circ\text{C}$	4.0	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	$V_{CC} 0 \rightarrow 5\text{ V}$ and $5 \rightarrow 0\text{ V}$	–	–	4.0	V
Supply Zener Clamp Voltage	$V_Z$	$I_{CC} = I_{CC(max)} + 3\text{ mA}$ ; $T_A = 25\text{ }^\circ\text{C}$	28	–	–	V
Supply Zener Current	$I_Z$	Test conditions only; $V_Z = 28\text{ V}$	–	–	$I_{CC(max)} + 3\text{ mA}$	mA
Supply Current	$I_{CC(Low)}$	ATS645LSH-I1	4.0	6	8.0	mA
		ATS645LSH-I2	5.9	7	8.4	mA
	$I_{CC(High)}$	ATS645LSH-I1	12.0	14.0	16.0	mA
		ATS645LSH-I2	11.8	14.0	16.8	mA
Supply Current Ratio	$I_{CC(High)}/I_{CC(Low)}$	Ratio of high current to low current	1.85	–	3.05	–
<b>POWER-ON STATE CHARACTERISTICS</b>						
Power-On State	POS	$t > t_{PO}$	–	$I_{CC(High)}$	–	–
Power-On Time <sup>3</sup>	$t_{PO}$	Target gear speed $< 100\text{ rpm}$	–	1	2	ms
<b>OUTPUT STAGE</b>						
Output Slew Rate <sup>4</sup>	$dI/dt$	$R_{LOAD} = 100\ \Omega$ , $C_{LOAD} = 10\text{ pF}$	–	10	–	mA/ $\mu\text{s}$

Continued on the next page.

OPERATING CHARACTERISTICS (continued) using reference target 60-0, $T_A$ and $V_{CC}$ within specification, unless otherwise noted						
Characteristic	Symbol	Test Conditions	Min.	Typ. <sup>1</sup>	Max.	Units
<b>SWITCHPOINT CHARACTERISTICS</b>						
Rotation Speed	$S_{ROT}$	Reference Target 60-0	0	–	8,000	rpm
Analog Signal Bandwidth	BW	Equivalent to $f - 3dB$	20	40	–	kHz
Operate Point	$B_{OP}$	Transitioning from $I_{CC(High)}$ to $I_{CC(Low)}$ ; positive peak referenced; $AG < AG_{MAX}$	–	120	–	mV
Release Point	$B_{RP}$	Transitioning from $I_{CC(Low)}$ to $I_{CC(High)}$ ; negative peak referenced; $AG < AG_{MAX}$	–	120	–	mV
<b>CALIBRATION</b>						
Initial Calibration	$C_1$	Quantity of rising output (current) edges required for accurate edge detection	–	–	3	Edge
<b>DAC CHARACTERISTICS</b>						
Allowable User-Induced Differential Offset		Output switching only; may not meet datasheet specifications	–60	–	60	G
<b>FUNCTIONAL CHARACTERISTICS<sup>5</sup></b>						
Operational Air Gap Range <sup>6</sup>	AG	$\Delta DC$ within specification	0.5	–	2.75	mm
Maximum Operational Air Gap Range	$AG_{OP(max)}$	Output switching (no missed edges); $\Delta DC$ not guaranteed	–	–	3	mm
Duty Cycle Variation <sup>7</sup>	$\Delta DC$	Wobble < 0.5mm; Typical value at $AG = 1.5$ mm, for max., min., AG within specification	43	53	63	%
Operating Magnetic Flux Density Differential <sup>8</sup>	$B_{AG(p-p)}$	Operating within specification	30	–	1000	G
Minimum Operating Signal	$Sig_{OP(min)}$	Output switching (no missed edges); $\Delta DC$ not guaranteed	20	–	–	G

<sup>1</sup>Typical values are at  $T_A = 25^\circ C$  and  $V_{CC} = 12$  V. Performance may vary for individual units, within the specified maximum and minimum limits.

<sup>2</sup>Maximum voltage must be adjusted for power dissipation and junction temperature; see *Power Derating* section.

<sup>3</sup>Power-On Time includes the time required to complete the internal automatic offset adjust. The DACs are then ready for peak acquisition.

<sup>4</sup> $dI$  is the difference between 10% of  $I_{CC(Low)}$  and 90% of  $I_{CC(High)}$ , and  $dt$  is time period between those two points.

Note:  $dI/dt$  is dependent upon the value of the bypass capacitor, if one is used.

<sup>5</sup>Functional characteristics valid only if magnetic offset is within the specified range for Allowable User Induced Differential Offset.

<sup>6</sup>AG is dependent on the available magnetic field. The available field is dependent on target geometry and material, and should be independently characterized. The field available from the reference target is given in the reference target parameter section of the datasheet.

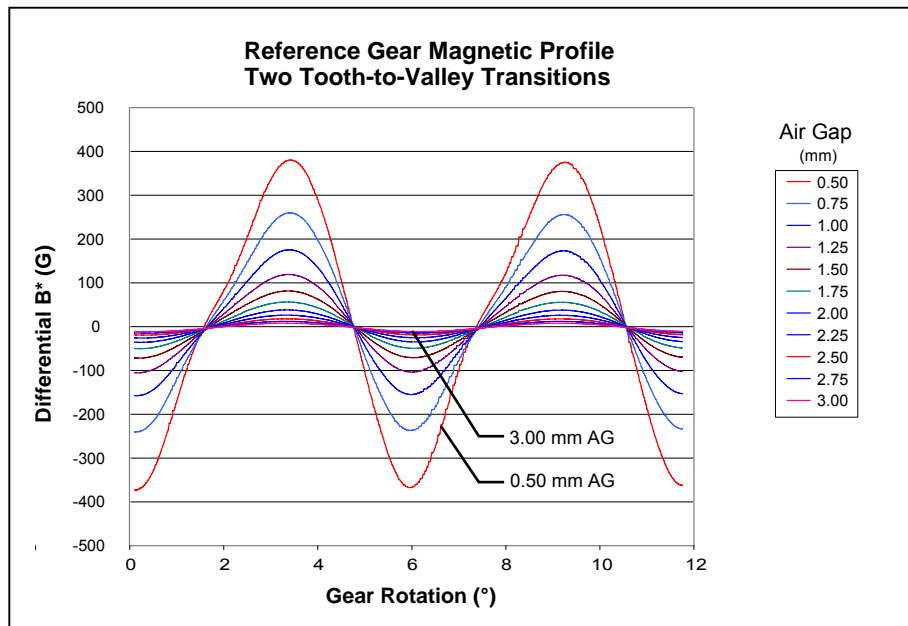
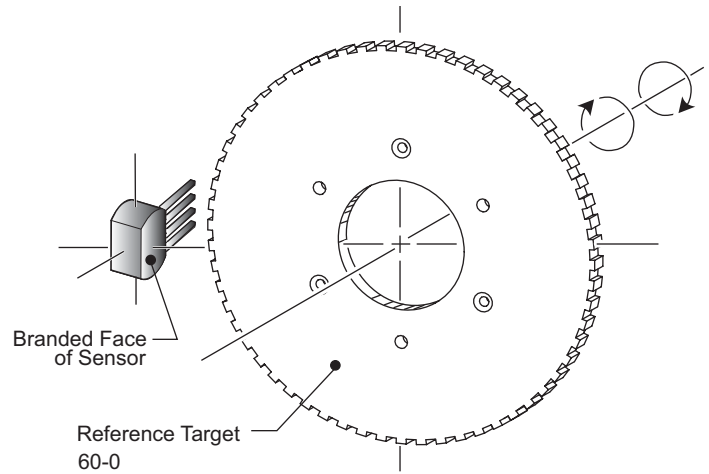
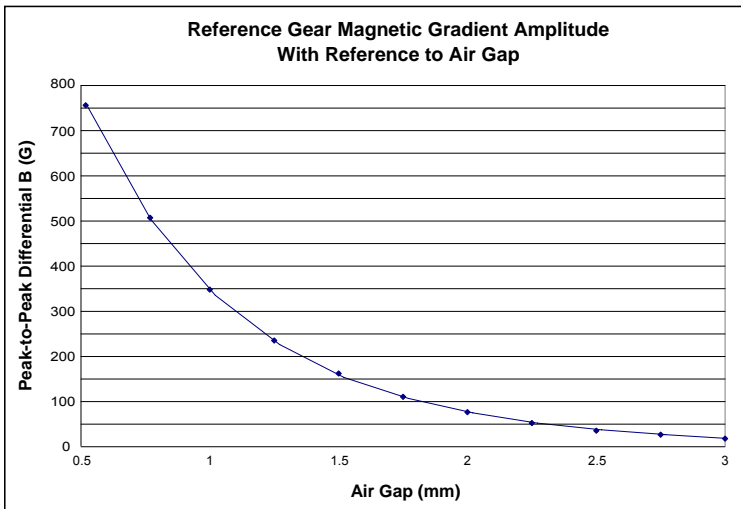
<sup>7</sup>Duty cycle specification may not be met if the magnetic signal during the calibration period is not representative of the installation air gap.

<sup>8</sup>In order to remain in specification, the magnetic gradient must induce an operating signal greater than the minimum value specified. This includes the effect of target wobble.

# True Zero Speed Miniature Differential Peak-Detecting Gear Tooth Sensor

REFERENCE TARGET, 60-0 (60 Tooth Target)

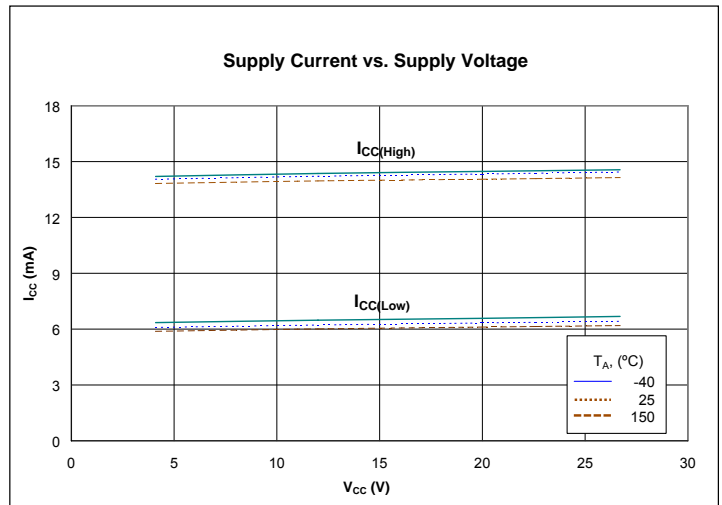
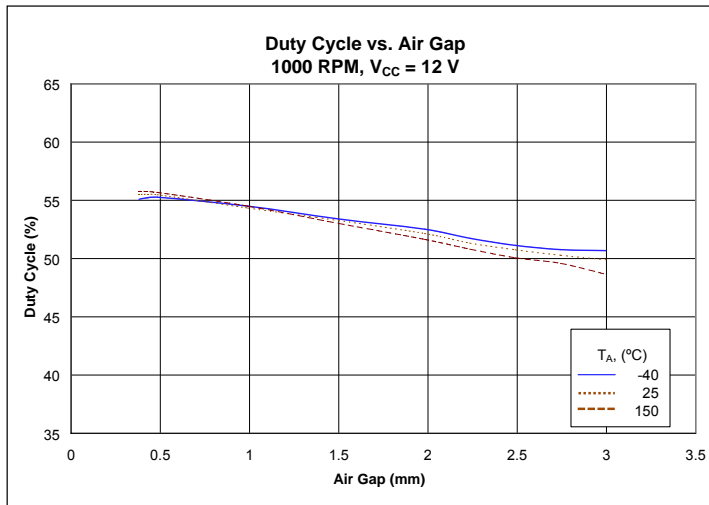
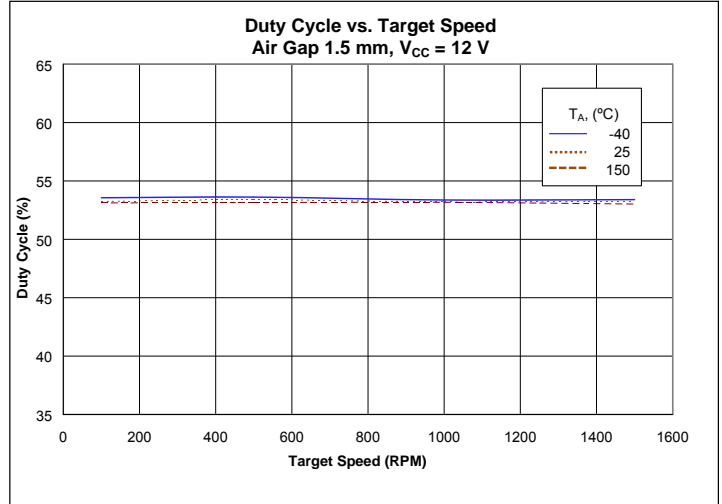
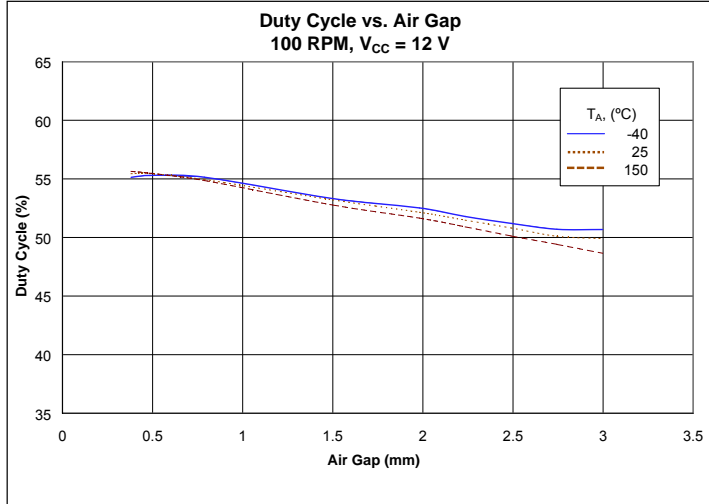
Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	$D_o$	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to sensor	6	mm	
Circular Tooth Length	t	Length of tooth, with respect to sensor; measured at $D_o$	3	mm	
Circular Valley Length	$t_v$	Length of valley, with respect to sensor; measured at $D_o$	3	mm	
Tooth Whole Depth	$h_t$		3	mm	
Material		Low Carbon Steel	-	-	



\*Differential B corresponds to the calculated difference in the magnetic field as sensed simultaneously at the two Hall elements in the device ( $B_{DIFF} = B_{E1} - B_{E2}$ ).

Characteristic Data

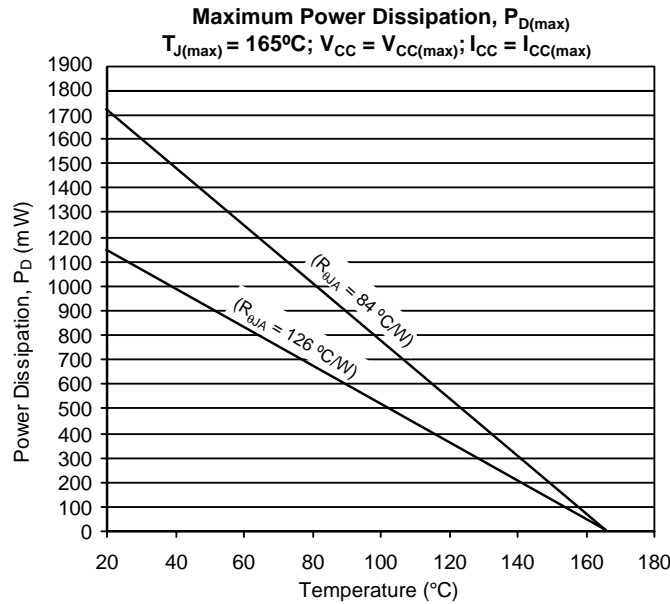
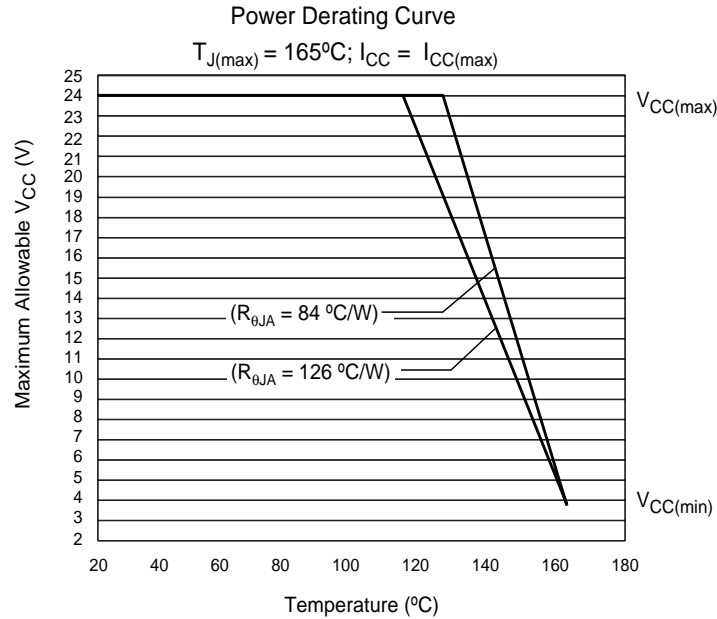
I1 Trim



THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

CHARACTERISTIC	Symbol	TEST CONDITIONS*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Single-layer PCB with copper limited to solder pads	126	$^{\circ}\text{C}/\text{W}$
		Two-layer PCB with 3.8 in. <sup>2</sup> of copper area on each side connected with thermal vias and to device ground pin	84	$^{\circ}\text{C}/\text{W}$

\*Additional information is available on the Allegro Web site.



## Functional Description

### Sensing Technology

The gear tooth sensor subassembly contains a single-chip differential Hall effect sensor IC, an optimized samarium cobalt magnet, and a flat ferrous pole piece. The Hall IC supports two Hall elements, which sense the magnetic profile of the ferrous target simultaneously, but at different points (spaced at a 1.5 mm pitch), generating a differential internal analog voltage ( $V_{PROC}$ ) that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also possesses a temperature compensated amplifier and offset cancellation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset rejection circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

### Target Profiling

An operating device is capable of providing digital information that is representative of the mechanical features on a rotating target. The waveform diagram shown in figure 3 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the sensor.

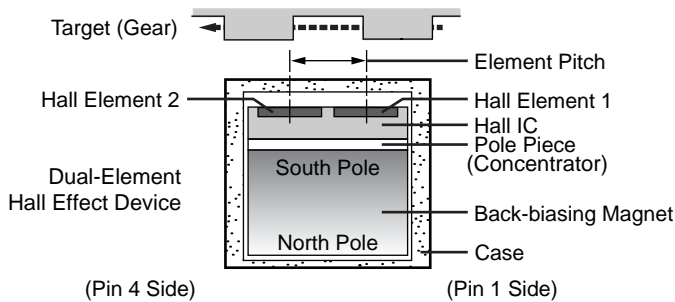


Figure 1. Relative motion of the target is detected by the dual Hall elements mounted on the Hall IC.

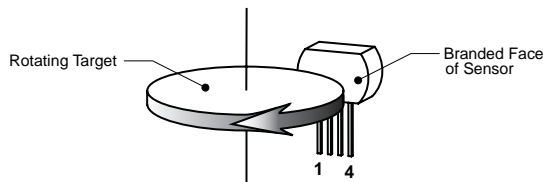


Figure 2. This left-to-right (pin 1 to pin 4) direction of target rotation results in a low output signal when a tooth of the target gear is nearest the face of the sensor (see figure 3). A right-to-left (pin 4 to pin 1) rotation inverts the output signal polarity.

### Output Polarity

Figure 3 shows the output polarity for the orientation of target and sensor shown in figure 2. The target direction of rotation shown is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 4 side. This results in the sensor output switching from high,  $I_{CC(High)}$ , to low  $I_{CC(Low)}$ , as the leading edge of a tooth (a rising mechanical edge, as detected by the sensor) passes the sensor face. In this configuration, the device output current switches to its low polarity when a tooth is the target feature nearest to the sensor. If the direction of rotation is reversed, then the output polarity inverts.

Note that output voltage polarity is dependent on the position of the sense resistor,  $R_{SENSE}$  (see figure 4).

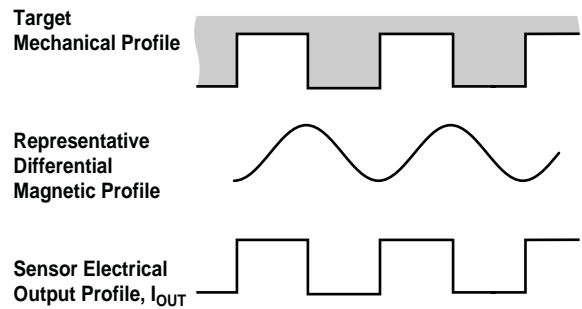


Figure 3. Output Profile of a ferrous target for the polarity indicated in figure 2.

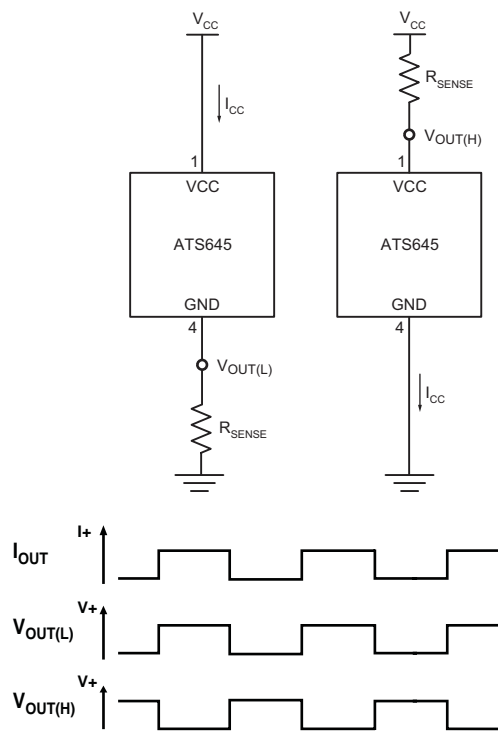


Figure 4: Voltages profiles for high side and low side two-wire sensing.



**Automatic Gain Control (AGC)**

This feature allows the device to operate with an optimal internal electrical signal, regardless of the air gap (within the AG specification). During calibration, the device determines the peak-to-peak amplitude of the signal generated by the target. The gain of the sensor is then automatically adjusted. Figure 5 illustrates the effect of this feature.

**Automatic Offset Adjust (AOA)**

The AOA is patented circuitry that automatically cancels the effects of chip, magnet, and installation offsets. (For capability, see Dynamic Offset Cancellation, in the Operating Characteristics table.) This circuitry is continuously active, including both during calibration mode and running mode, compensating for any offset drift. Continuous operation also allows it to compen-

sate for offsets induced by temperature variations over time.

**Digital Peak Detection**

A digital DAC tracks the internal analog voltage signal  $V_{PROC}$ , and is used for holding the peak value of the internal analog signal. In the example shown in figure 6, the DAC would first track up with the signal and hold the upper peak's value. When  $V_{PROC}$  drops below this peak value by  $B_{OP}$ , the device hysteresis, the output would switch and the DAC would begin tracking the signal downward toward the negative  $V_{PROC}$  peak. Once the DAC acquires the negative peak, the output will again switch states when  $V_{PROC}$  is greater than the peak by the value  $B_{RP}$ . At this point, the DAC tracks up again and the cycle repeats. The digital tracking of the differential analog signal allows the sensor to achieve true zero-speed operation.

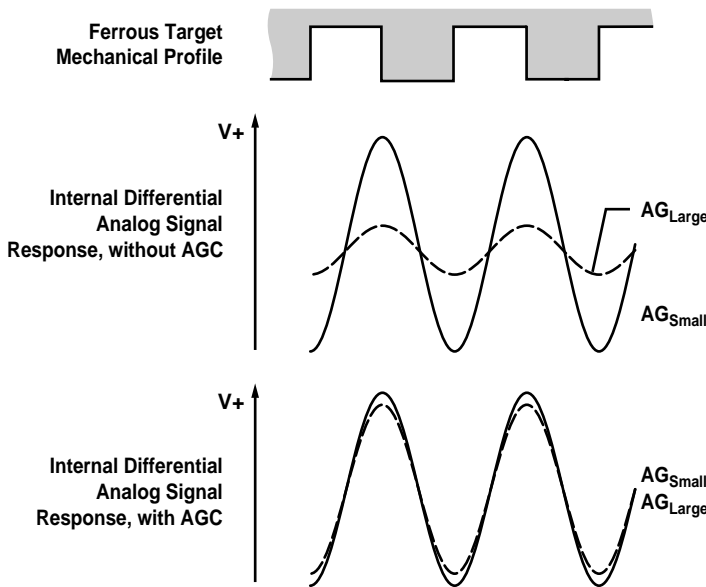


Figure 5. Automatic Gain Control (AGC). The AGC function corrects for variances in the air gap. Differences in the air gap affect the magnetic gradient, but AGC prevents that from affecting device performance, as shown in the lowest panel.

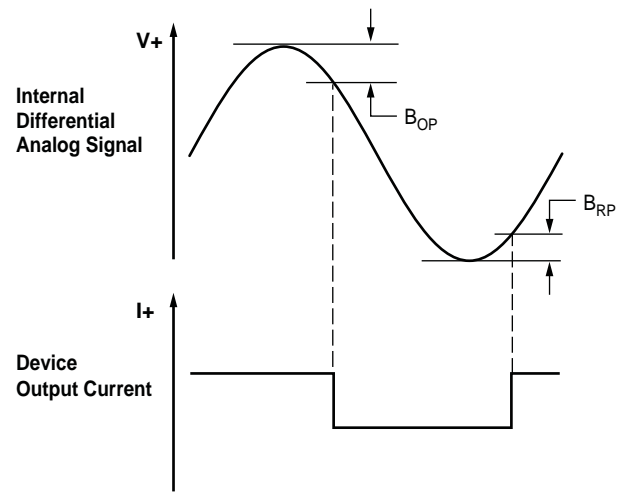


Figure 6: Peak Detecting Switchpoint Detail

**Power Supply Protection**

The device contains an on-chip regulator and can operate over a wide  $V_{CC}$  range. For devices that need to operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection may still be required. Contact Allegro Microsystems for information on the circuitry needed for compliance with various EMC specifications. Refer to figure 7 for an example of a basic application circuit.

**Undervoltage Lockout**

When the supply voltage falls below the undervoltage lockout

voltage,  $V_{CC(UV)}$ , the device enters Reset, where the output state returns to the Power-On State (POS) until sufficient  $V_{CC}$  is supplied.  $I_{CC}$  levels may not meet datasheet limits when  $V_{CC} < V_{CC(min)}$ .

**Assembly Description**

This sensor is integrally molded into a plastic body that has been optimized for size, ease of assembly, and manufacturability. High operating temperature materials are used in all aspects of construction.

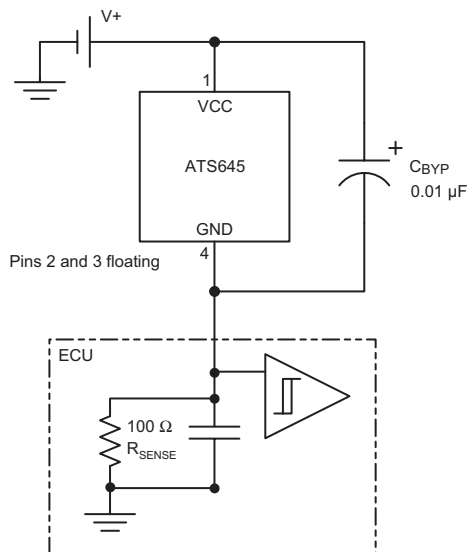


Figure 7: Typical Application Circuit

## **SENSOR OPERATION**

Each operating mode is described in detail below.

### **Power-On**

When power ( $V_{CC} > V_{CCMIN}$ ) is applied to the device, a short period of time is required to power the various portions of the IC. During this period, the ATS645 is guaranteed to power-on in the high current state,  $I_{CC(High)}$ .

### **Initial Offset Adjust**

The sensor initially cancels the effects of chip, magnet, and installation offsets. Once offsets have been cancelled, the digital tracking DAC is ready to track the signal and provide output switching. The period of time required for both Power-On and Initial Offset Adjust is defined as the Power-On Time.

### **Calibration Mode**

The calibration mode allows the sensor to automatically select the proper signal gain and continue to adjust for offsets. The AGC is active, and selects the optimal signal gain based on the amplitude of the  $V_{PROC}$  signal. Following each adjustment to the AGC DAC, the Offset DAC is also adjusted to ensure the

internal analog signal is properly centered.

During this mode, the tracking DAC is active and output switching occurs, but the duty cycle is not guaranteed to be within specification.

### **Diagnostics**

The regulated current output is configured for two wire applications, requiring one less wire for operation than do switches with the more traditional open-collector output. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges. Any current level not within these ranges indicates a fault condition.

### **Running Mode**

After the initial calibration period,  $C_1$ , during which a signal gain is established, the device moves to Running mode. During Running mode, the sensor tracks the input signal and gives an output edge for every peak of the signal. AOA remains active to compensate for any offset drift over time.

Power Derating

The device must be operated below the maximum junction temperature of the device,  $T_{J(max)}$ . Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating  $T_J$ . (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance,  $R_{\theta JA}$ , is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity,  $K$ , of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case,  $R_{\theta JC}$ , is relatively small component of  $R_{\theta JA}$ . Ambient air temperature,  $T_A$ , and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation,  $P_D$ ), can be estimated. The following formulas represent the fundamental relationships used to estimate  $T_J$ , at  $P_D$ .

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as:  $T_A = 25^\circ C$ ,  $V_{CC} = 12 V$ ,  $I_{CC} = 4 mA$ , and  $R_{\theta JA} = 140^\circ C/W$ , then:

$$P_D = V_{CC} \times I_{CC} = 12 V \times 4 mA = 48 mW$$

$$\Delta T = P_D \times R_{\theta JA} = 48 mW \times 140^\circ C/W = 7^\circ C$$

$$T_J = T_A + \Delta T = 25^\circ C + 7^\circ C = 32^\circ C$$

A worst-case estimate,  $P_{D(max)}$ , represents the maximum allowable power level ( $V_{CC(max)}$ ,  $I_{CC(max)}$ ), without exceeding  $T_{J(max)}$ , at a selected  $R_{\theta JA}$  and  $T_A$ .

*Example:* Reliability for  $V_{CC}$  at  $T_A = 150^\circ C$ , package SH (I1 trim), using minimum-K PCB

Observe the worst-case ratings for the device, specifically:  $R_{\theta JA} = 126^\circ C/W$ ,  $T_{J(max)} = 165^\circ C$ ,  $V_{CC(max)} = 24 V$ , and  $I_{CC(max)} = 16 mA$ .

Calculate the maximum allowable power level,  $P_{D(max)}$ . First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165^\circ C - 150^\circ C = 15^\circ C$$

This provides the allowable increase to  $T_J$  resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15^\circ C \div 126^\circ C/W = 119 mW$$

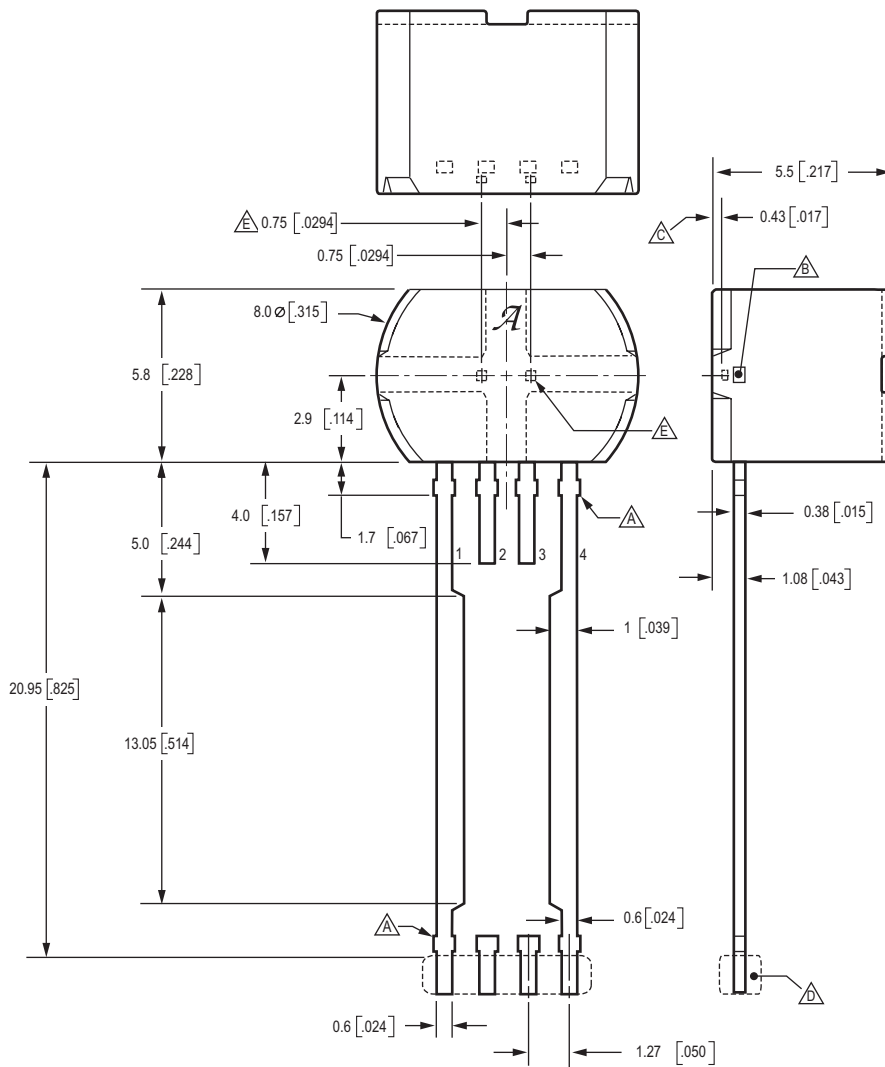
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 119 mW \div 16 mA = 7 V$$

The result indicates that, at  $T_A$ , the application and device can dissipate adequate amounts of heat at voltages  $\leq V_{CC(est)}$ .

Compare  $V_{CC(est)}$  to  $V_{CC(max)}$ . If  $V_{CC(est)} \leq V_{CC(max)}$ , then reliable operation between  $V_{CC(est)}$  and  $V_{CC(max)}$  requires enhanced  $R_{\theta JA}$ . If  $V_{CC(est)} \geq V_{CC(max)}$ , then operation between  $V_{CC(est)}$  and  $V_{CC(max)}$  is reliable under these conditions.

Package SH Module



- Dimensions in millimeters. Untoleranced dimensions are nominal.  
 U.S. Customary dimensions (in.) in brackets, for reference only
- ▲ Dambar removal protrusion (16X)
  - ▲ Metallic protrusion, electrically connected to pin 4 and substrate (both sides)
  - ▲ Active Area Depth
  - ▲ Thermoplastic Molded Lead Bar for alignment during shipment
  - ▲ Hall elements (2X); controlling dimension inches

*The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.*

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