STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT SERIES 7ch Stepping Motor Driver

TYPE BD6889GU

FEATURES
- Built in 6 Full-ON Driver
- Built in 1 Linear Constant-Current Driver
- Built in 4 Digital transistor (NPN)
- Built in 4 Digital transistor (PNP)
- Built in 1 Regulator for PI

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power supply voltage	VCC	-0.5 to +7.0	V
Motor power supply voltage	VM	-0.5 to +7.0	V
Control input voltage	VIN	-0.5 to VCC+0.5	V
Power dissipation	Pd	980※1	mW
Operating temperature range	Topr	-25 to +85	°C
Junction temperature	Tjmax	150	°C
Storage temperature range	Tstg	-55 to +150	°C
H-bridge output current	Iout	-800 to +800※2	mA

※1 Reduced by 7.84mW/°C over 25°C, when mounted on a glass epoxy board (70mm × 70mm × 1.6mm).

※2 Must not exceed Pd, ASO, or Tjmax of 150°C.

●Operating Conditions (Ta=-25°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	2.5	3.0	5.7	V
Motor power supply voltage	VM	2.5	5.0	5.7	V
Control input voltage	VIN	0	-	VCC	V
H-bridge output current	Iout	-	-	±500※3	mA
Logic input freqency	FIN	0	-	100	kHz

※3 Must not exceed Pd or ASO.

This product isn't designed for protection against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

●Package Outline

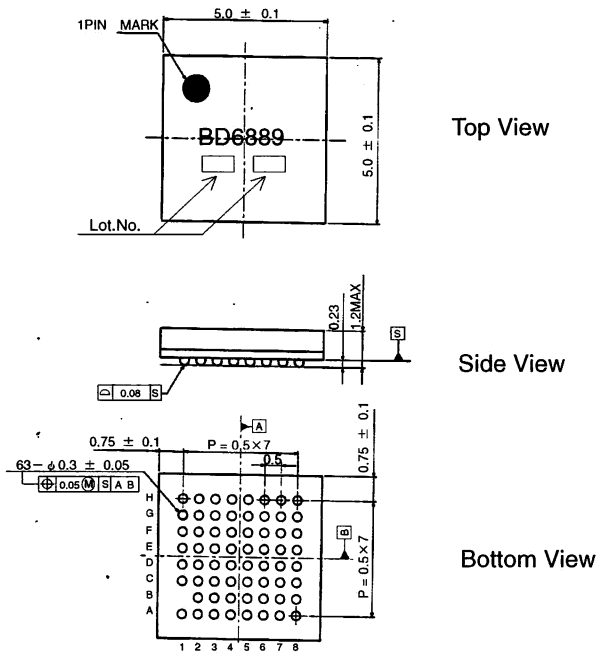

Fig.1 VBGA063W050 package (Unit: mm)

●Block Diagram

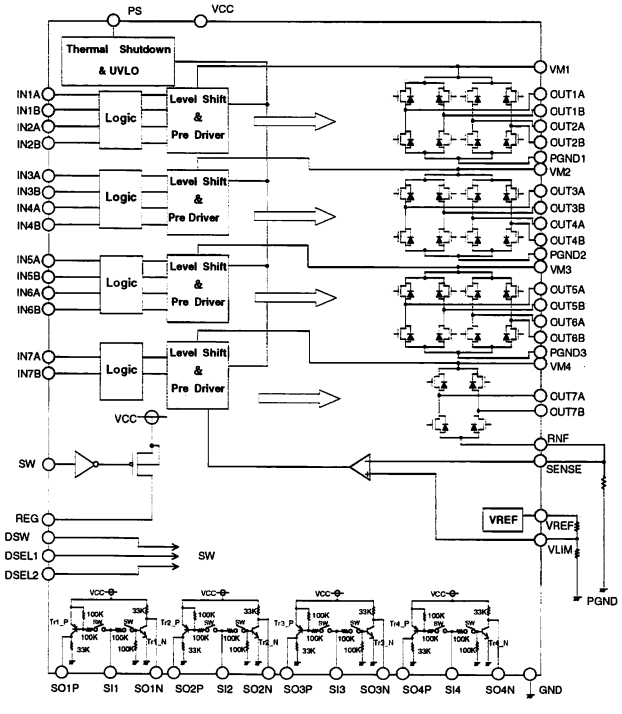

Fig.3 BD6889GU Block Diagram

●Pin Arrangement (Top View)

	1	2	3	4	5	6	7	8
A	N.C.	OUT6A	OUT6B	VM3	PGND3	OUT5B	OUT5A	N.C.
B		DSW	IN6A	IN6B	SO4P	SO4N	REG	OUT4A
C	OUT7A	SW	DSEL2	IN7A	SI4	IN5A	PS	OUT4B
D	VM4	VCC	VREF	IN7B	IN5B	SI3	SO3P	VM2
E	RNF	DSEL1	IN1A	IN1B	IN4B	IN4A	SO3N	PGND2
F	SENSE	VLIM	IN2A	SI1	SI2	IN3A	IN3B	OUT3B
G	OUT7B	GND	IN2B	SO1P	SO1N	SO2P	SO2N	OUT3A
H	N.C.	OUT1A	OUT1B	PGND1	VM1	OUT2B	OUT2A	N.C.

Fig.2 BD6889GU Pin Arrangement (Top View)

●Pin No. and Pin Name

No.	Pin name	No.	Pin name	No.	Pin name
1A	N.C.	1D	VM4	1G	OUT7B
2A	OUT6A	2D	VCC	2G	GND
3A	OUT6B	3D	VREF	3G	IN2B
4A	VM3	4D	IN7B	4G	SO1P
5A	PGND3	5D	IN5B	5G	SO1N
6A	OUT5B	6D	SI3	6G	SO2P
7A	OUT5A	7D	SO3P	7G	SO2N
8A	N.C.	8D	VM2	8G	OUT3A
1B		1E	RNF	1H	N.C.
2B	DSW	2E	DSEL1	2H	OUT1A
3B	IN6A	3E	IN1A	3H	OUT1B
4B	IN6B	4E	IN1B	4H	PGND1
5B	SO4P	5E	IN4B	5H	VM1
6B	SO4N	6E	IN4A	6H	OUT2B
7B	REG	7E	SO3N	7H	OUT2A
8B	OUT4A	8E	PGND2	8H	N.C.
1C	OUT7A	1F	SENSE		
2C	SW	2F	VLIM		
3C	DSEL2	3F	IN2A		
4C	IN7A	4F	SI1		
5C	SI4	5F	SI2		
6C	IN5A	6F	IN3A		
7C	PS	7F	IN3B		
8C	OUT4B	8F	OUT3B		

●H-Bridge Driver I/O Truth Table

Full-ON Driver ch1 to ch6 I/O Turn Table

Input mode	INPUT		OUTPUT	
	INxA	INxB	OUTxA	OUTxB
IN/IN	L	L	Z	Z
	L	H	L	H
	H	L	H	L
	H	H	L	L

Linear Constant-Current Driver ch7 I/O Truth Table

Input mode	INPUT		OUTPUT	
	IN7A	IN7B	OUT7A	OUT7B
EN/IN	L	X	Z	Z
	H	L	H	L
	H	H	L	H

H : High, L : Low, X : Don't care, Z : Hi impedance

●Regulator for PI I/O Truth Table

	INPUT	OUTPUT
	SW	REG
Logic	L	OFF
	H	ON

●Digital Transistor I/O Truth Table

	INPUT			OUTPUT							
	DSW	DSEL1	DSEL2	Tr1_P	Tr1_N	Tr2_P	Tr2_N	Tr3_P	Tr3_N	Tr4_P	Tr4_N
Logic	L	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
	H	L	L	OFF	ON	OFF	ON	OFF	ON	OFF	ON
	H	L	H	OFF	ON	OFF	ON	ON	OFF	ON	OFF
	H	H	L	ON	OFF	ON	OFF	OFF	ON	OFF	ON
	H	H	H	ON	OFF	ON	OFF	ON	OFF	ON	OFF

● BD6889GU Electrical Characteristics (Unless otherwise specified, Ta=25°C, VCC=3.0V, VM=5.0V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Overall						
Circuit current during standby operation	ICCST	-	0	10	μA	PS=L
Circuit current	ICC	-	1.5	3	mA	PS=H with no signal
Control input						
High level input voltage	VINH	2.0	-	-	V	IN1A~IN7B, PS
Low level input voltage	VINL	-	-	0.7	V	IN1A~IN7B, PS
High level input current	IINH	15	30	60	μA	IN1A~IN7B, PS; VIN=3V
Low level input current	IINL	-1	0	-	μA	IN1A~IN7B, PS; VIN=0V
Pull-down resistor	RIN	50	100	200	kΩ	
UVLO						
UVLO voltage	VUVLO	1.6	-	2.4	V	
Full-ON Drive block (ch1 to ch6)						
Output ON-Resistance	RON	-	1.3	1.6	Ω	Io=±400mA on high and low sides in total
Pulse input response	tp	100	-	-	ns	With an input pulse with of 200ns
Linear Constant-Current Drive block (ch7)						
Output ON-Resistance	RON	-	0.9	1.1	Ω	Io=±400mA on high and low sides in total
VREF output voltage	VREF	0.88	0.90	0.92	V	Iout=0~1mA
Output limit current 1	VOL1	388	400	412	mA	RNF=0.5Ω with a load of 10Ω, VLIM=0.2V
Output limit current 2	VOL2	285	300	315	mA	RNF=0.5Ω with a load of 10Ω, VLIM=0.15V
Output limit current 3	VOL3	190	200	210	mA	RNF=0.5Ω with a load of 10Ω, VLIM=0.1V
Digital transistor block for waveform shaping (NPN)						
Input current	ISIH	-	-	0.1	mA	SIx=3V
Low level output voltage	VSOL	-	0.1	0.25	V	SIx=3V, ISO=0.5mA
Input dividing resistance	RSIL	70	100	130	kΩ	
Output pull-up resistance	RSOH	-	33	-	kΩ	
Input dividing comparison	-	0.8	1	1.2	-	Division comparison between SIx and GND*4

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Digital transistor block for waveform shaping (PNP)						
Input current	ISIL	-0.1	-	-	mA	SIx=0V
High level output voltage	VSOH	VCC -0.25	VCC -0.1	-	V	SIx=0V, ISO=-0.5mA
Input dividing resistance	RSIP	70	100	130	kΩ	
Output pull-down resistance	RSOL	-	33	-	kΩ	
Input dividing comparison	-	0.8	1	1.2	-	Division comparison between SIx and VCC※4
Regulator for PI						
Output H voltage	VREGH	VCC -0.25	VCC -0.2	-	V	SW=VCC, IREG=100mA
Output ON-Resistance	RONREG	-	2	2.5	kΩ	SW=VCC, IREG=100mA
Output leak current	ILPI	-	0	1	μA	SW=VCC

※4 Design target value (No total shipment inspection is made.)

●Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Power supply lines

Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may loose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) ASO

When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

(7) Thermal shutdown circuit

This IC incorporates a TSD (thermal shutdown) circuit (TSD circuit). If the temperature of the chip reaches the following temperature, the motor coil output will be opened. The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

TSD ON temperature [°C] (Typ.)	Hysteresis temperature [°C] (Typ.)
175	25

(8) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

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