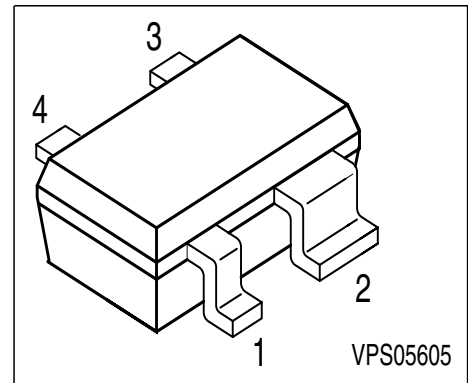
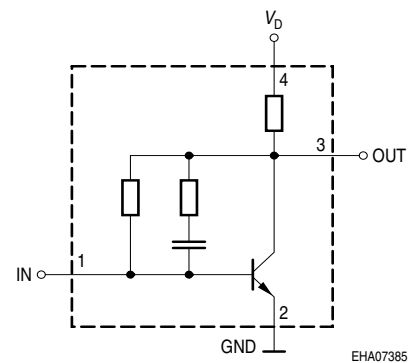


Si-MMIC-Amplifier in SIEGET 25-Technologie

- Cascadable 50 Ω-gain block
- Unconditionally stable
- Gain  $|S_{21}|^2 = 13$  dB at 1.8 GHz  
 $IP_{3out} = +13$  dBm at 1.8 GHz  
 $(V_D = 3$  V,  $I_D =$  typ. 6.7 mA)
- Noise figure  $NF = 2.3$  dB at 1.8 GHz
- Reverse isolation  $> 28$  dB and  
return loss  $IN / OUT > 12$  dB at 1.8 GHz



Circuit Diagram



**ESD:** Electrostatic discharge sensitive device, observe handling precaution!

Type	Marking	Pin Configuration				Package
BGA420	BLs	1, IN	2, GND	3, OUT	4, VD	SOT343

Maximum Ratings

Parameter	Symbol	Value	Unit
Device current	$I_D$	15	mA
Device voltage	$V_D$	6	V
Total power dissipation $T_S = 110$ °C	$P_{tot}$	90	mW
RF input power	$P_{RFIn}$	0	dBm
Junction temperature	$T_j$	150	°C
Ambient temperature	$T_A$	-65 ... 150	
Storage temperature	$T_{stg}$	-65 ... 150	

Thermal Resistance

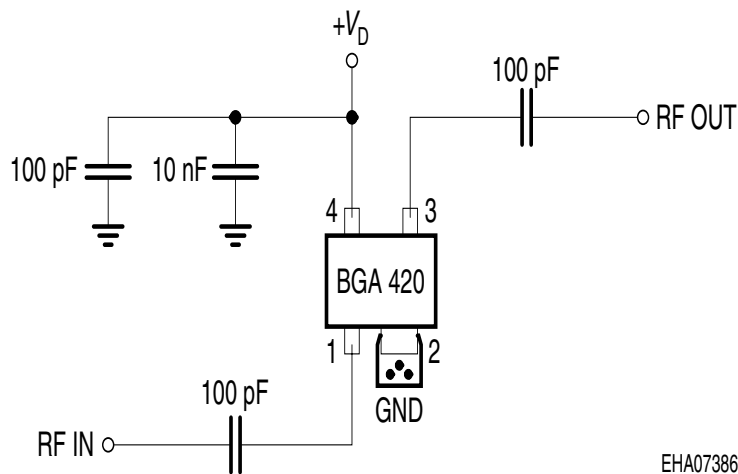
Junction - soldering point <sup>1)</sup>	$R_{thJS}$	$\leq 410$	K/W
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<sup>1)</sup>For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

Electrical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>AC characteristics</b> $V_D = 3\text{ V}$ , $Z_0 = 50\ \Omega$					
Device current	$I_D$	5.4	6.7	8	mA
Insertion power gain	$ S_{21} ^2$				dB
$f = 0.1\text{ GHz}$		17	19	-	
$f = 1\text{ GHz}$		15	17	-	
$f = 1.8\text{ GHz}$		11	13	-	
Reverse isolation	S12	25	28	-	dBm
$f = 1.8\text{ GHz}$					
Noise figure	NF				
$f = 0.1\text{ GHz}$		-	1.9	2.3	
$f = 1\text{ GHz}$		-	2.2	2.6	
$f = 1.8\text{ GHz}$		-	2.3	2.7	
Intercept point at the output	$IP_{3out}$	10	13	-	dBm
$f = 1\text{ GHz}$					
1dB compression point	$P_{-1dB}$	-6	-2.5	-	dB
$f = 1\text{ GHz}$					
Return loss input	$RL_{in}$	8	11	-	dB
$f = 1.8\text{ GHz}$					
Return loss output	$RL_{out}$	12	16	-	
$f = 1.8\text{ GHz}$					

**Typical biasing configuration**



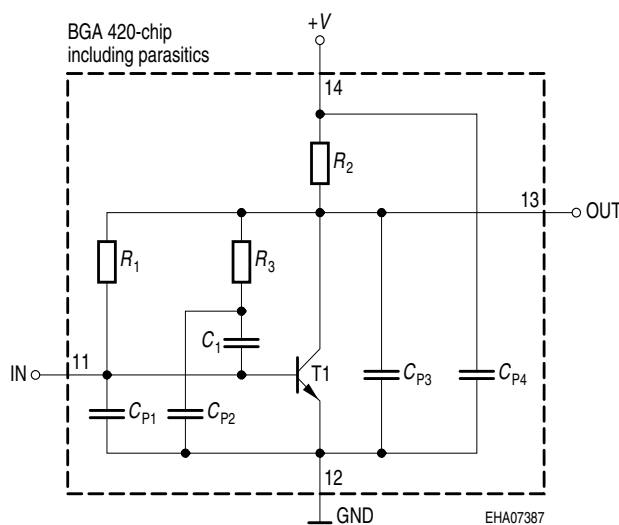
EHA07386

- Note: 1) Large-value capacitors should be connected from pin 4 to ground right at the device to provide a low impedance path.  
 2) The use of plated through holes right at pin 2 is essential for pc-board-applications. Thin boards are recommended to minimize the parasitic inductance to ground.

**Typical S-Parameters at  $T_A = 25\text{ }^\circ\text{C}$**

$f$ GHz	$S_{11}$		$S_{21}$		$S_{12}$		$S_{22}$	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
$V_D = 3\text{ V}, Z_0 = 50\text{ }\Omega$								
0.1	0.5686	-8.5	9.314	170.6	0.0268	12.7	0.2808	-8.6
0.5	0.5066	-19.2	8.393	149.4	0.0248	11.7	0.2613	-3.8
0.8	0.4404	-28.7	7.352	135.2	0.0236	25.6	0.2361	-6.7
1	0.3904	-34.6	6.69	126.8	0.024	35.9	0.2144	-9
1.5	0.2841	-50.5	5.244	111.1	0.0314	57.2	0.1398	-15
1.8	0.2343	-60.6	4.567	104	0.0378	63.5	0.0979	-18.2
1.9	0.2136	-64.1	4.355	102	0.0406	66.1	0.0838	-21.5
2	0.2062	-68.4	4.165	99.7	0.0426	67.2	0.0689	-22.2
2.4	0.1688	-89.7	3.417	91.7	0.0549	71.4	0.0224	-48
3	0.1558	-104.9	2.861	85.3	0.0682	73.1	0.0284	-147.5

**Spice-model BGA 420**



T1	T501
$R_1$	14.5k $\Omega$
$R_2$	140 $\Omega$
$R_3$	2.4k $\Omega$
$C_1$	2.3pF
$C_{P1}$	0.2pF
$C_{P2}$	0.2pF
$C_{P3}$	0.6pF
$C_{P4}$	0.1pF

**Transistor Chip Data T1 (Berkley-SPICE 2G.6 Syntax) :**

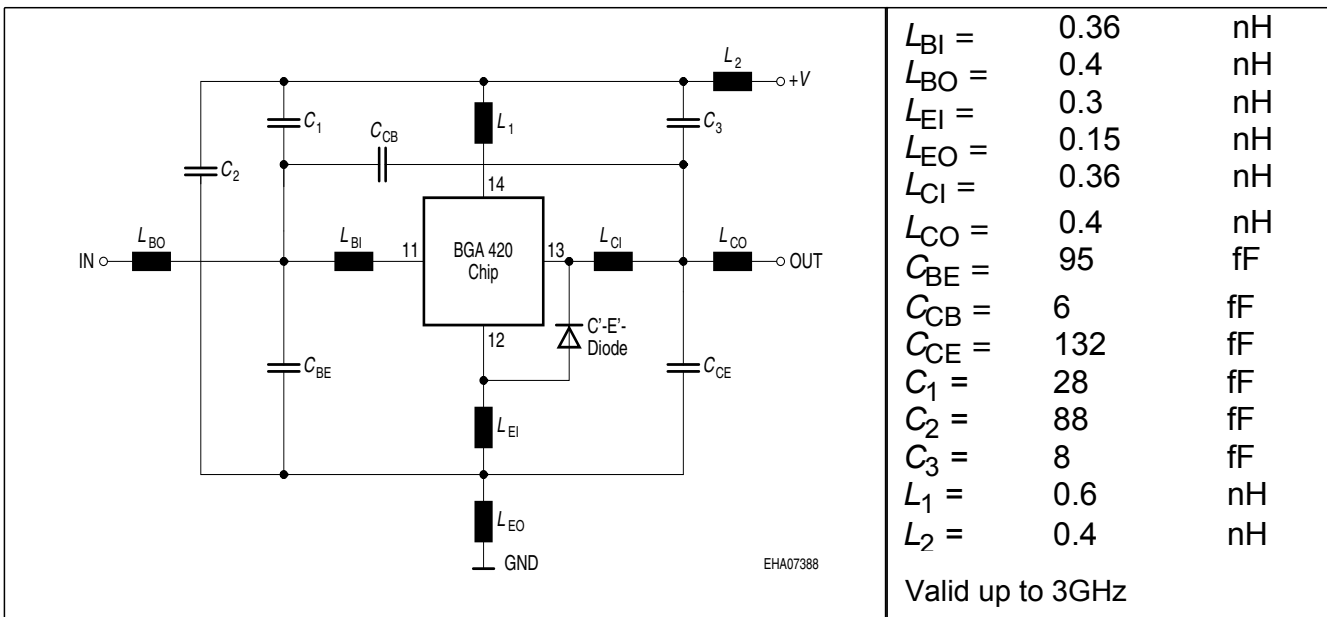
IS =	0.21024	fA	BF =	83.23	-	NF =	1.0405	-
VAF =	39.251	V	IKF =	0.16493	A	ISE =	15.761	fA
NE =	1.7763	-	BR =	10.526	-	NR =	0.96647	-
VAR =	34.368	V	IKR =	0.25052	A	ISC =	0.037223	fA
NC =	1.3152	-	RB =	15	$\Omega$	IRB =	0.21215	A
RBM =	1.3491	$\Omega$	RE =	1.9289		RC =	0.12691	$\Omega$
CJE =	3.7265	fF	VJE =	0.70367	V	MJE =	0.37747	-
TF =	4.5899	ps	XTF =	0.3641	-	VTF =	0.19762	V
ITF =	1.3364	mA	PTF =	0	deg	CJC =	96.941	fF
VJC =	0.99532	V	MJC =	0.48652	-	XCJC =	0.08161	-
TR =	1.4935	ns	CJS =	0	fF	VJS =	0.75	V
MJS =	0	-	XTB =	0	-	EG =	1.11	eV
XTI =	3	-	FC =	0.99469	-	TNOM	300	K

**C'-E'-Diode Data (Berkley-SPICE 2G.6 Syntax) :**

IS =	2	fA	N =	1.02	-	RS =	20	$\Omega$
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All parameters are ready to use, no scaling is necessary

**Package Equivalent Circuit:**

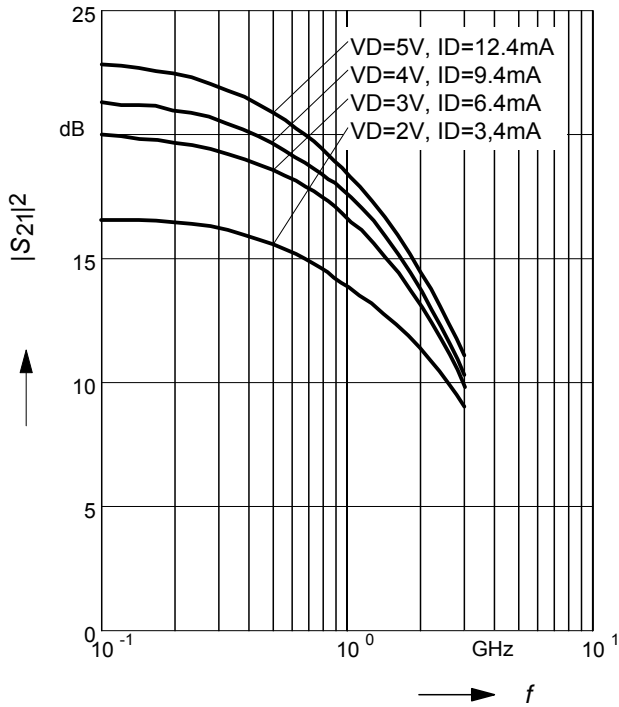


Extracted on behalf of Infineon Technologies AG by:  
 Institut für Mobil-und Satellitentechnik (IMST)

For examples and ready to use parameters please contact your local Infineon Technologies distributor or sales office to obtain a Infineon Technologies CD-ROM or see Internet:  
<http://www.infineon.com/silicondiscretes>

**Insertion power gain  $|S_{21}|^2 = f(f)$**

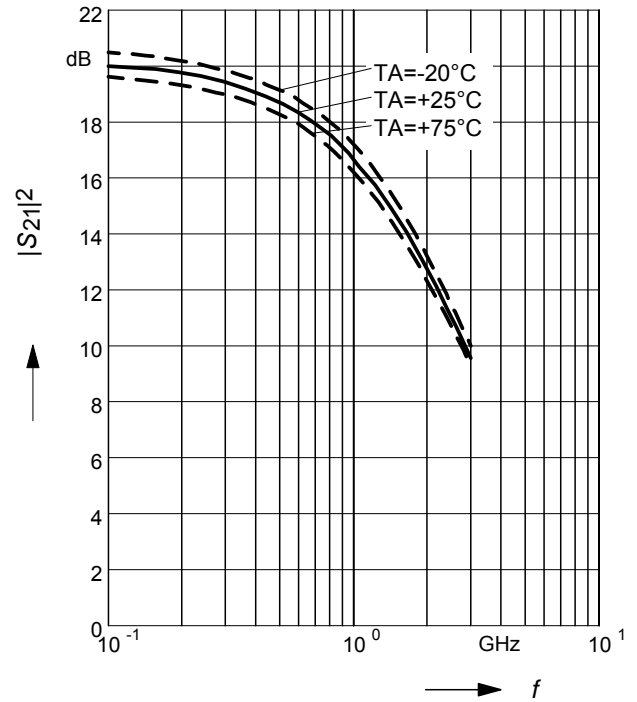
$V_D, I_D = \text{parameter}$



**Insertion power gain  $|S_{21}|^2 = f(f)$**

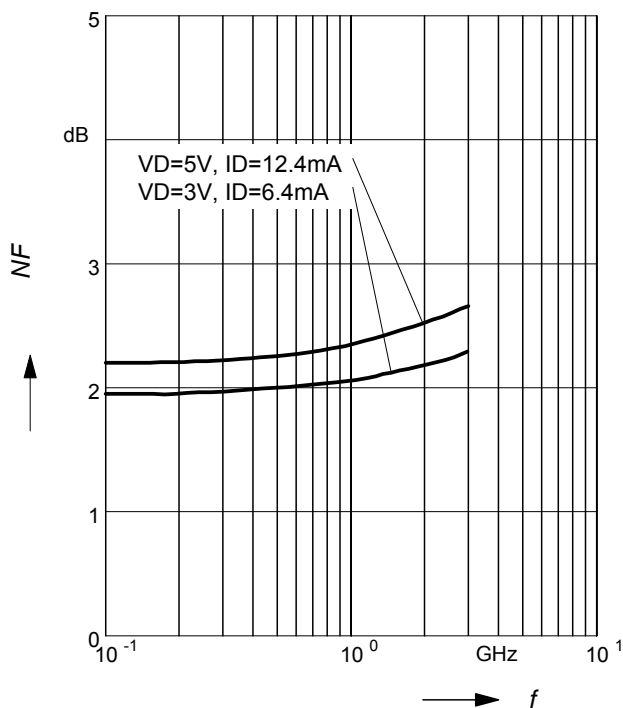
$V_D = 3V$

$T_A = \text{parameter}$



**Noise figure  $NF = f(f)$**

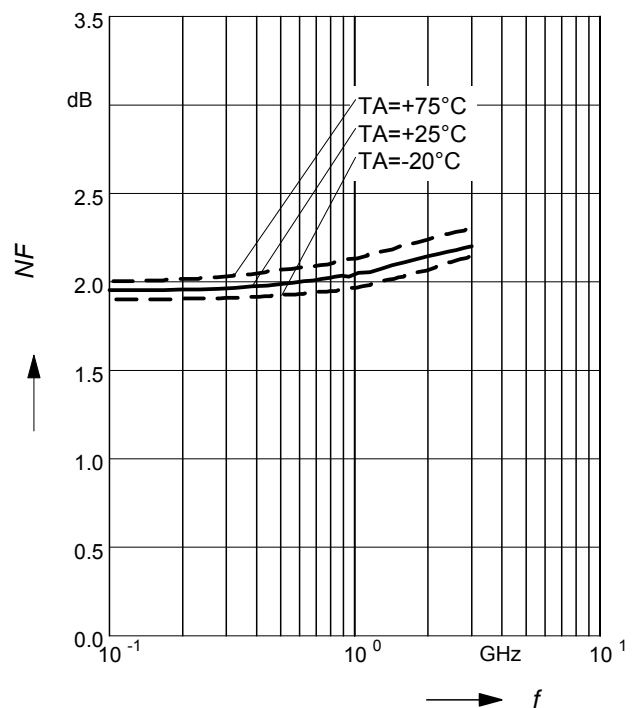
$V_D, I_D = \text{parameter}$



**Noise figure  $NF = f(f)$**

$V_D = 3V$

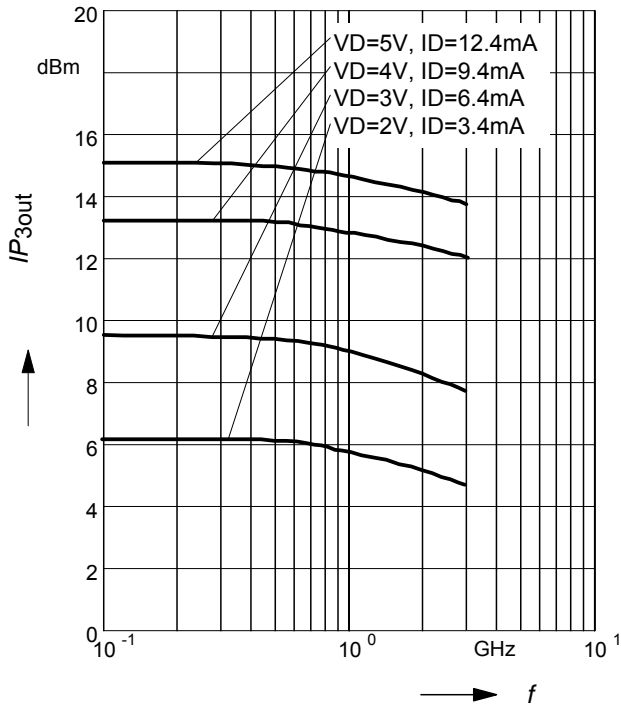
$T_A = \text{parameter}$



**Intercept point at the output**

$IP_{3out} = f(f)$

$V_D, I_D = \text{parameter}$



**Intercept point at the output**

$IP_{3out} = f(f), V_D = 3V$

$T_A = \text{parameter}$

