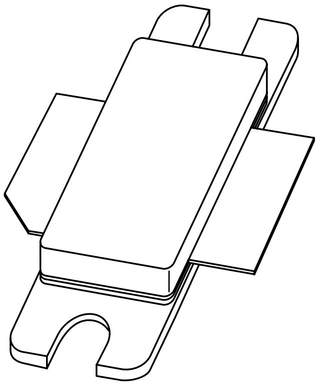
DATA SHEET



BLF1049
Base station LDMOS transistor

Product specification
Supersedes data of 2001 Dec 05

2003 May 14

Philips Semiconductors

PHILIPS

FEATURES

- Typical performance at a supply voltage of 27 V:
  - 1-tone CW; I_{DQ} = 1000 mA
  - Output power = 125 W
  - Gain = 16.5 dB
  - Efficiency = 54%
  - EDGE output power = 45 W (AV)
  - ACPR400 = –64 dBc at 400 kHz (EDGE; I_{DQ} = 750 mA)
  - EVM = 2% rms (AV) (EDGE; I_{DQ} = 750 mA)
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (800 to 1000 MHz)
- Internally matched for ease of use.

APPLICATIONS

- RF power amplifier for GSM, EDGE and CDMA base stations and multicarrier applications in the 800 to 1000 MHz frequency range.

DESCRIPTION

125 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange

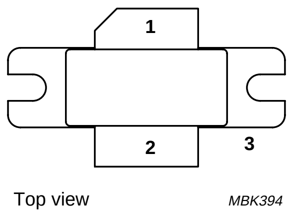


Fig.1 Simplified outline SOT502A .

QUICK REFERENCE DATA

Typical RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dBc)	ACPR 400 (dBc)	EVM % rms (AV)
2-tone	920	125 (PEP)	15.5	37	–32	–	–
1-tone CW		125	16.5	54	–	–	–
GSM EDGE		45 (AV)	15	32	–	–64	2

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	75	V
V_{GS}	gate-source voltage	–	±15	V
T_{stg}	storage temperature	–65	150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	T_h = 25 °C, P_L = 35 W (AV), note 1	0.42	K/W
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_h = 25 °C, P_L = 35 W (AV), note 2	0.62	K/W

Notes

1. Thermal resistance is determined under RF operating conditions.
2. Depending on mounting condition in application.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 3 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 36 V	–	–	3	μA
I_{DSX}	on-state drain current	$V_{GS} = V_{GSth}$ + 9 V; V_{DS} = 10 V	45	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	μA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10 A	–	9	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = 9 V; I_D = 10 A	–	60	–	mΩ

APPLICATION INFORMATION

RF performance in a common source class-AB circuit; V_{DS} = 27 V; T_h = 25 °C; unless otherwise specified.

Mode of operation: 2-tone CW, 100 kHz spacing; I_{DQ} = 1130 mA; f = 890 MHz

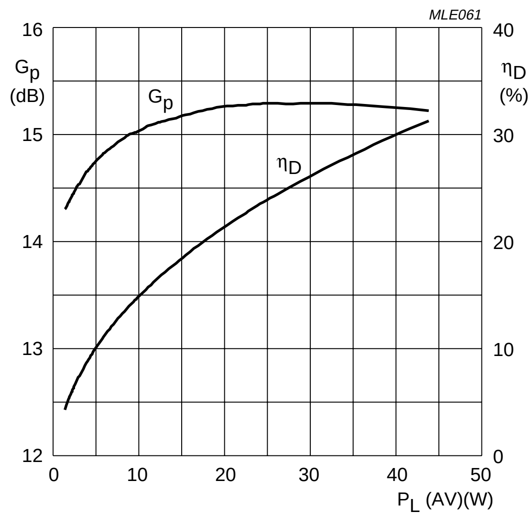
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_p	gain power	P_L = 125 W (PEP)	14.6	15.5	–	dB
η_D	drain efficiency		33	37	–	%
IRL	input return loss		–	–12	–6	dB
d_3	third order inter modulation distortion		–	–32	–25	dBc

Mode of operation: GSM EDGE; I_{DQ} = 750 mA; f = 920 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_p	gain power	P_L = 45 W (AV)	–	15	–	dB
η_D	drain efficiency		–	32	–	%
ACPR 400	adjacent channel power ratio		–	–64	–	dBc
EVM (AV)	EVM rms average signal distortion		–	2	–	%
EVM peak	EVM rms peak signal distortion		–	2.2	–	%

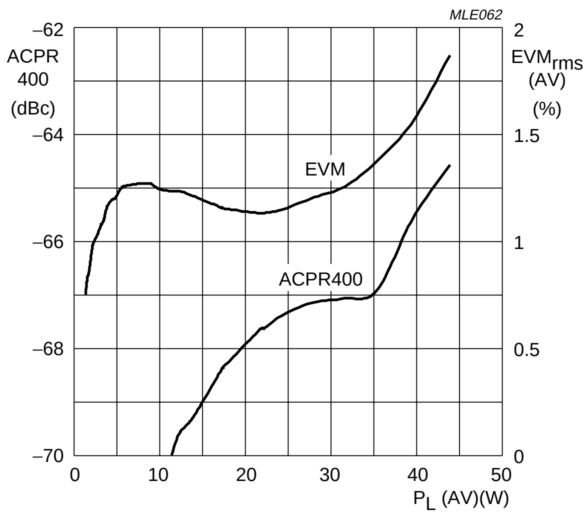
Mode of operation: 1-tone CW; I_{DQ} = 1000 mA; f = 920 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_p	gain power	$P_L = P_{L\ 1\ dB}$ = 125 W	–	16.5	–	dB
η_D	drain efficiency		–	54	–	%



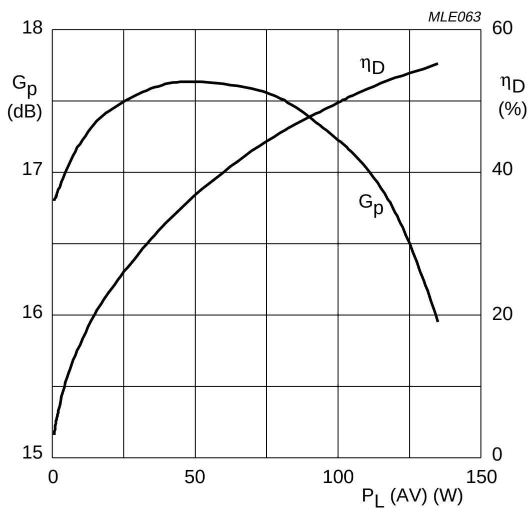
V_{DS} = 27 V; f = 920 MHz; I_{DQ} = 750 mA; $T_h \leq 25$ °C.

Fig.2 GSM EDGE power gain and efficiency as functions of load power; typical values.



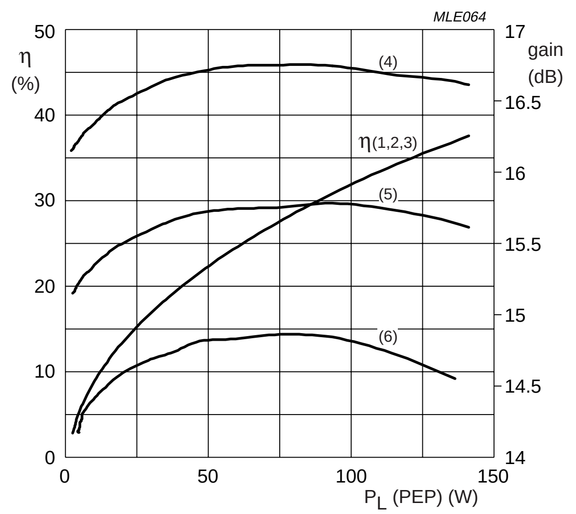
V_{DS} = 27 V; f = 920 MHz; I_{DQ} = 750 mA; $T_h \leq 25$ °C.

Fig.3 GSM EDGE ACPR400 and EVM as functions of average load power; typical values.



V_{DS} = 27 V; f = 920 MHz; I_{DQ} = 1000 mA;

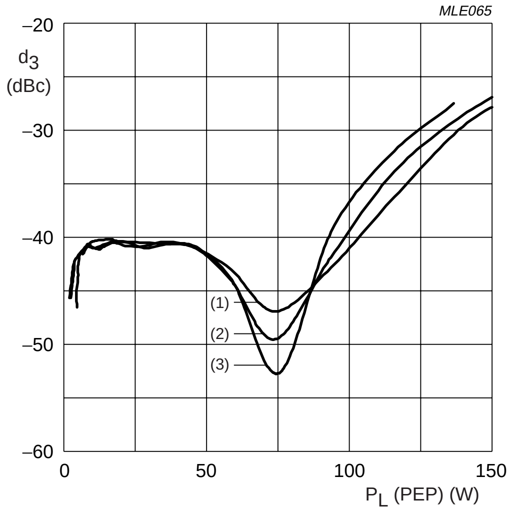
Fig.4 1-tone CW power gain and efficiency as functions of load power; typical values.



V_{DS} = 27 V; I_{DQ} = 1.1 A; f_1 = 920.0 MHz; f_2 = 920.1 MHz.

(1) η at T_h = –40 °C.
(2) η at T_h = 20 °C.
(3) η at T_h = 80 °C.
(4) gain at T_h = –40 °C.
(5) gain at T_h = 20 °C.
(6) gain at T_h = 80 °C.

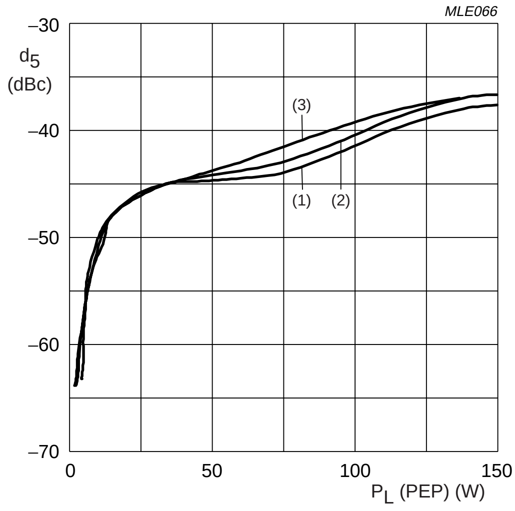
Fig.5 2-tone power gain and efficiency as functions of load power at different temperatures.



V_{DS} = 27 V; I_{DQ} = 1.1 A; f_1 = 920.0 MHz; f_2 = 920.1 MHz.

(1) T_h = –40 °C.
(2) T_h = 20 °C.
(3) T_h = 80 °C.

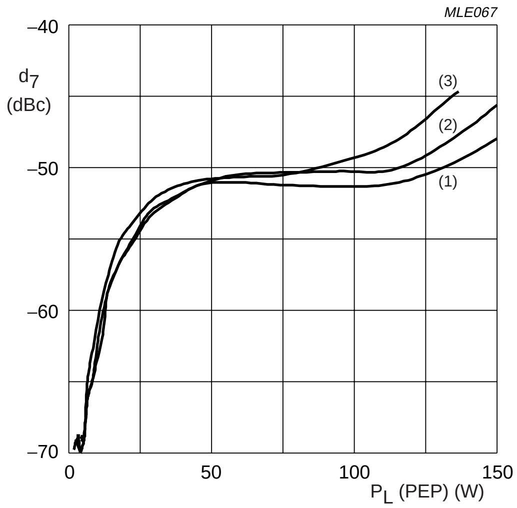
Fig.6 Third order intermodulation distortion as a function of load power at different temperatures.



V_{DS} = 27 V; I_{DQ} = 1.1 A; f_1 = 920.0 MHz; f_2 = 920.1 MHz.

(1) T_h = –40 °C.
(2) T_h = 20 °C.
(3) T_h = 80 °C.

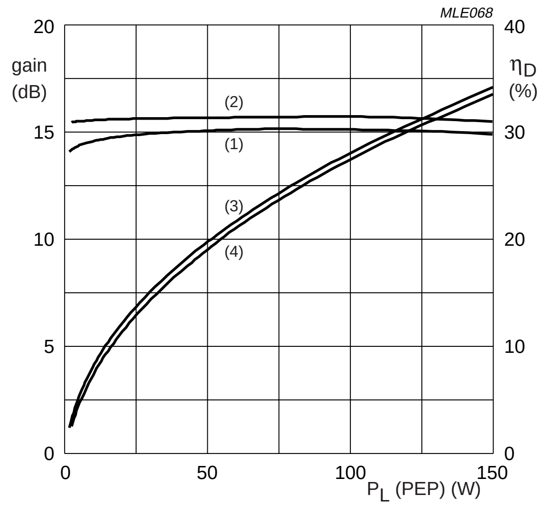
Fig.7 Fifth order intermodulation distortion as a function of load power at different temperatures.



V_{DS} = 27 V; I_{DQ} = 1.1 A; f_1 = 920.0 MHz;

(1) T_h = –40 °C.
(2) T_h = 20 °C.
(3) T_h = 80 °C.

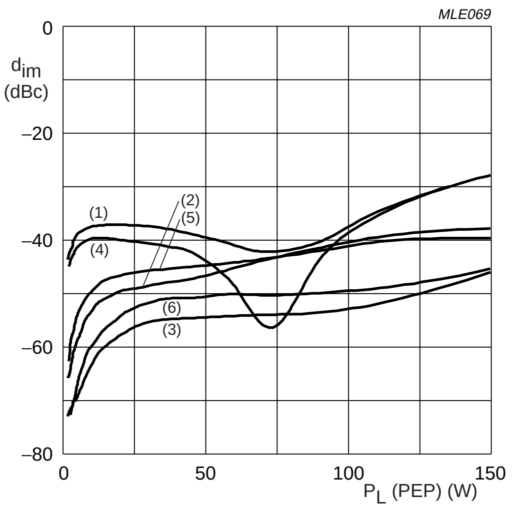
Fig.8 Seventh order intermodulation distortion as a function of load power at different temperatures.



V_{DS} = 27 V; f_1 = 920.0 MHz; f_2 = 920.1 MHz.

(1) I_{DQ} = 1 A.
(2) I_{DQ} = 1.45 A.
(3) I_{DQ} = 1 A.
(4) I_{DQ} = 1.45 A.

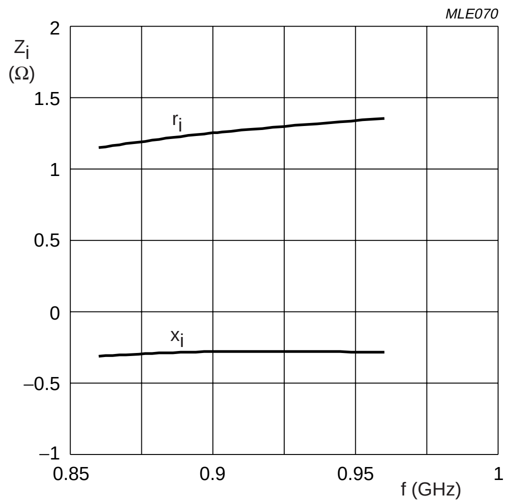
Fig.9 Power gain and drain efficiency as functions of peak envelope load power; typical values.



V_{DS} = 27 V; f_1 = 920.0 MHz; f_2 = 920.1 MHz.

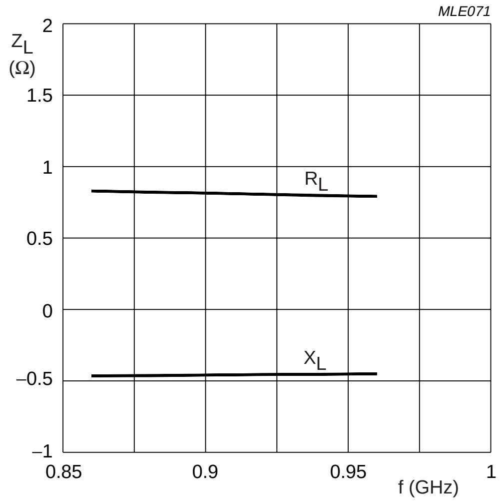
(1) d_3; I_{DQ} = 1 A.
(2) d_5; I_{DQ} = 1 A.
(3) d_7; I_{DQ} = 1 A.
(4) d_3; I_{DQ} = 1.3 A.
(5) d_5; I_{DQ} = 1.3 A.
(6) d_7; I_{DQ} = 1.3 A.

Fig.10 Intermodulation distortion as a function of peak envelope load power; typical values.



Class-AB operation; V_{DS} = 27 V; I_{DQ} = 1125 mA; P_L = 35 W.
Values comprised for different parameters.

Fig.11 Input impedance as a function of frequency (series components); typical values.



Class-AB operation; V_{DS} = 27 V; I_{DQ} = 1125 mA; P_L = 35 W.
Values comprised for different parameters.

Fig.12 Input impedance as a function of frequency (series components); typical values.

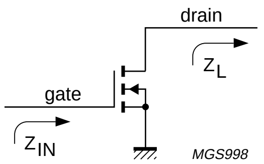


Fig.13 Definition of transistor impedance.

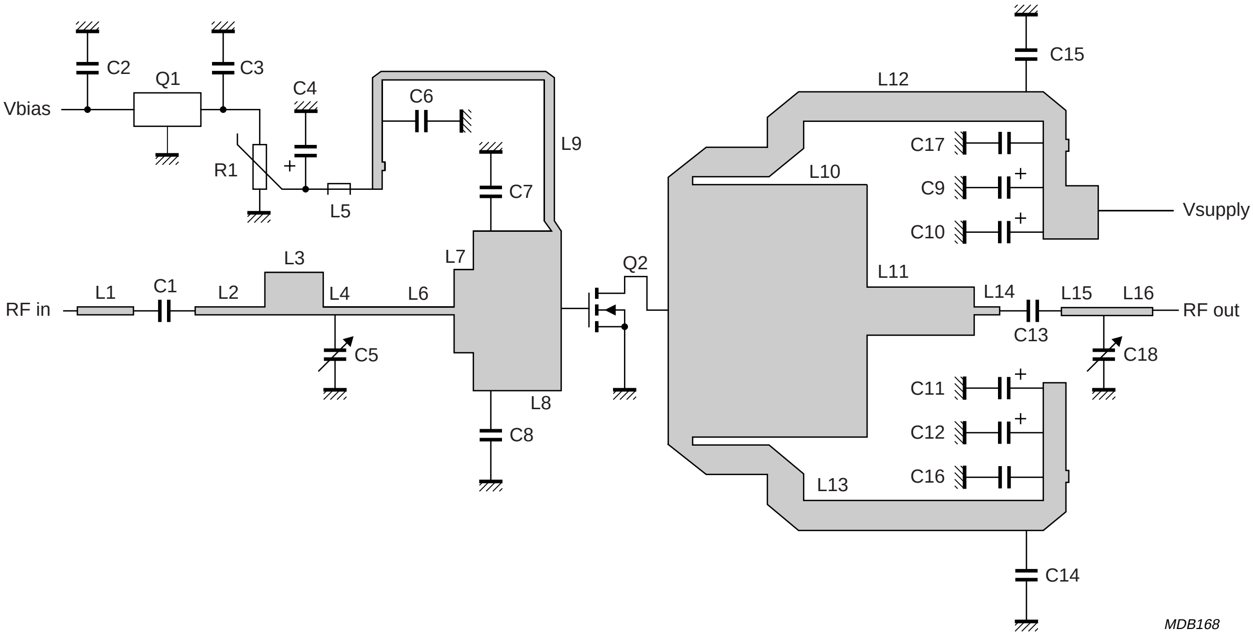
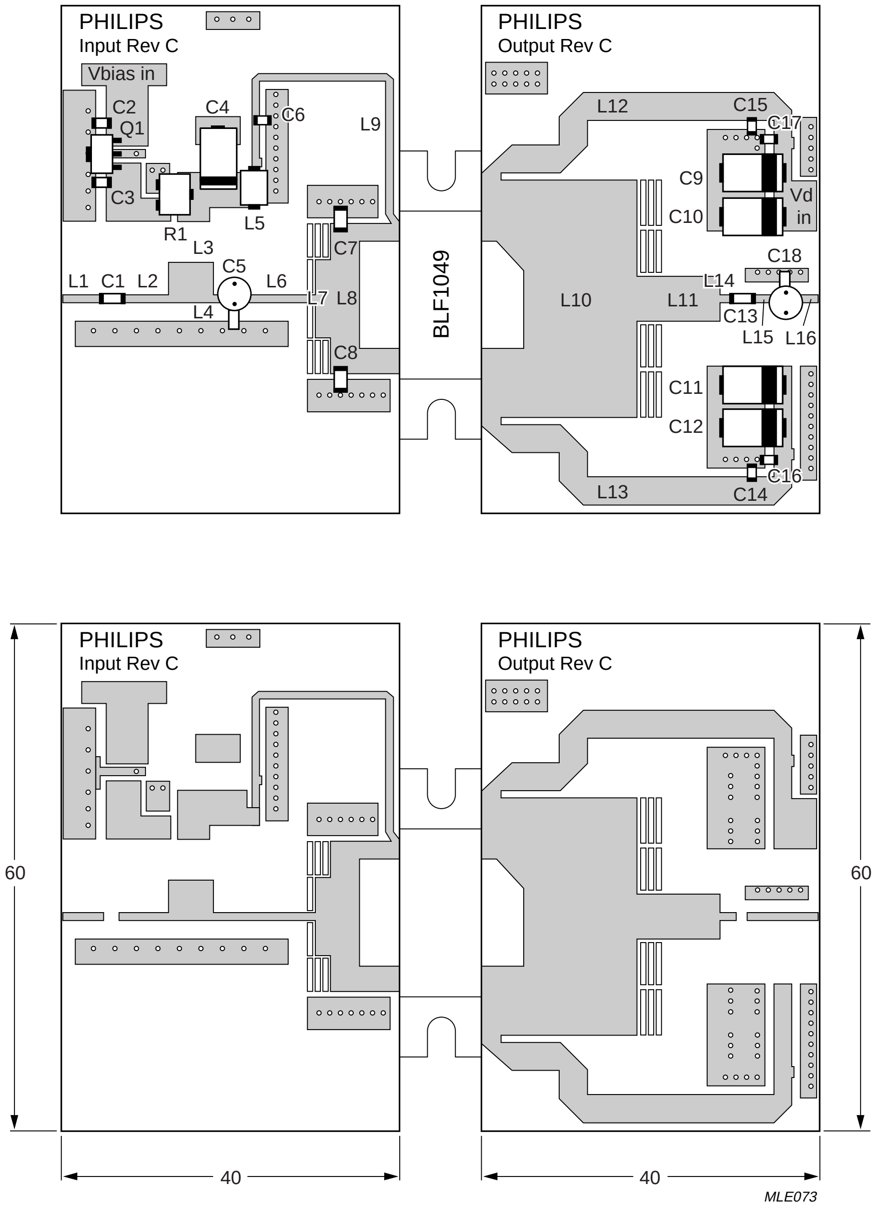


Fig.14 Test circuit for 860 to 900 MHz.



Dimensions in mm.

The components are situated on one side of the copper-clad Rogers 6006 printed-circuit board (ε_r = 6.15); thickness = 25 mm. The other side is unetched and serves as a ground plane.

Fig.15 Component layout for 860 to 900 MHz test circuit.

List of components (see Figs 14 and 15)

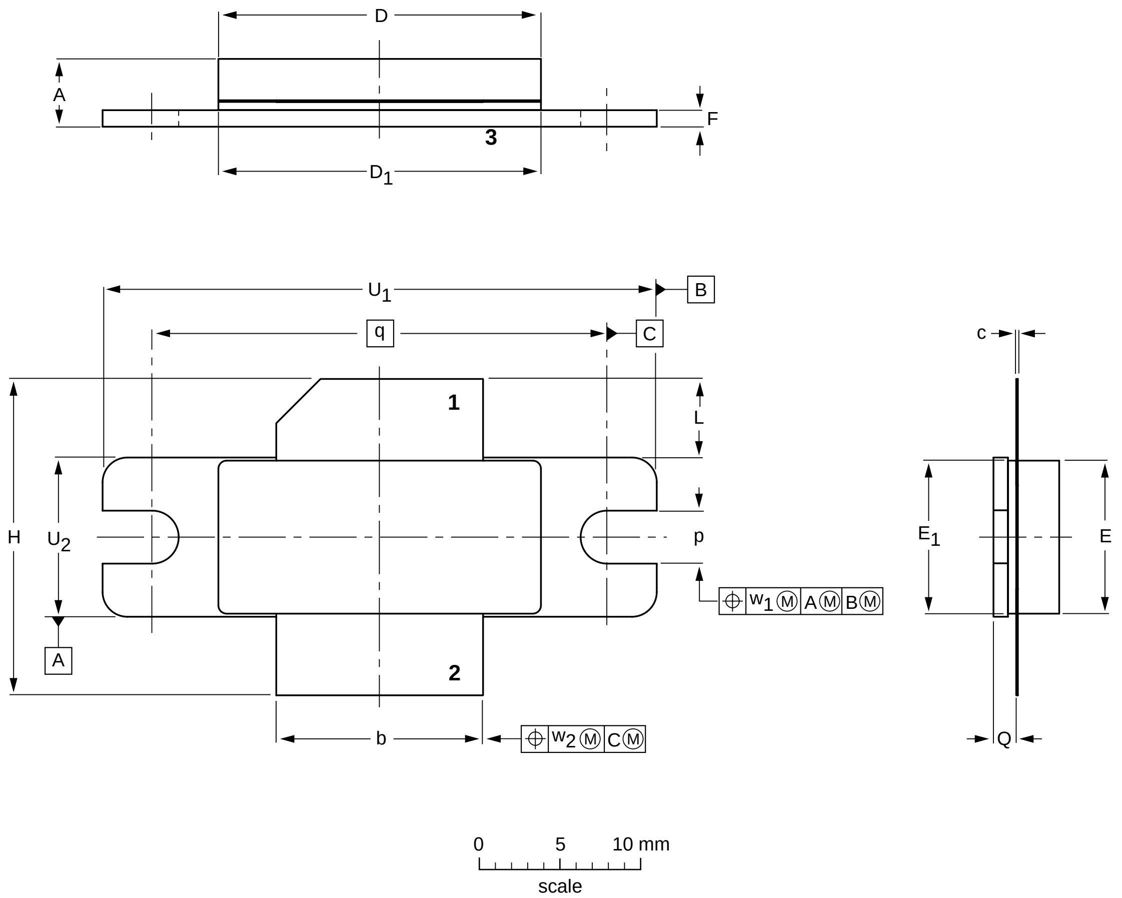
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1, C6, C13, C14, C15, C16, C17	multilayer ceramic chip capacitor; note 1	68 pF	
C2	multilayer ceramic chip capacitor; note 1	330 nF	
C3	multilayer ceramic chip capacitor; note 1	100 nF	
C4, C9, C10, C11, C12	tantalum capacitor	10 μF	
C5, C18	air trimmer capacitor	5 pF	
C7, C8	multilayer ceramic chip capacitor	8.2 pF	
R1	potentiometer	1 kΩ	
Q1	7808 voltage regulator		
Q2	BLF1049 LDMOS transistor		
L1	stripline; note 2		5.22 × 0.92 mm
L2	stripline; note 2		6.47 × 0.92 mm
L3	stripline; note 2		5.38 × 4.8 mm
L4	stripline; note 2		2.4 × 0.92 mm
L5	ferroxcube		
L6	stripline; note 2		9.73 × 0.92 mm
L7	stripline; note 2		1.82 × 9.3 mm
L8	stripline; note 2		8.15 × 17.9 mm
L9	stripline; note 2		44 × 0.92 mm
L10	stripline; note 2		18.45 × 28.3 mm
L11	stripline; note 2		9.95 × 5.38 mm
L12, L13	stripline; note 2		37.6 × 3.35 mm
L14	stripline; note 2		2.36 × 0.92 mm
L15, L16	stripline; note 2		4.22 × 0.92 mm

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad Rogers 6006 printed-circuit board (ε_r = 6.15); thickness = 0.64 mm.

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

Printed in The Netherlands 613524/03/pp12 Date of release: 2003 May 14 Document order number: 9397 750 11123

Let's make things better.

Philips
Semiconductors

PHILIPS