Low Vcesat NPN Epitaxial Planar Transistor

BTD1805J3

Description

The device is manufactured in NPN planar technology by using a “Base Island” layout. The resulting transistor shows exceptional high gain performance coupled with very low saturation voltage.

Features

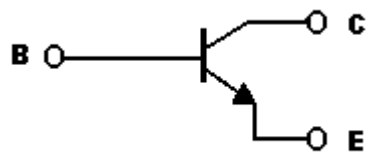
- Very low collector-to-emitter saturation voltage
- Fast switching speed
- High current gain characteristic
- Large current capability

Applications

- CCFL drivers
- Voltage regulators
- Relay drivers
- High efficiency low voltage switching applications

Symbol

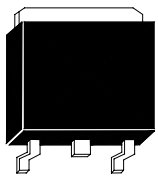
BTD1805J3



B：Base
C：Collector
E：Emitter

Outline

TO-252



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage (I_E=0)	V_{CBO}	150	V
Collector-Emitter Voltage (I_B=0)	V_{CEO}	60	V
Emitter-Base Voltage (I_C=0)	V_{EBO}	7	V
Collector Current (DC)	I_C	5	A
Collector Current (Pulse)	I_{CP}	10 (Note 1)	
Base Current	I_B	2	A
Power Dissipation @ T_A=25℃	P_D	1	W
Power Dissipation @ T_C=25℃	P_D	15	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	-55~+150	°C

Note : 1. Single Pulse , Pw≦380μs,Duty≦2%.

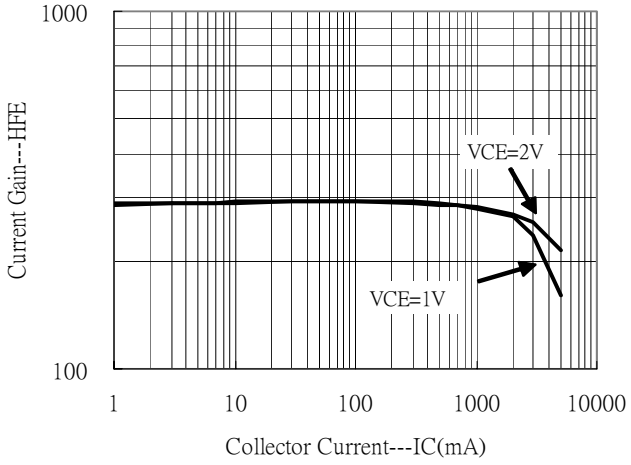
Characteristics (Ta=25°C)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV_{CBO}	150	-	-	V	I_C=100μA, I_E=0
*BV_{CEO}	60	-	-	V	I_C=1mA, I_B=0
BV_{EBO}	7	-	-	V	I_C=100μA, I_C=0
I_{CBO}	-	-	0.1	μA	V_{CB}=80V, I_E=0
I_{EBO}	-	-	0.1	μA	V_{EB}=4V, I_C=0
*$V_{CE(sat)}$ 1	-	-	50	mV	I_C=100mA, I_B=5mA
*$V_{CE(sat)}$ 2	-	200	300	mV	I_C=2A, I_B=50mA
*$V_{CE(sat)}$ 3	-	240	400	mV	I_C=3A, I_B=150mA
*$V_{CE(sat)}$ 4	-	-	600	mV	I_C=5A, I_B=200mA
*$V_{BE(sat)}$	-	0.9	1.2	V	I_C=2A, I_B=100mA
*h_{FE} 1	200	-	400	-	V_{CE}=2V, I_C=100mA
*h_{FE} 2	85	-	-	-	V_{CE}=2V, I_C=5A
*h_{FE} 3	20	-	-	-	V_{CE}=2V, I_C=10A
f_T	-	150	-	MHz	V_{CE}=10V, I_C=50mA
Cob	-	50	-	pF	V_{CB}=10V, f=1MHz
t_{on}	-	50	-	ns	V_{CC}=30V, I_C=10I_{B1}=-10I_{B2}=1A, R_L=30Ω
t_{stg}	-	1.35	-	μs	
t_f	-	120	-	ns	

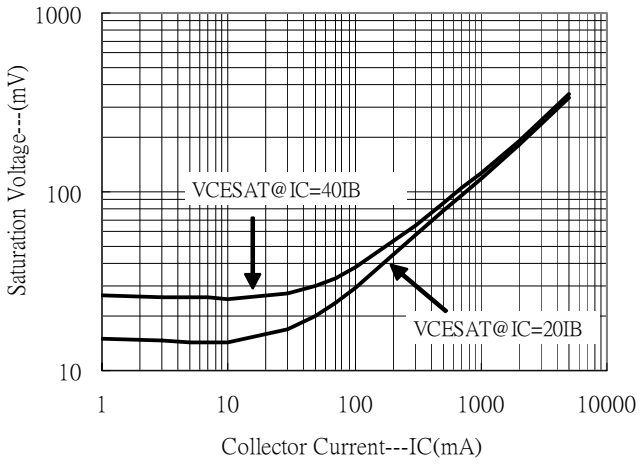
*Pulse Test : Pulse Width ≤380μs, Duty Cycle≤2%

Characteristic Curves

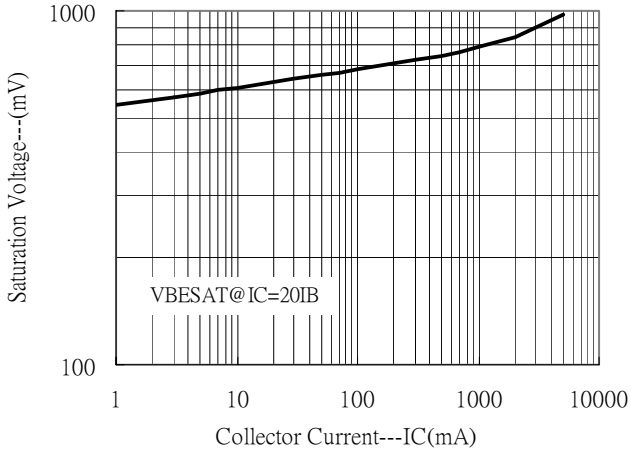
Current Gain vs Collector Current



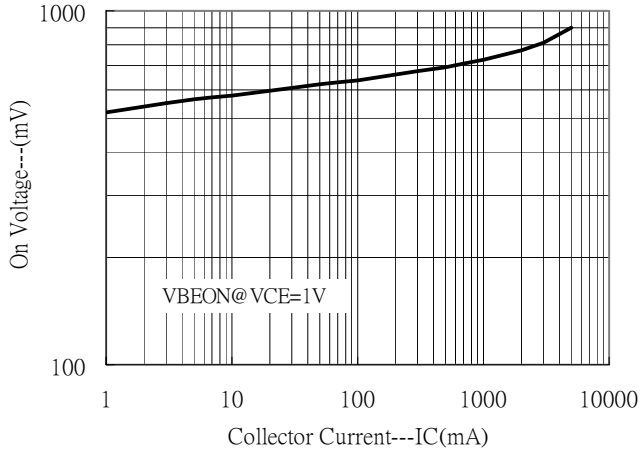
Saturation Voltage vs Collector Current



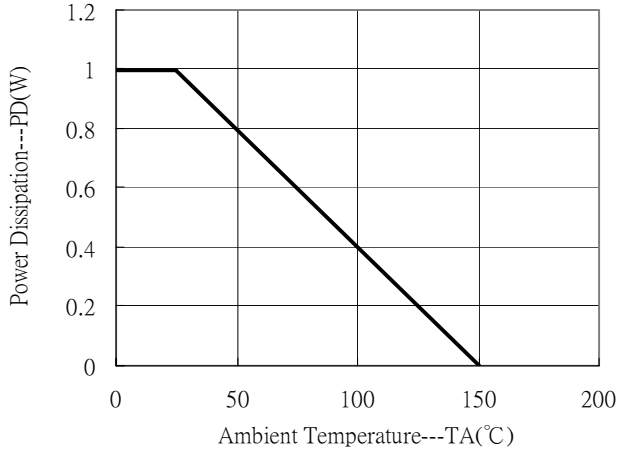
Saturation Voltage vs Collector Current



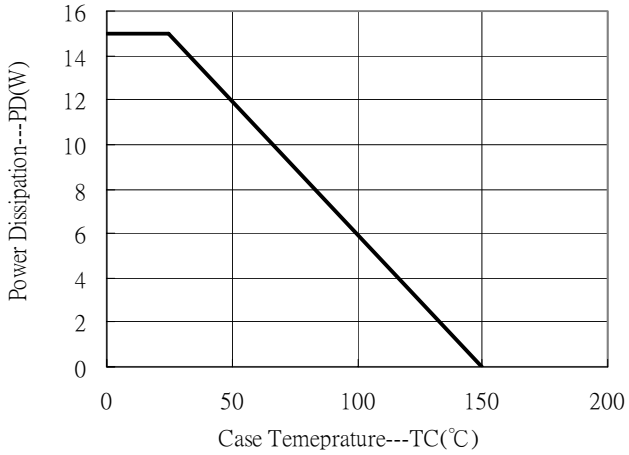
On Voltage vs Collector Current



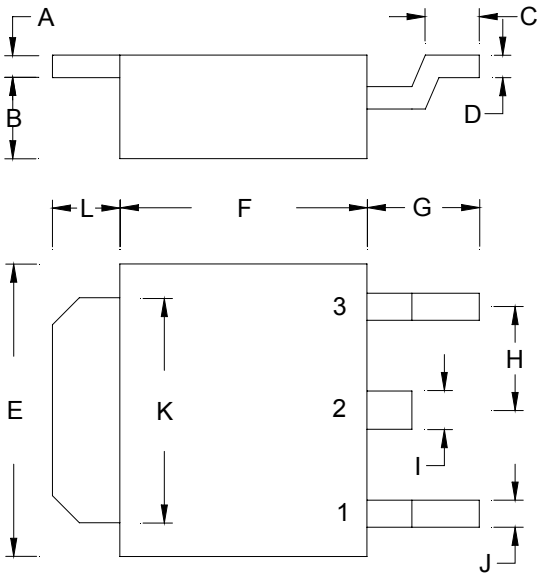
Power Derating Curve



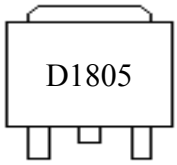
Power Derating Curve



TO-252 Dimension



Marking:



Style: Pin 1.Base 2.Collector 3.Emitter

3-Lead TO-252 Plastic Surface Mount Package
CYStek Package Code: J3

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.0177	0.0217	0.45	0.55	G	0.0866	0.1102	2.20	2.80
B	0.0650	0.0768	1.65	1.95	H	-	*0.0906	-	*2.30
C	0.0354	0.0591	0.90	1.50	I	-	0.0354	-	0.90
D	0.0177	0.0236	0.45	0.60	J	-	0.0315	-	0.80
E	0.2520	0.2677	6.40	6.80	K	0.2047	0.2165	5.20	5.50
F	0.2125	0.2283	5.40	5.80	L	0.0551	0.0630	1.40	1.60

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: 42 Alloy; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0