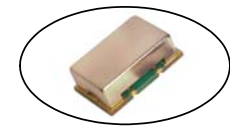


CCHD-950 Model
9X14 mm SMD, 3.3V, CMOS



Ultra-Low Phase Noise
Clock Oscillator



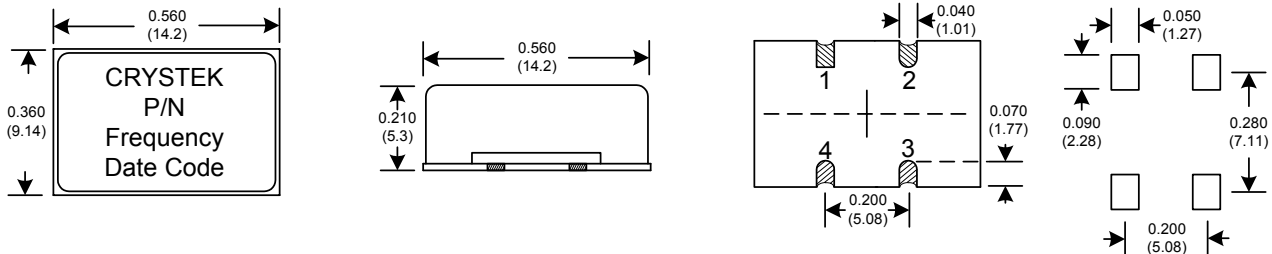
Frequency Range: 50MHz to 125MHz
Frequency Stability: ±20ppm, ±25ppm, ±50ppm
Temperature Range: 0°C to 70°C (±20ppm, ±25ppm, ±50ppm)
 (Option M) -20°C to 70°C (±25ppm, ±50ppm)
 (Option X) -40°C to 85°C (±25ppm, ±50ppm)
Storage: -55°C to 120°C
Input Voltage: 3.3V ±0.3V
Input Current: 15mA Typ, 25mA Max
Output: CMOS
 Symmetry: 45/55% Max @ 50% Vdd
 Rise/Fall Time: 3ns Max @ 20% to 80% Vdd
 Logic: "0" = 10% Vdd Max
 "1" = 90% Vdd Min
 Load: 15pF
 Output current: ±24mA Max
Jitter: 12KHz to 80MHz 0.5psec Typ., 1psec RMS Max
Phase Noise Floor: -160dBc Typ., -155dBc Max Guaranteed
Sub-Harmonics: None
Aging: <3ppm 1st/yr, <1ppm every year thereafter

The CCHD-950 was designed specifically for applications requiring Ultra-Low Phase Noise. Also available in VCXO version. Available on tape and reel in quantities of 100, 250 and 500pcs.

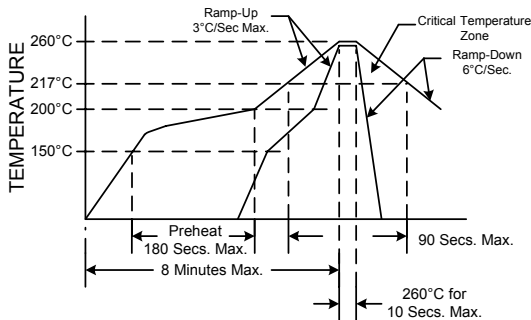
Part Number Example:

CCHD-950-20-100.000 = 3.3V, 45/55, ±20ppm, 0/70°C, 100.000 MHz
CCHD-950M-25-100.000 = 3.3V, 45/55, ±25ppm, -20/70°C, 100.000 MHz
CCHD-950X-50-100.000 = 3.3V, 45/55, ±50ppm, -40/85°C, 100.000 MHz

SUGGESTED PAD LAYOUT

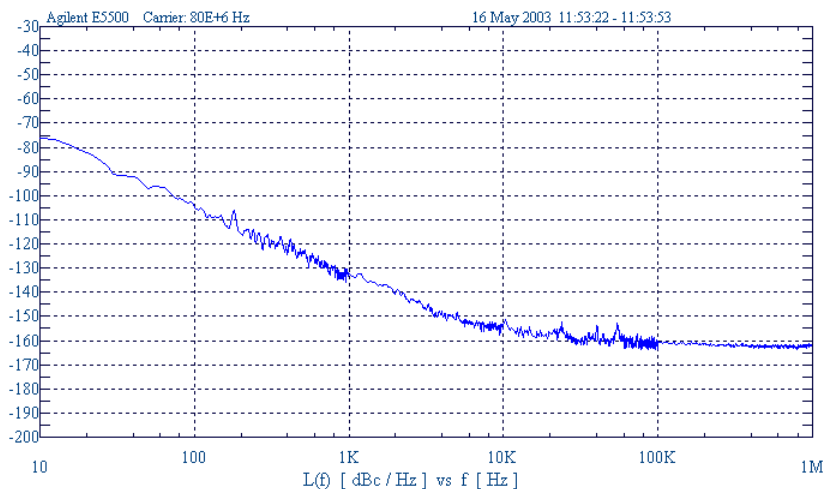


RECOMMENDED REFLOW SOLDERING PROFILE



Pad	Connection
1	N/C
2	GND
3	OUT
4	Vdd

80MHz Phase Noise Plot



Specifications subject to change without notice.

TD-030603 Rev. C



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