

17-24GHz Low Noise, Variable Gain Amplifier

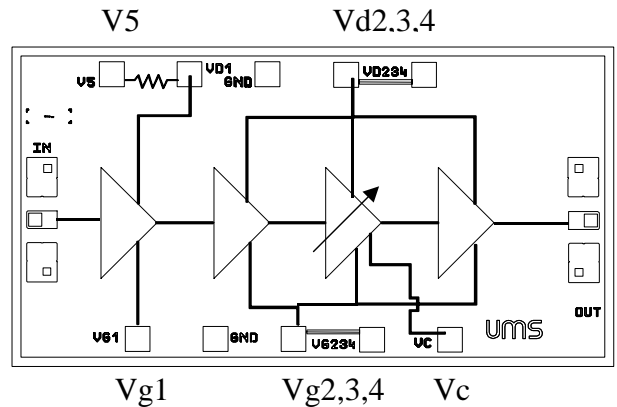
GaAs Monolithic Microwave IC

preliminary

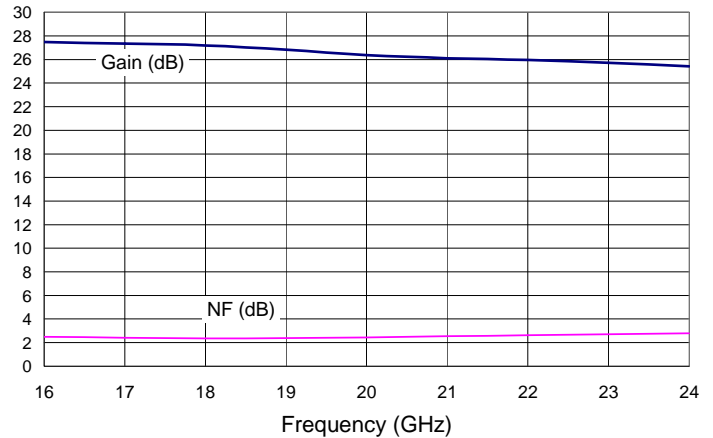
Description

The CHA2292 is a high gain four-stage monolithic low noise amplifier with variable gain. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounded. This helps simplify the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



Typical on wafer measurements : Gain & NF



Main Features

- Frequency range : 17-24GHz
- 2.8dB Noise Figure.
- 25dB gain
- Gain control range: 15dB
- DC power consumption: 160mA @ 5V
- Chip size : 2.32 X 1.23 X 0.10 mm

Main Characteristics

Tamb. = 25°C

	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		24	GHz
G	Small signal gain		25		dB
NF	Noise figure		2.8		dB
Gctrl	Gain control range with Vc variation		15		dB
Id	Bias current		160		mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics for Broadband OperationT_{amb} = +25°C, V₅=V_{d2,3,4}= 5V*preliminary*

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		24	GHz
G	Small signal gain (1)		25		dB
ΔG	Small signal gain flatness (1)		±1		dB
Is	Reverse isolation (1)		50		dB
NF	Noise figure with V _c =1.2V		2.8		dB
Gctrl	Gain control range versus V _c		15		dB
P1dB	Output power at 1dB compression with V _c =1.2V		11		dBm
VSWR _{in}	Input VSWR (1)			3.0:1	
VSWR _{out}	Output VSWR (1)			2.5:1	
V _d	DC voltage V ₅ = V _{d2,3,4} V _c	-1.5	5 [-0.7, +1.2]	+1.3	V V
I _{d1}	Bias current (2) with V _c =1.2V		35		mA
I _d	Bias current total (3) with V _c =1.2V		160		mA

(1) These values are representative of on-wafer measurements that are made without bonding wires at RF ports.

(2) For optimum noise figure, the bias current I_{d1} should be adjusted to 35mA with V_{g1} voltage.

(3) With I_{d1}=35mA, adjust V_{g2,3,4} voltage for a total drain current around 160mA.

Absolute Maximum RatingsT_{amb.} = 25°C (1)

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	5.5	V
V _c	Control bias voltage	1.5	V
I _d	Drain bias current	250	mA
V _g	Gate bias voltage	-2.0 to +0.4	V
P _{in}	Maximum peak input power overdrive (2)	+15	dBm
T _a	Operating temperature range	-40 to +85	°C
T _{stg}	Storage temperature range	-55 to +155	°C

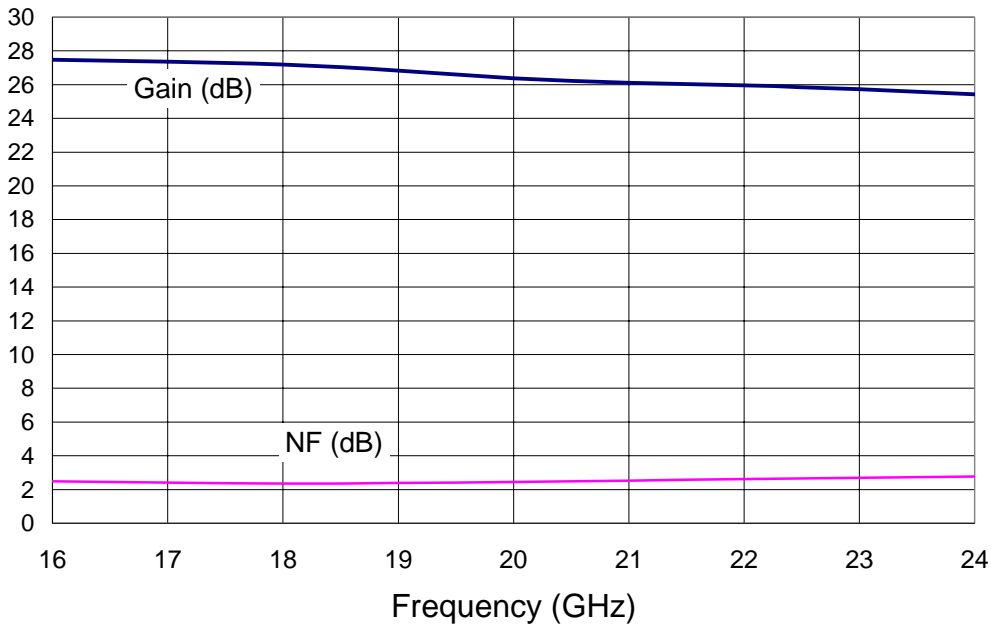
(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

preliminary

Typical on wafer Measurements

Bias Conditions : $V_5=V_{d2,3,4}= 5V$, V_{g1} for $I_{d1}= 35mA$, $V_g = -0.3V$, $V_c=1.2V$

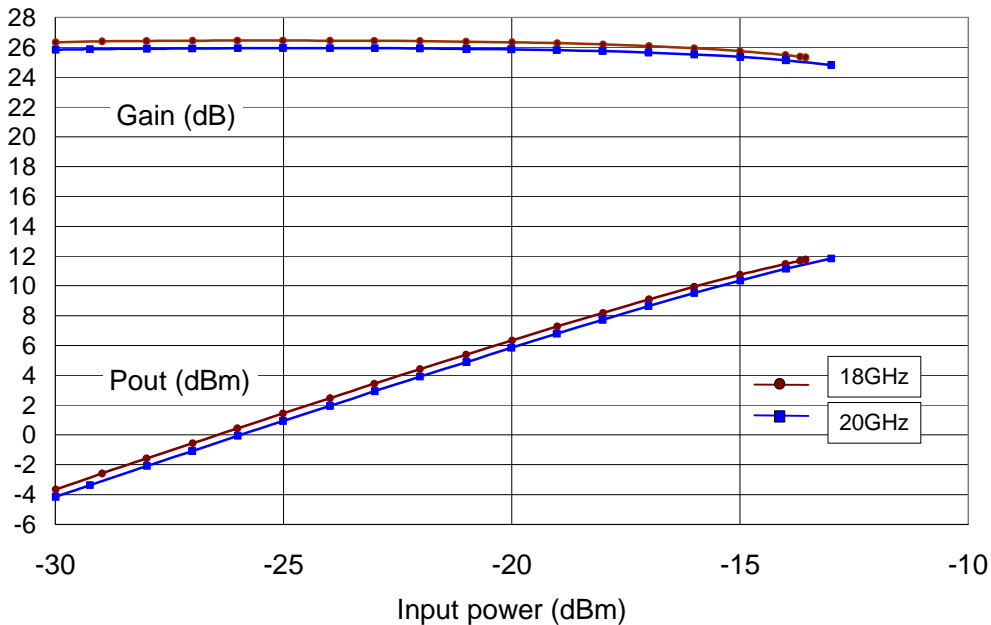


Gain & Noise Figure versus frequency

In jig Measurements

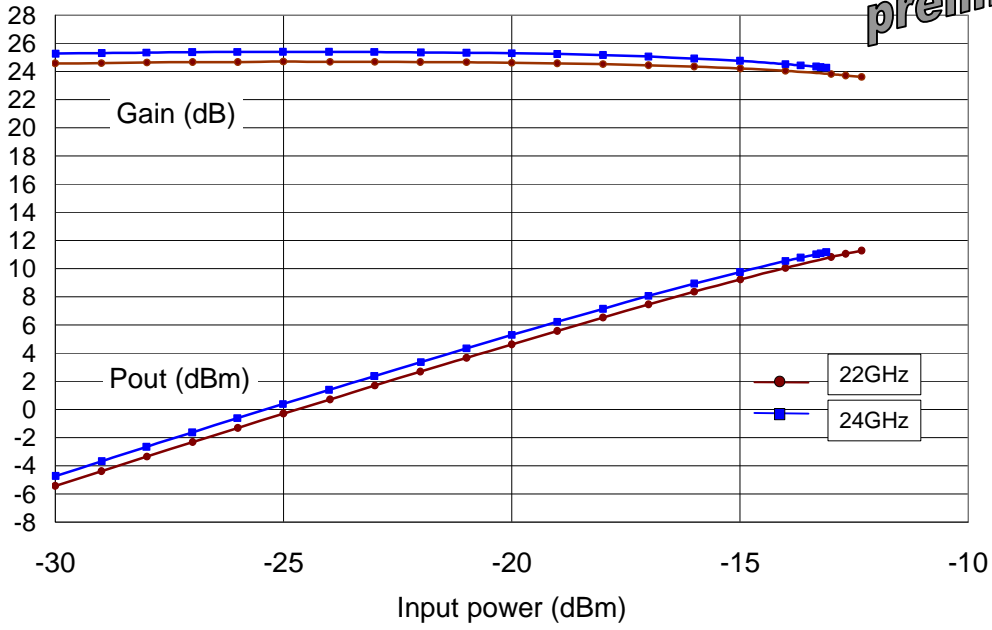
Bias Conditions : $V_5=V_{d2,3,4}= 5V$, $V_{g1}= V_g = -0.3V$, $V_c= 1.2V$

All these measurements include the jig losses (about 0.5dB on gain, 0.2dB on noise figure and 0.3dB on output power).

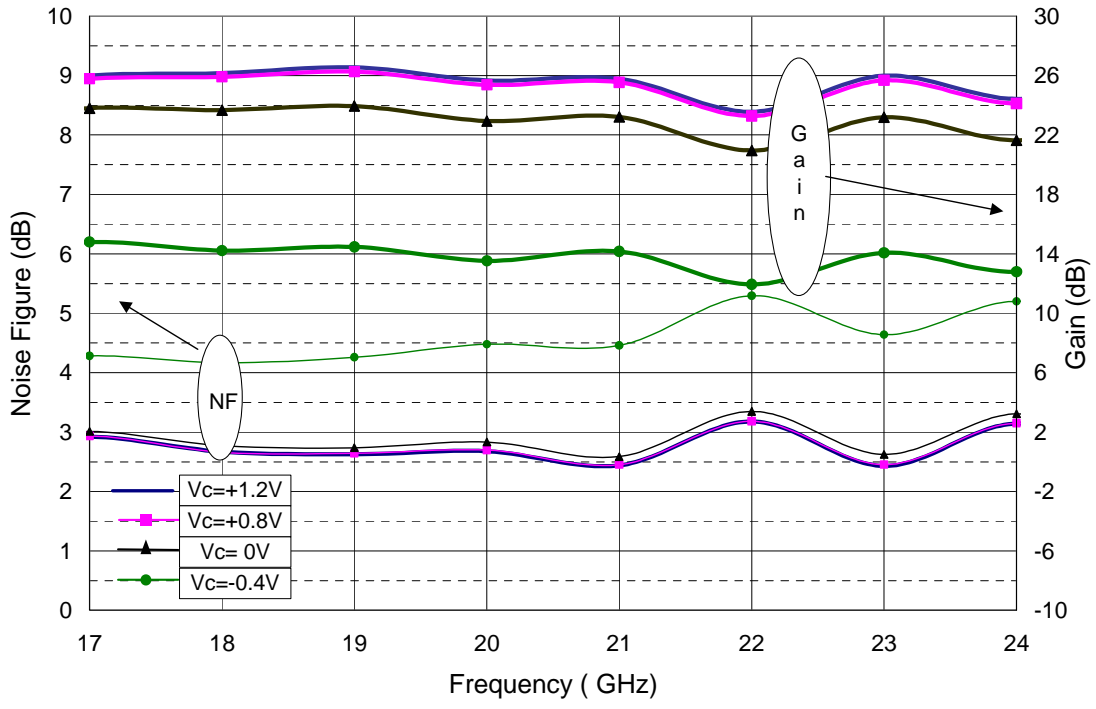


Gain & Output power @ 18-20 GHz

preliminary



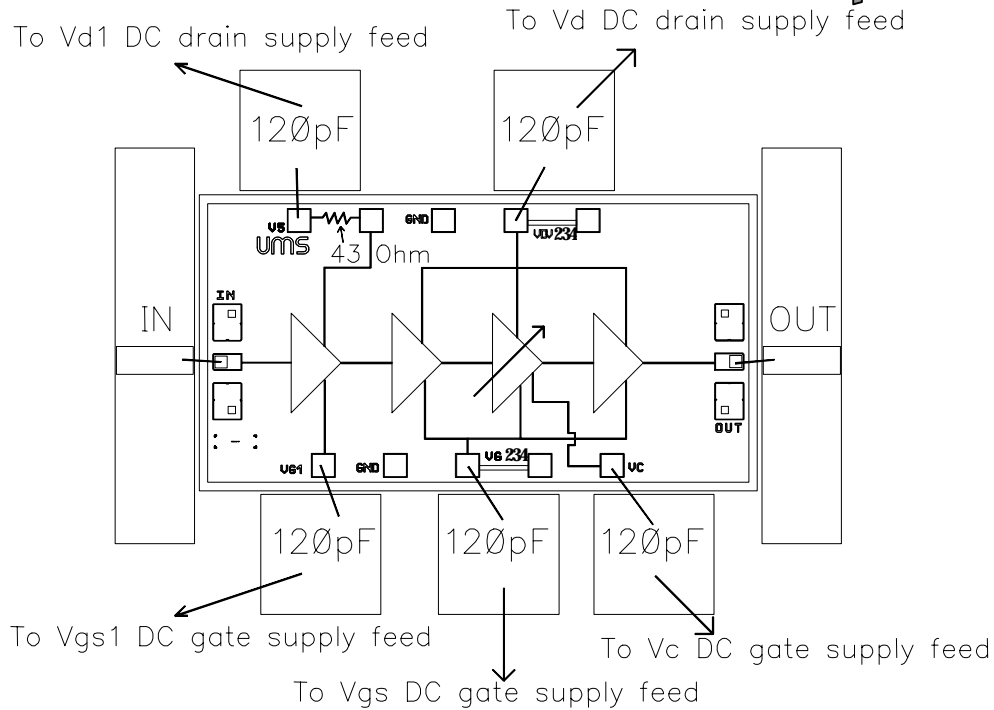
Gain & Output power @ 22-24 GHz



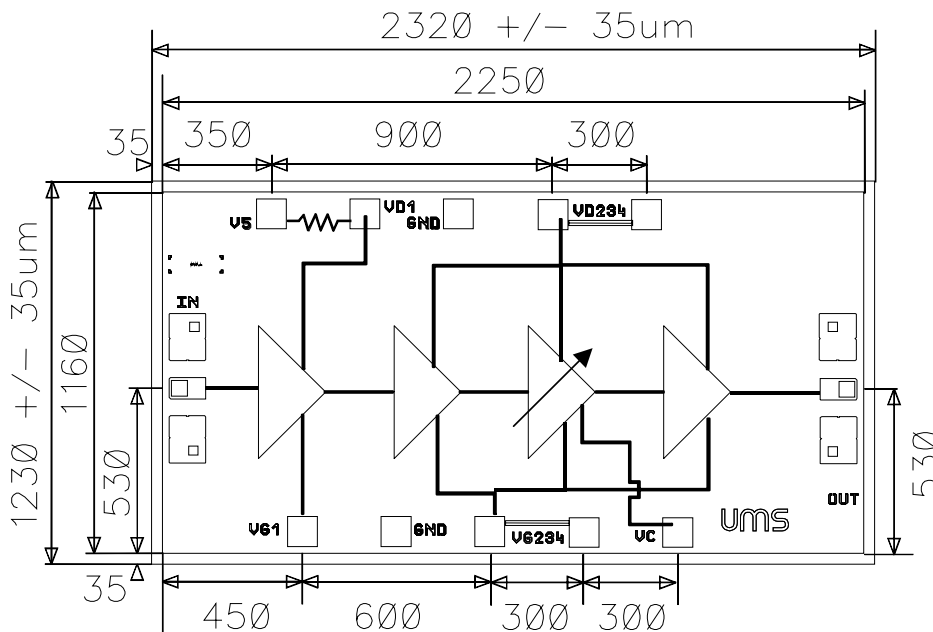
Gain & Noise Figure versus Vc

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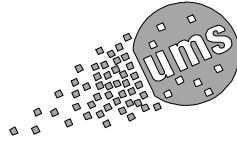
Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended
Bond Pad:100 x 100 µm



Bonding pad positions
(Chip thickness : 100µm. All dimensions are in micrometers)



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Ordering Information

Chip form : CHA2292-99F/00

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