CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX878
Line Powered Modem plus DAA

D/878/2 December 2002

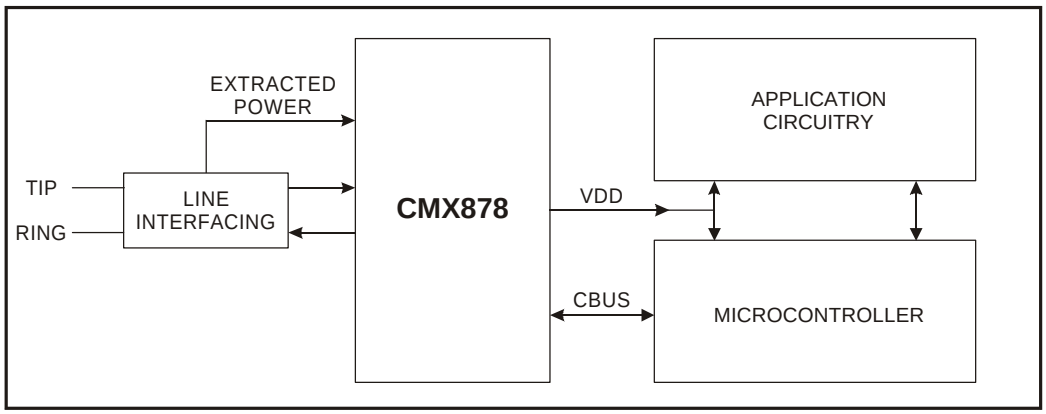
Provisional Issue

Features

- V.22bis, V.22, Bell 212A, V.23/Bell 202, V.21/Bell 103 modulation schemes
- DTMF/Tones Transmit and Receive
- Line Reversal and Ring Detection
- Regulated Power taken from Line
- Gyrator and Impedance Matching Control
- Parallel Phone Detection
- Low Power Operation and Standby

Applications

- Line Powered Applications
- EPOS Terminals
- Remote Utility Meter Reading
- Security Systems
- Telephone Telemetry Systems
- ATMs
- Pay-Phones
- E-mail Terminals



1.1 Brief Description

The CMX878 is a line-powered multi-standard modem for use in telephone based information and telemetry systems. It provides the building blocks for interfacing to the telephone line without the need for a transformer - this is the Data Access Arrangement (DAA) – allowing for the coupling of data signals to and from the line; it can also detect Ringing and Line Reversals.

Provision is made for the conditioning and monitoring of other aspects of the telephone line – this includes the gyrator/loop current, line impedance control, and line voltage measurement. A complete line interface can be implemented using low cost external components.

Very low power consumption and built-in power management makes the CMX878 suitable for telephone line power usage. Furthermore the microcontroller can be de-powered whilst awaiting the detection of a Ring, Line Reversal, or WAKE pin event.

Control of the device is via a simple high speed serial bus, compatible with most types of µC serial interface. Data transmitted and received by the modem is transferred over the same serial bus.

The CMX878 is available in 28-pin SOIC, SSOP and TSSOP packages.

CONTENTS

1.2 Block Diagrams

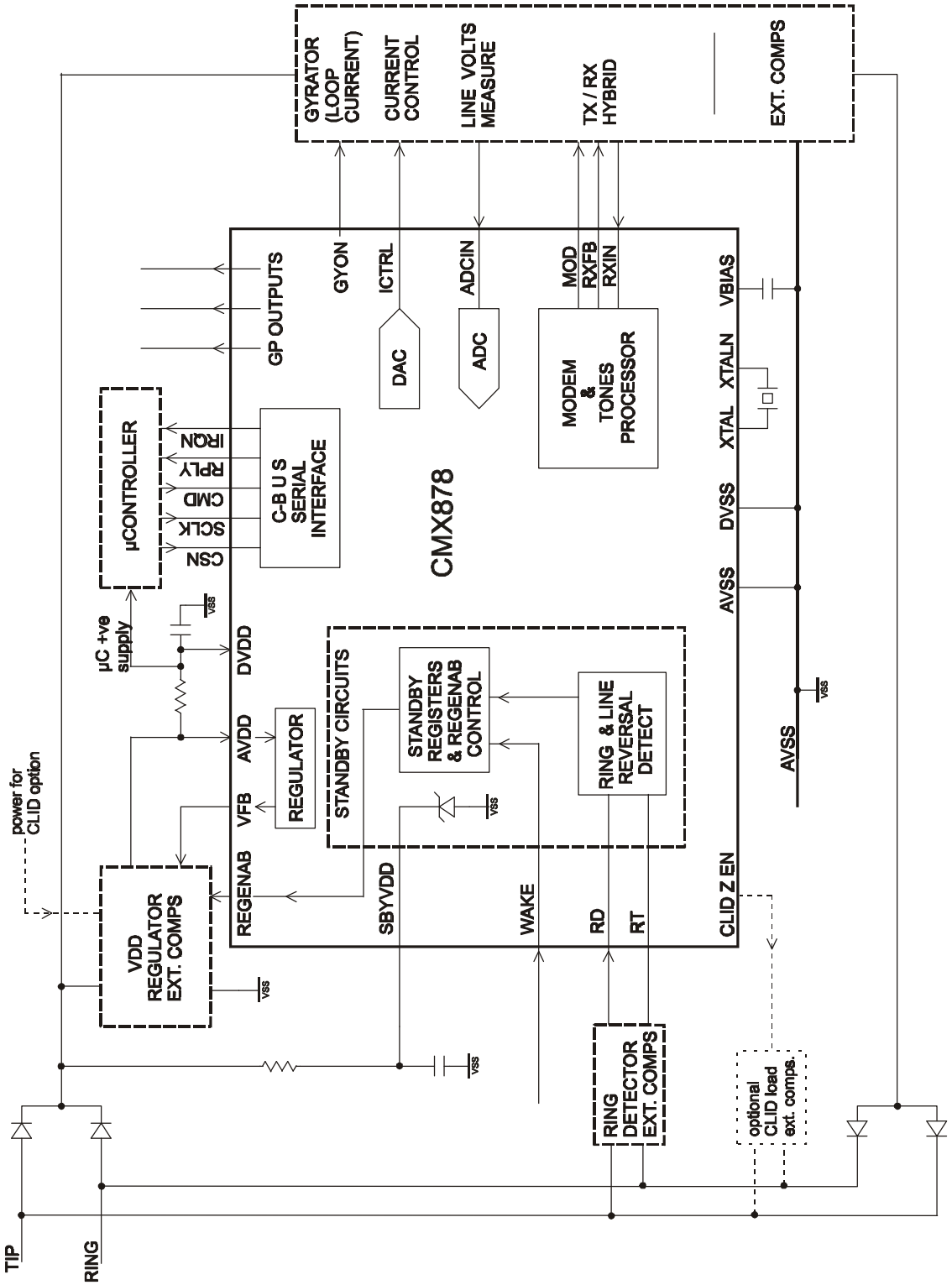


Figure 1a Block Diagram of CMX878 within a typical application
(See Figure 1b for details of MODEM & TONES PROCESSOR block)

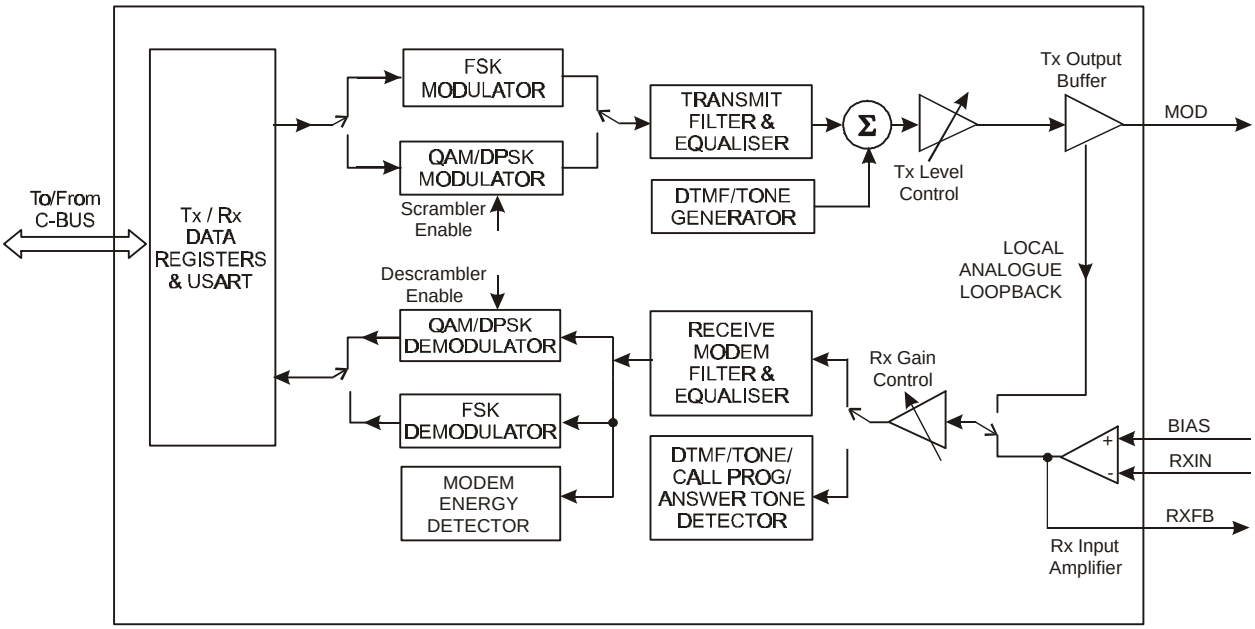


Figure 1b Block Diagram of MODEM & TONES PROCESSOR

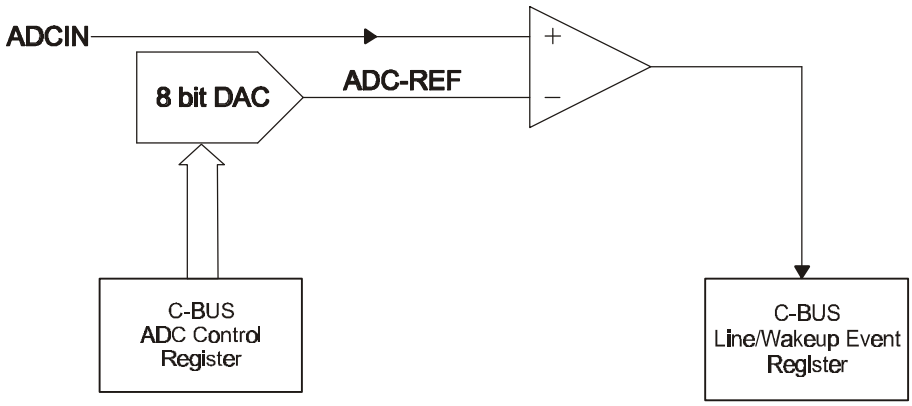


Figure 1c Block Diagram of the ADC circuit

1.3 Signal List

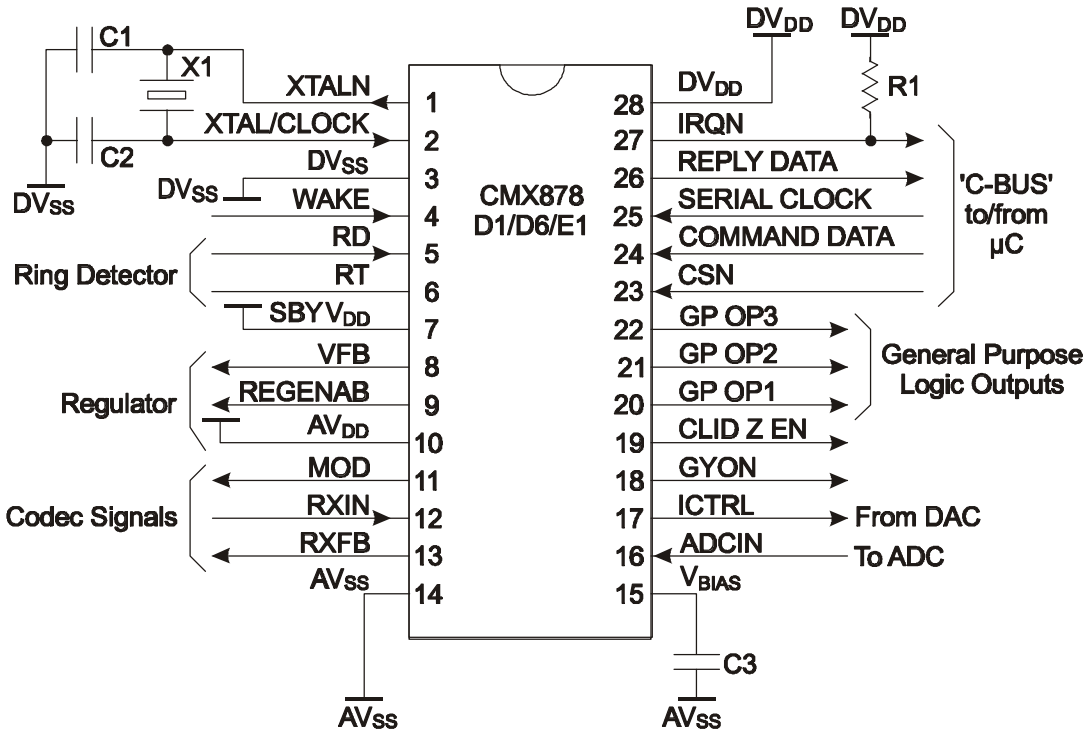
CMX878 D1/D6/E1 packages	Signal		Description
Pin No.	**Name**	**Type**	
1	XTALN	O/P	The output of the on-chip Xtal oscillator inverter.
2	XTAL/CLOCK	I/P	The input to the oscillator inverter from the Xtal circuit or external clock source.
3	DV_{SS}	Power	The negative supply rail for the digital on-chip blocks.
4	WAKE	I/P	A 0 to 1 transition on this pin can be used to wake the device.
5	RD	I/P	Schmitt trigger input to the Ring signal detector. Connect to V_{SS} if Ring Detector not used.
6	RT	BI	Open drain output and Schmitt trigger input forming part of the Ring signal detector. Connect to $SBYV_{DD}$ if Ring Detector not used.
7	$SBYV_{DD}$	Power	The positive rail of the low current Standby Supply. This supply will normally remain present even when the regulated supply has been de-powered.
8	VFB	O/P	Forms part of the regulator feedback loop.
9	REGENAB	O/P	A logic output used to enable the regulator. This pin is powered from the Standby Supply and will take the level of $SBYV_{DD}$ when high.
10	AV_{DD}	Power	The positive rail of the regulated power supply.
11	MOD	O/P	The modulation signals generated by the device are output at this pin.
12	RXIN	I/P	The inverting input to the Rx Input Amplifier.
13	RXFB	O/P	The output of the Rx Input Amplifier.
14	AVss	Power	The negative supply rail for the analogue on-chip blocks.
15	V_{BIAS}	I/P	Internally generated bias voltage of approximately $AV_{DD}/2$. It will discharge to V_{SS} when in powersave mode or when the regulated supply is de-powered.
16	ADCIN	I/P	The input to the Analogue to Digital Converter. Used in line voltage measurement and detection of extensions going off-hook.
17	ICTRL	O/P	The output of the programmable DAC. Used for programming a current drawn from the line.
18	GYON	O/P	A logic output used to enable the gyrator.
19	CLID Z EN	O/P	A logic output. Could be used in circuits with Caller Line ID provision to switch in a line matching impedance.

CMX878 D1/D6/E1 packages	Signal		Description
Pin No.	**Name**	**Type**	
20	GP OP1	O/P	A General Purpose logic output. An example use would be as an enable for a second regulator in circuits with a battery.
21	GP OP2	O/P	A General Purpose logic output. An example use would be as a line voltage measurement divider enable in circuits where this function is required separately from the regulator.
22	GP OP3	O/P	A General Purpose logic output. An example use would be as a control to inhibit the ring signal in systems where the application is in series with a phone.
23	CSN	I/P	The C-BUS chip select input from the µC.
24	CMD DATA	I/P	The C-BUS serial data input from the µC.
25	SERIAL CLOCK	I/P	The C-BUS serial clock input from the µC.
26	REPLY DATA	T/S	A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
27	IRQN	O/P	A 'wire-ORable' output for connection to a µC Interrupt Request input. This output is pulled down to V_{SS} when active and is high impedance when inactive. An external pullup resistor is required ie R1 of Figure 2
28	DV_{DD}	Power	The positive supply rail for the digital on-chip blocks.

Notes:

I/P = Input
O/P = Output
BI = Bidirectional
T/S = 3-state Output
NC = No Connection

1.4 External Components



R1	100kΩ	C1, C2	22pF
X1	11.0592MHz or 12.288MHz	C3	100nF

Resistors ±5%, capacitors ±20% unless otherwise stated.

Figure 2a Pin-out of Packaged Device

Power Supply Arrangement

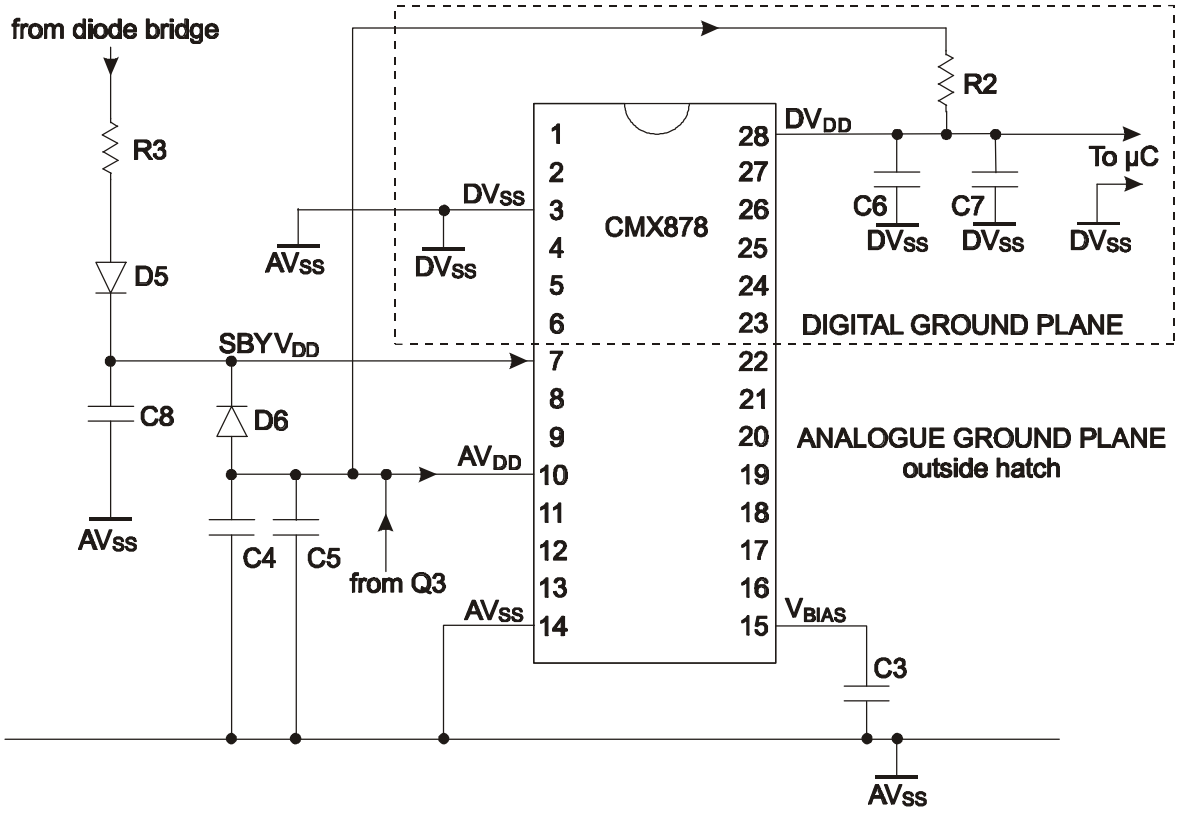


Figure 2b Recommended Power Supply Connections and De-coupling

This device is capable of detecting and decoding small amplitude signals. To achieve this DV_{DD}, AV_{DD} and V_{BIAS} should be decoupled and the receive path protected from extraneous in-band signals. It is recommended that the printed circuit board is laid out with both AV_{SS} and DV_{SS} ground planes in the CMX878 area, as shown in Figure 2b, with provision to make a link between them close to the CMX878. To provide a low impedance connection to ground, the decoupling capacitors must be mounted as close to the CMX878 as possible and connected directly to their respective ground plane. This will be achieved more easily by using surface mounted capacitors.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity. Apart from the decoupling capacitor, no other loads are allowed. If V_{BIAS} needs to be used to set external analogue levels, it must be buffered with a high input impedance buffer.

The DV_{SS} connections to the Xtal oscillator capacitors C1 and C2 should also be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up of the oscillator.

In a line powered application it is important to prevent noise from the circuit being coupled onto the line; careful board layout should be employed to minimise this. It is also important to minimise power supply noise currents from causing undesirable modulation of the line; the circuit configuration shown in Figure 4a will minimise this effect.

1.4.1 Ring Detector Interface

This interface runs from the Standby Supply.

Figure 3 shows how the CMX878 may be used to detect the large amplitude Ringing signal voltage or a Line Reversal present at the start of an incoming telephone call.

The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through either C19 and R26 or C20 and R27 to appear at the top end of R28 (point X in Figure 3) in a rectified and attenuated form.

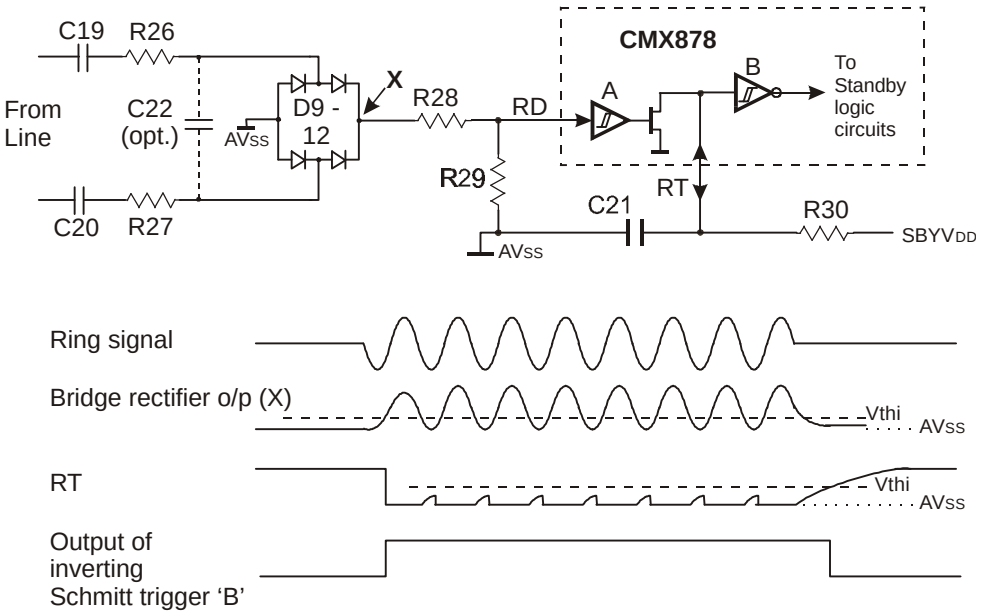
The signal at point X is further attenuated by the potential divider formed by R28 and R29 before being applied to the CMX878 RD input. If the amplitude of the signal appearing at RD is greater than the input threshold (Vthi) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to V_{SS} by discharging the external capacitor C21. The output of the Schmitt trigger 'B' will then go high; this output is then processed by logic circuits running from the Standby Supply.

The minimum amplitude ringing signal that is certain to be detected is:

$$(0.7 + Vthi \times [R26 + R28 + R29] / R29) \times 0.707 \quad Vrms$$

where Vthi is the high-going threshold voltage of the Schmitt trigger A (see section 1.7.1).

With R26-28 all 470kΩ as Figure 3, then setting R29 to 68kΩ will ensure detection of ringing signals of 30Vrms and above for $SBYV_{DD}$ over the range 2.9V to 3.9V.



R26, 27, 28	470kΩ	C19, 20	0.1µF
R29	See text	C21	150nF
R30	1MΩ	D9-12	1N4004

Resistors ±5%, capacitors ±20%

Figure 3 Ring Signal Detector Interface Circuit

If the time constant of R30 and C21 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger for the duration of a ring cycle.

The time for the voltage on RT to charge from V_{SS} towards $SBYV_{DD}$ can be derived from the formula

$$V_{RT} = SBYV_{DD} \times [1 - \exp(-t/(R30 \times C21))]$$

As the Schmitt trigger high-going input threshold voltage (Vthi) has a minimum value of 0.56 x $SBYV_{DD}$, then the Schmitt trigger B output will remain high for a time of at least 0.821 x R30 x C21 following a pulse at RD.

The values of R30 and C21 given in Figure 3 (1MΩ and 150nF) give a minimum RT charge time of 100 msec, which is adequate for ring frequencies of 10Hz or above.

The circuit will also respond to a telephone line voltage reversal. The BT specification SIN242 gives a range of reversal voltages and slew times which must be detected. The slowest change required to be detected is a +15V to –15V reversal between the two lines slewing in 30ms. In order to ensure detection of this reversal the resistor R29 should be set to 300kΩ.

There are systems where the 'ring' signal is made up from consecutive fast line reversals – an example is an ISDN terminal adapter which connects to local POTS ports. In such a case the CMX878 ring detector circuit will give a better response with the inclusion of capacitor C22 (10nF).

If the Ring detect function is not used then pin RD should be connected to V_{SS} and RT to $SBYV_{DD}$.

1.4.2 Line-derived Power and Line Interfacing

The CMX878 has the building blocks for providing a variety of line interfacing solutions. Figure 4a shows a suitable set of external components for interfacing to the line (explained in Figure 4b) . Note that some of the component values vary according to whether the application is for American or European markets.

1.4.2.1 Standby Regulator

The Ring Detect and Wake input circuitry and the Standby C-BUS registers are permanently powered by the voltage on the $SBYV_{DD}$ pin. This voltage is generated from the telephone line voltage by the Standby Regulator, which consists of the high value resistor R3 and an on-chip zener diode (nominally 3.3V) connected between the $SBYV_{DD}$ and V_{SS} pins. D5 and C8 ensure that $SBYV_{DD}$ remains at a workable value during short line breaks. D6 provides an alternative source of $SBYV_{DD}$ when the main Regulated Supply is present.

1.4.2.2 The Regulated Supply and Line Volts Measurement

When the REGENAB pin is high M1 and Q1 connect the +ve line voltage to the line voltage measurement divider R6, R7 and, via R8 and R9, to the AV_{DD} regulator circuit Q2, Q3. An on-chip comparator and bandgap reference control the base drive to Q2 via the VFB pin to keep the Regulated Supply AV_{DD} at nominally 3.3V.

The digital parts of the CMX878 are powered from the DV_{DD} pin. This supply is derived from the regulated supply AV_{DD} through a decoupling network R2, C6, C7.

The Regulated Supply powers all parts of the CMX878 (except the Standby Circuits) and also the host microcontroller. It is recommended that the total load on this supply should not exceed 10mA.

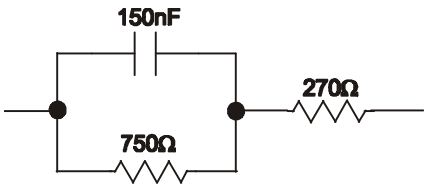
The Standby Supply will out-live the Regulated Supply following a loss of line voltage.

1.4.2.3 Loop Current Control, AC Impedance and Modulation

When the CMX878 is in Standby mode, the GYON and ICTRL output pins will be at Vss, hence Q4, Q5 and M2 will be turned off and will draw no current from the telephone line.

In the off-hook mode, the regulated supply will be turned on, the GYON output will be at V_{DD} and the ICTRL output will be high impedance, hence M2 will be turned on, providing drive to the quasi-darlington Q4/Q5. The DC loop current taken from the line is then controlled by the network R16, D8, R19, R20, R14 and R15. Transistor Q6, together with the voltage divider R17, R18 and decoupling capacitor C11, act as an optional DC current limiter which limits to approx. 60mA with the recommended components (as required in TBR21). With selection of the appropriate external component values the resulting DC line voltage vs. current characteristic can be made to meet the requirements of TBR21 or EIA-470-A.

The AC impedance presented to the line in the off-hook mode is controlled by the network C10, R15, R14. With selection of the component values for the appropriate market it will either give a good match to the TBR21 (European) nominal impedance as shown below…



…or 600Ω for American systems.

The analogue signal output of the CMX878 modem appears at the MOD pin and modulates the line voltage via C13, R22, R21, Q5 and Q4. C14 attenuates any high frequency noise that may be present at the MOD output pin.

When the regulated supply is enabled, the CMX878 may also be set into a 'line probing' mode, in which it draws a programmable current from the telephone line. This can be useful in characterising the line. In this mode the GYON output is at V_{SS} and the line current is determined by the output of the DAC appearing at the ICTRL output pin. Note that in this mode the AC impedance presented to the line and the transmit signal levels will not be correct.

1.4.2.4 Rx Hybrid

The AC signal input to the CMX878 is taken from the line through C16 and R25 to the input amplifier pin RXIN, the level of the receive signal appearing at the RXFB pin being determined by the ratio of the resistors R25 and R24. C15 and R23 provide a receive hybrid function to reduce the level of transmitted signal appearing at the RXFB pin (the CMX878 requires a minimum of 7dB rejection, however with careful component selection it will be possible to greatly exceed this).

1.4.2.5 Transmit Levels and Receive Thresholds

Transmit levels and receive thresholds are proportional to AV_{DD}. 0dBm = 775mVrms.

With the circuit in Figure 4a (which regulates AV_{DD} to 3.3V), the Tx Mode Register set for a Tx Level Control gain of 0dB and a matched line, the nominal transmit line levels will be:

QAM, DPSK and FSK Tx modes (no guard tone)	-10dBm
Single tone transmit mode	-10dBm
DTMF transmit mode	-6 and -8 dBm

With the Rx Mode Register set for a Rx Level Control gain of 0dB, the nominal receiver thresholds will be as stated in the Operating Characteristics.

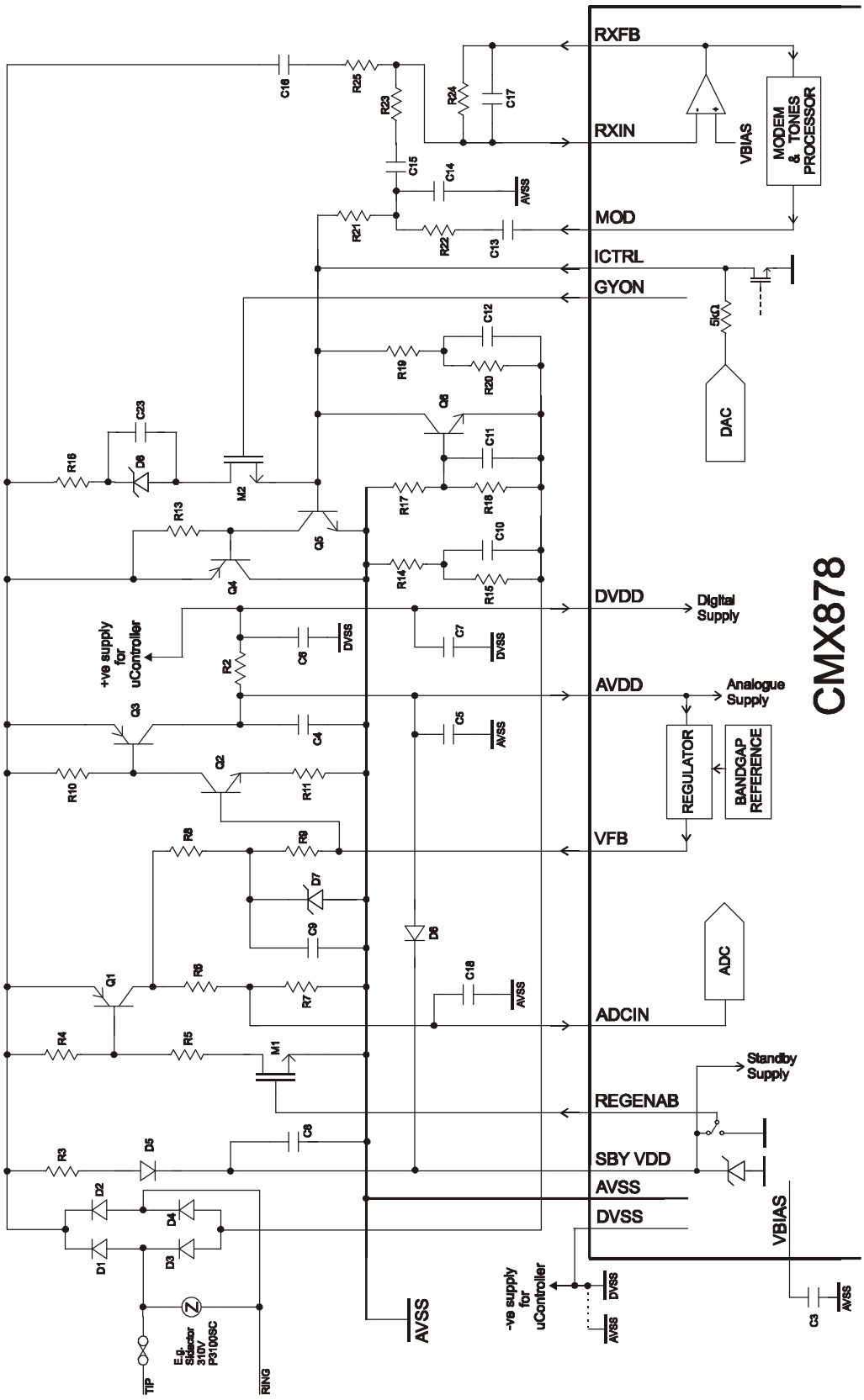


Figure 4a Line interfacing components (ring detection components shown separately)

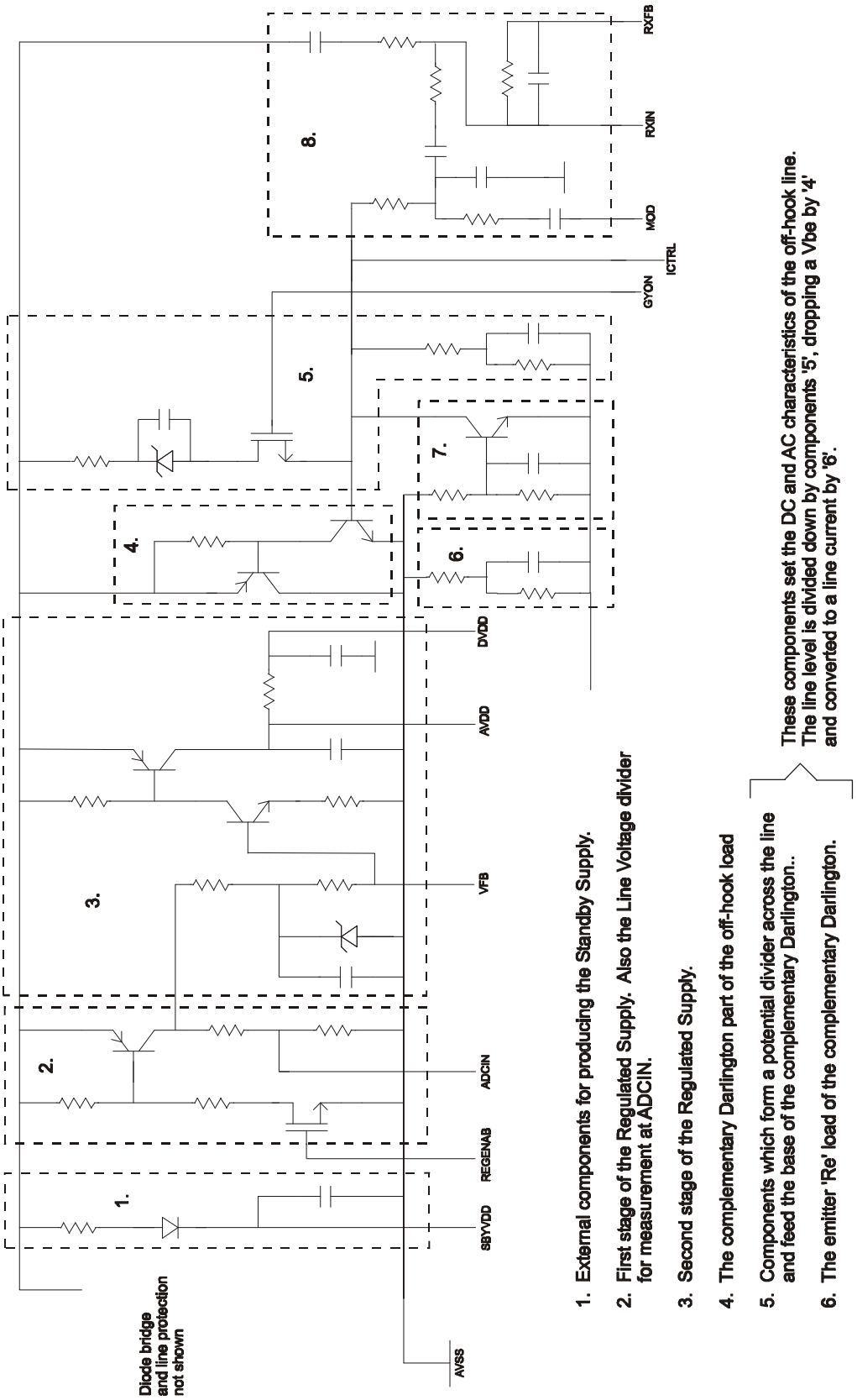


Figure 4b Explanatory view of line interfacing circuit shown in Figure 4a

Component Values – for Figures 2a, 2b and 4a

Resistors ±5%, capacitors ±20%

R1	100kΩ
R2	30Ω
R3	6.8MΩ
R4	100kΩ
R5	220kΩ
R6	470kΩ
R7	15kΩ
R8	100kΩ
R9	100kΩ
R10	100kΩ
R11	2.7kΩ
R13	10kΩ
R14	EURO: 12Ω (0.25W) US: 27Ω (0.5W)
R15	EURO: 36Ω (0.6W) US: wire link
R16	10kΩ
R17	EURO: 5.6kΩ US: not required
R18	EURO: 2kΩ US: not required
R19	470Ω
R20	10kΩ
R21	EURO: 3.3kΩ US: 3kΩ
R22	EURO: 2.7kΩ US: 3kΩ
R23	EURO: 100kΩ US: 91kΩ
R24	100kΩ
R25	160kΩ

C1, C2	22pF
C3	100nF
C4	22µF
C5	100nF
C6	22µF
C7	100nF
C8	100nF
C9	100nF
C10	EURO: 3.3µF US: not required
C11	EURO: 33µF US: not required
C12	3.3µF
C13	220nF
C14	10nF
C15	100nF
C16	47nF
C17	100pF
C18	3.3µF
C23	220nF
D1 - D4	D1N4004
D5	1N914
D6	1N914
D7	BZX84C5V6
D8	BZX84C4V7

Q1	MMBTA92
Q2	MMBTA42
Q3	MMBTA92
Q4*	FZT757
Q5	MMBTA42
Q6	EURO: BC846 US: not required

M1, M2	BSN304 or ZVNL535A

X1	11.0592MHz or 12.288MHz

*Transistor Q4 is the main off-hook load and will dissipate heat. In circuits with the built-in current limiting, the power dissipation can be up to 2 Watts; without current limiting the power dissipation can be up to
1 Watt. Ensure adequate heat sink provision.

'EURO' represents component values for European markets (specification TBR21).
'US' represents component values for North American markets (specification EIA-470)

1.5 General Description

The CMX878 transmit and receive operating modes are independently programmable.

The transmit mode can be set to any one of the following:

V.22bis modem. 2400bps QAM (Quadrature Amplitude Modulation).

V.22 and Bell 212A modem. 1200 or 600 bps DPSK (Differential Phase Shift Keying).

V.21 modem. 300bps FSK (Frequency Shift Keying).

Bell 103 modem. 300bps FSK.

V.23 modem. 1200 or 75 bps FSK.

Bell 202 modem. 1200 or 150 bps FSK.

DTMF transmit.

Single tone transmit (from a range of modem calling, answer and other tone frequencies)

User programmed tone or tone pair transmit (programmable frequencies and levels)

Disabled.

The receive mode can be set to any one of the following:

V.22bis modem. 2400bps QAM.

V.22 and Bell 212A modem. 1200 or 600 bps DPSK.

V.21 modem. 300bps FSK.

Bell 103 modem. 300 bps FSK.

V.23 modem. 1200 or 75 bps FSK.

Bell 202 modem. 1200 or 150 bps FSK.

DTMF detect.

2100Hz and 2225Hz answer tone detect.

Call progress signal detect.

User programmed tone or tone pair detect.

Disabled.

The CMX878 may also be set into a Powersave mode which disables all circuitry except for the C-BUS interface and the Ring Detector.

1.5.1 Tx USART

A flexible Tx USART is provided for all modem modes, meeting the requirements of V.14 for QAM and DPSK modems.

It can be programmed to transmit continuous patterns, Start-Stop characters or Synchronous Data.

In both Synchronous Data and Start-Stop modes the data to be transmitted is written by the µC into the 8-bit C-BUS Tx Data Register from which it is transferred to the Tx Data Buffer.

If Synchronous Data mode has been selected the 8 data bits in the Tx Data Buffer are transmitted serially, b0 being sent first.

In Start-Stop mode a single Start bit is transmitted, followed by 5, 6, 7 or 8 data bits from the Tx Data Buffer - b0 first - followed by an optional Parity bit then - normally - one or two Stop bits. The Start, Parity and Stop bits are generated by the USART as determined by the Tx Mode Register settings and are not taken from the Tx Data Register.

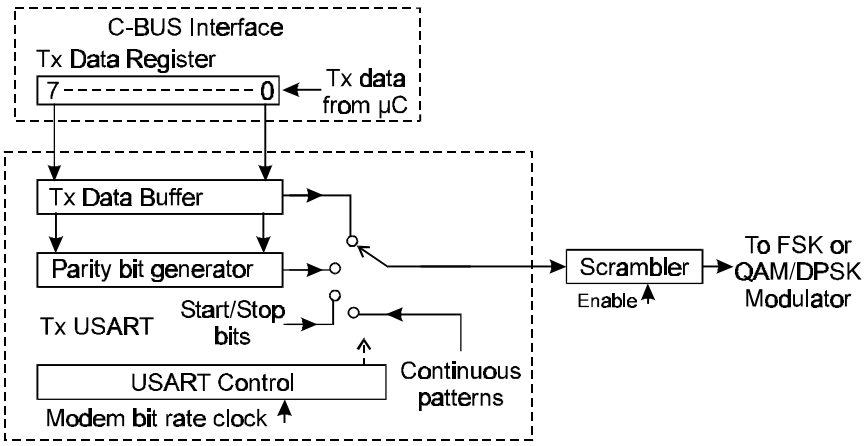


Figure 5a Tx USART

Every time the contents of the C-BUS Tx Data Register are transferred to the Tx Data Buffer the Tx Data Ready flag bit of the Status Register is set to 1 to indicate that a new value should be loaded into the C-BUS Tx Data Register. This flag bit is cleared to 0 when a new value is loaded into the Tx Data Register.

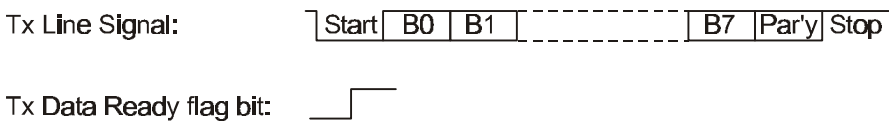


Figure 5b Tx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If a new value is not loaded into the Tx Data Register in time for the next Tx Data Register to Tx Data Buffer transfer then the Status Register Tx Data Underflow bit will be set to 1. In this event the contents of the Tx Data Buffer will be re-transmitted if Synchronous Data mode has been selected, or if the Tx modem is in Start-Stop mode then a continuous Stop signal (1) will be transmitted until a new value is loaded into the Tx Data Register.

In all modes the transmitted bit and baud rates are the nominal rates for the selected modem type, with an accuracy determined by the XTAL frequency accuracy, however for QAM and DPSK modes V.14 requires that Start-Stop characters can be transmitted at up to 1% overspeed (basic signalling rate range) or 2.3% overspeed (extended signalling rate range) by deleting a Stop bit from no more than one out of every 8 (basic range) or 4 (extended range) consecutive transmitted characters.

To accommodate the V.14 requirement the Tx Data Register has been given two C-BUS addresses, $E3 and $E4. Data should normally be written to $E3.

In QAM or DPSK Start-Stop modes if data is written to $E4 then the programmed number of Stop bits will be reduced by one for that character. In this way the µC can delete transmitted Stop bits as needed.

In FSK Start-Stop modes, data written to $E4 will be transmitted with a 12.5% reduction in the length of the Stop bit at the end of that character.

In all Synchronous Data modes data written to $E4 will be treated as though it had been written to $E3.

The underspeed transmission requirement of V.14 is automatically met by the CMX878 as in Start-Stop mode it automatically inserts extra Stop bit(s) if it has to wait for new data to be loaded into the C-BUS Tx Data Register.

The optional V.22/V.22bis compatible data scrambler can be programmed to invert the next input bit in the event of 64 consecutive ones appearing at its input. It uses the generating polynomial:

$$1 + x^{-14} + x^{-17}$$

1.5.2 FSK and QAM/DPSK Modulators

Serial data from the USART is fed via the optional scrambler to the FSK modulator if V.21, V.23, Bell 103 or Bell 202 mode has been selected or to the QAM/DPSK modulator for V.22, V.22bis and Bell 212A modes.

The FSK modulator generates one of two frequencies according to the transmit mode and the value of current transmit data bit.

The QAM/DPSK modulator generates a carrier of 1200Hz (Low Band, Calling modem) or 2400Hz (High Band, Answering modem) which is modulated at 600 symbols/sec as described below:

600bps V.22 signals are transmitted as a +90° carrier phase change for a '0' bit, +270° for '1'.

For V.22 and Bell 212A 1200bps DPSK the transmit data stream is divided into groups of two consecutive bits (dibits) which are encoded as a carrier phase change:

Dibit (left-hand bit is the first of the pair)	**Phase change**
00	+90°
01	0°
11	+270°
10	+180°

For V.22bis 2400bps QAM the transmit data stream is divided into groups of 4 consecutive data bits. The first two bits of each group are encoded as a phase quadrant change and the last two bits define one of four elements within a quadrant:

First two bits of group (left-hand bit is the first of the pair)	Phase quadrant change
00	+90° (e.g. quadrant 1 to 2)
01	0° (no change of quadrant)
11	+270° (e.g. quadrant 1 to 4)
10	+180° (e.g. quadrant 1 to 3)

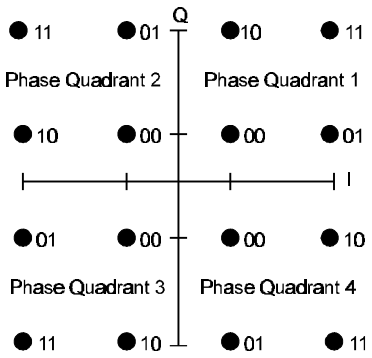


Figure 6 V.22bis Signal Constellation

1.5.3 Tx Filter and Equaliser

The FSK or QAM/DPSK modulator output signal is fed through the Transmit Filter and Equaliser block which limits the out-of-band signal energy to acceptable limits. In 600, 1200 and 2400 bps FSK, DPSK and QAM modes this block includes a fixed compromise line equaliser which is automatically set for the particular modulation type and frequency band being employed. This fixed compromise line equaliser may be enabled or disabled by bit 10 of the General Control Register. The amount of Tx equalisation provided compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1 over the frequency band used.

1.5.4 DTMF/Tone Generator

In DTMF/Tones mode this block generates DTMF signals or single or dual frequency tones. In QAM/DPSK modem modes it is used to generate the optional 550 or 1800Hz guard tone.

1.5.5 Tx Level Control and Output Buffer

The outputs (if present) of the Transmit Filter and DTMF/Tone Generator are summed then passed through the programmable Tx Level Control and Tx Output Buffer to the pins MOD pin.

1.5.6 Rx DTMF/Tones Detectors

In Rx Tones Detect mode the received signal, after passing through the Rx Gain Control block, is fed to the DTMF / Tones / Call Progress / Answer Tone detector. The user may select any of four separate detectors:

The DTMF detector detects standard DTMF signals. A valid DTMF signal will set bit 5 of the Status Register to 1 for as long as the signal is detected.

The programmable tone pair detector includes two separate tone detectors (see Figure 12). The first detector will set bit 6 of the Status Register for as long as a valid signal is detected, the second detector sets bit 7, and bit 10 of the Status Register will be set when both tones are detected.

The Call Progress detector measures the amplitude of the signal at the output of a 275 - 665 Hz bandpass filter and sets bit 10 of the Status Register to 1 when the signal level exceeds the measurement threshold.

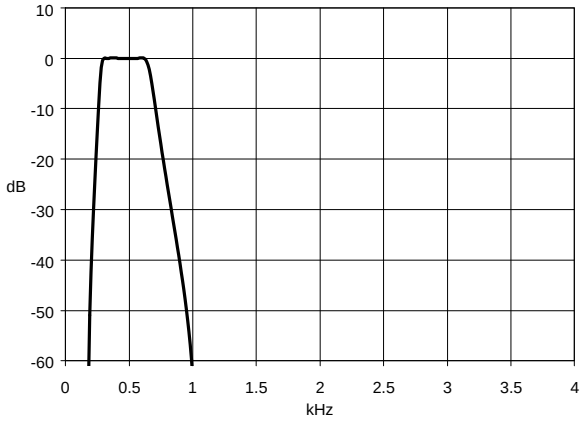


Figure 7a Response of Call Progress Filter

The Answer Tone detector measures both amplitude and frequency of the received signal and sets bit 6 or bit 7 of the Status Register when a valid 2225Hz or 2100Hz signal is received.

1.5.7 Rx Modem Filterering and Demodulation

When the receive part of the CMX878 is operating as a modem, the received signal is fed to a bandpass filter to attenuate unwanted signals and to provide fixed compromise line equalisation for 600, 1200 and 2400 bps FSK, DPSK and QAM modes. The characteristics of the bandpass filter and equaliser are determined by the chosen receive modem type and frequency band. The line equaliser may be enabled or disabled by bit 10 of the General Control Register and compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1.

The responses of these filters, including the line equaliser and the effect of external components used in Figures 4a are shown in Figures 7b-e:

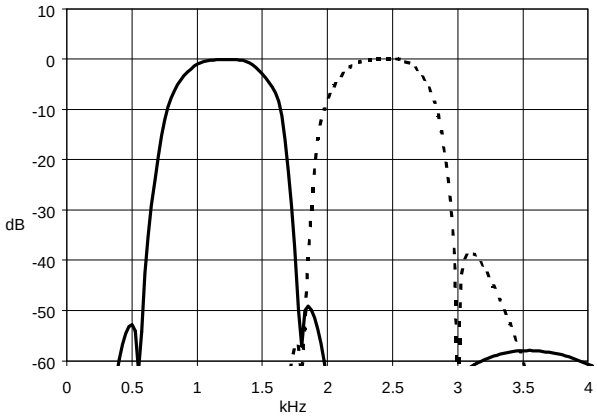


Figure 7b QAM/DPSK Rx Filters

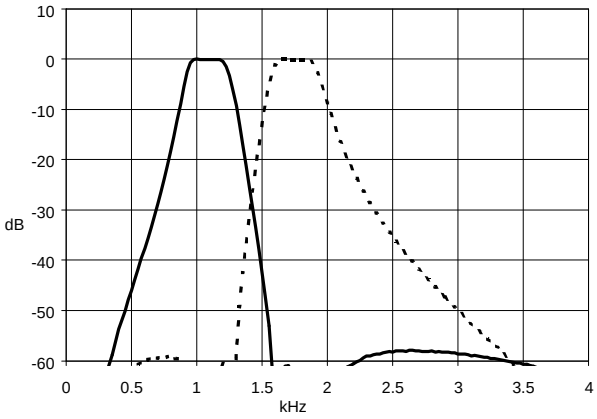


Figure 7c V.21 Rx Filters

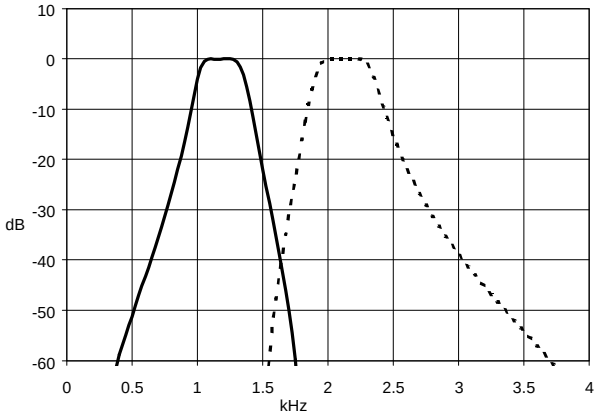


Figure 7d Bell 103 Rx Filters

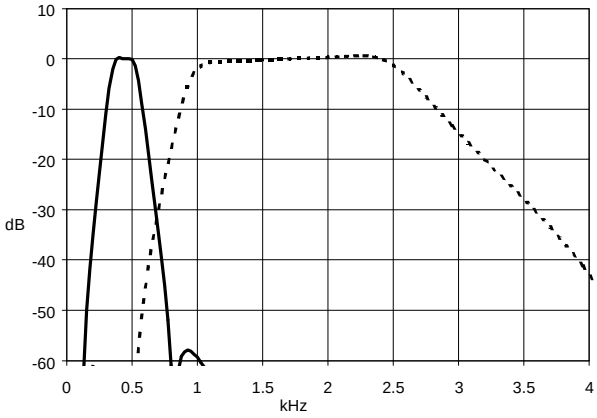


Figure 7e V.23/Bell 202 Rx Filters

The signal level at the output of the Receive Modem Filter and Equaliser is measured in the Modem Energy Detector block, compared to a threshold value, and the result controls bit 10 of the Status Register.

The output of the Receive Modem Filter and Equaliser is also fed to the FSK or QAM/DPSK demodulator depending on the selected modem type.

The FSK demodulator recognises individual frequencies as representing received '1' or '0' data bits:

The QAM/DPSK demodulator decodes QAM or DPSK modulation of a 1200Hz or 2400Hz carrier and is used for V.22, V.22bis and Bell 212A modes. It includes an adaptive receive signal equaliser (auto-equaliser) that will automatically compensate for a wide range of line conditions in both QAM and DPSK modes. It must be enabled when receiving 2400bps QAM. The auto-equaliser can provide a useful improvement in performance in 600 or 1200bps DPSK modes as well as 2400bps QAM, so although it must be disabled at the start of a handshake sequence, it can be enabled as soon as scrambled 1200bps 1s have been detected.

Both FSK and QAM/DPSK demodulators produce a serial data bit stream which is fed to the Rx pattern detector, descrambler and USART block, See Figure 8a. In QAM/DPSK modes the demodulator input is also monitored for the V.22bis handshake 'S1' signal.

The QAM/DPSK demodulator also estimates the received bit error rate by comparing the actual received signal against an ideal waveform. This estimate is placed in bits 2-0 of the Status Register, see Figure 11.

1.5.8 Rx Modem Pattern Detectors and Descrambler

See Figure 8a.

The 1010.. pattern detector operates only in FSK modes and will set bit 9 of the Status Register when 32 bits of alternating 1s and 0s have been received.

The 'Continuous Unscrambled 1s' detector operates in all modem modes and sets bits 8 and 7 of the Status Register to '01' when 32 consecutive 1s have been received.

The descrambler operates only in DPSK/QAM modes and is enabled by setting bit 7 of the Rx Mode Register.

The 'Continuous Scrambled 1's' detector operates only in DPSK/QAM modes when the descrambler is enabled and sets bits 8 and 7 of the Status Register to '11' when 32 consecutive 1s appear at the output of the descrambler. To avoid possible ambiguity, the 'Scrambled 1s' detector is disabled when continuous unscrambled 1s are detected.

The 'Continuous 0s' detector sets bits 8 and 7 of the Status Register to '10' when NX consecutive 0s have been received, NX being 32 except when DPSK/QAM Start-Stop mode has been selected, in which case NX = 2N + 4 where N is the number of bits per character including the Start, Stop and any Parity bits.

All of these pattern detectors will hold the 'detect' output for 12 bit times after the end of the detected pattern unless the received bit rate or operating mode is changed, in which case the detectors are reset within 2 msec.

1.5.9 Rx Data Register and USART

A flexible Rx USART is provided for all modem modes, meeting the requirements of V.14 for QAM and DPSK modems. It can be programmed to treat the received data bit stream as Synchronous data or as Start-Stop characters.

In Synchronous mode the received data bits are all fed into the Rx Data Buffer which is copied into the C-BUS Rx Data Register after every 8 bits.

In Start-Stop mode the USART Control logic looks for the start of each character, then feeds only the required number of data bits (not parity) into the Rx Data Buffer. The parity bit (if used) and the presence of a Stop bit are then checked and the data bits in the Rx Data Buffer copied to the C-BUS Rx Data Register.

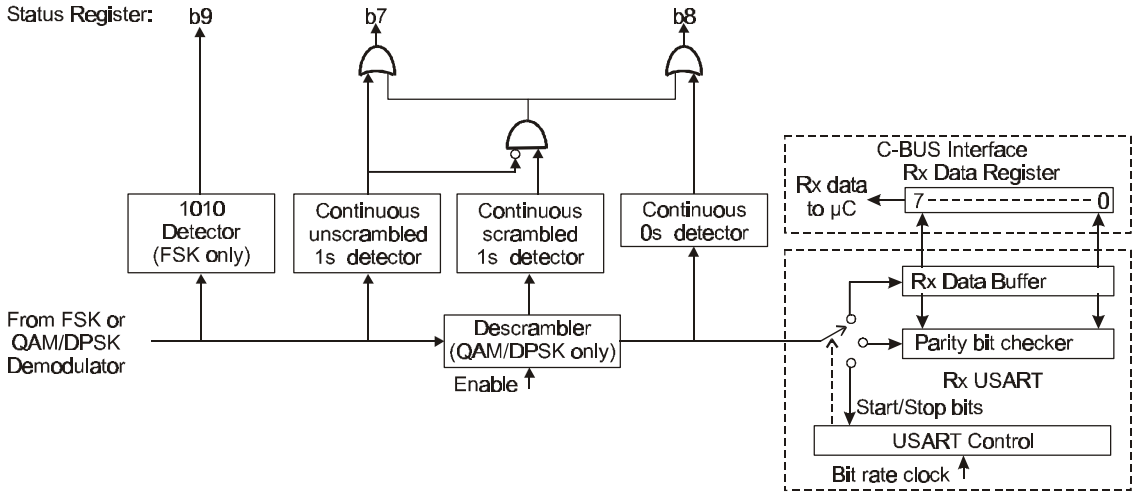


Figure 8a Rx Modem Data Paths

Whenever a new character is copied into the C-BUS Rx Data Register, the Rx Data Ready flag bit of the Status Register is set to '1' to prompt the µC to read the new data and, in Start-Stop mode, the Even Rx Parity flag bit of the Status Register is updated.

In Start-Stop mode, if the Stop bit is missing (received as a '0' instead of a '1') the received character will still be placed into the Rx Data Register and the Rx Data Ready flag bit set, but, unless allowed by the V.14 overspeed option described below, the Status Register Rx Framing Error bit will also be set to '1' and the USART will re-synchronise onto the next '1' – '0' (Stop – Start) transition. The Rx Framing Error bit will remain set until the next character has been received.

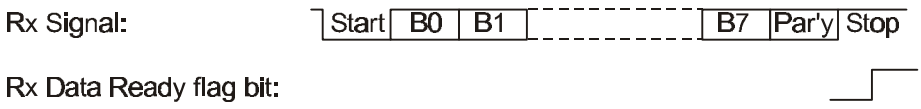


Figure 8b Rx USART Function (Start-Stop mode, 8 Data Bits + Parity)

If the µC has not read the previous data from the Rx Data Register by the time that new data is copied to it from the Rx Data Buffer then the Rx Data Overflow flag bit of the Status Register will be set to 1.

The Rx Data Ready flag and Rx Data Overflow bits are cleared to 0 when the Rx Data Register is read by the µC.

For QAM and DPSK Start-Stop modes, V.14 requires that the receive USART be able to cope with missing Stop bits; up to 1 missing Stop bit in every 8 consecutive received characters being allowed for the +1% overspeed (basic signalling rate) V.14 mode and 1 in 4 for the +2.3% overspeed (extended signalling rate) mode.

To accommodate the requirements of V.14, the CMX878 Rx Mode Register can be set for 0, +1% or +2.3% overspeed operation in QAM or DPSK Start-Stop modes. Missing Stop bits beyond those allowed by the selected overspeed option will set the Rx Framing Error flag bit of the Status Register.

In order that received Break signals can be handled correctly in V.14 Rx overspeed mode, a received character which has all bits '0', including the Stop and any Parity bits, will always cause the Rx Framing Error bit to be set and the USART to re-synchronise onto the next '1' – '0' transition. Additionally the received Continuous 0s detector will respond when more than 2M + 3 consecutive '0's are received, where 'M' is the selected total number of bits per character including Stop and any Parity bits.

1.5.10 DAC

This is an 8-bit linear Digital to Analogue Converter. The primary intended purpose is that it will be used for controlling a current drawn from the line as part of a line characterisation function; it could, however, be used for any other purpose if so required. It is powered from the Regulated Supply. The output level is set by programming the C-BUS DAC Control Register – see the register description for more information.

Note that when the DAC is enabled, the output impedance is set to a nominal 5kΩ. When used in conjunction with the circuit in Figure 4a and with the gyrator disabled, the programmed DAC voltage will give a current out of the ICTRL pin of approximately (DAC voltage – 0.7V) / 5kΩ. The current drawn from the line will be approximately 200 times this current.

1.5.11 ADC

The Analogue to Digital Converter has two major components: a dedicated 8-bit DAC and a comparator. See Figure 1c. The comparator compares the output of the DAC (ADC-REF voltage) with the input signal ADCIN. The output of the comparator is fed to the C-BUS. See also the register description for more information.

There are two main ways of using this ADC:

i. Line Drop-out Detection, e.g. testing for an extension going off-hook

Determine the Line voltage at below which the microcontroller needs to be alerted and calculate the corresponding divided-down voltage at ADCIN. Program ADC-REF to this voltage. Read the Line/Wakeup Event Register to clear any false drop-out detection which may occur at the moment when the ADC circuit is programmed. Set mask bits to enable the IRQ.

When the Line voltage drops below the threshold, Line/Wakeup Event Register bit 8 will go to 1, and consequently so will Status Register bit 14. The microcontroller will then detect the IRQ and will read the Status Register and the Line/Wakeup Event Register which will indicate the Line Drop-out Event. As a guard against a false drop-out caused by noise, the microcontroller then could poll the ADC comparator level (Line/Wakeup Event Register bit 9) to confirm that it is a reliable 0. Alternatively, it could measure the voltage by using the following successive approximation technique.

ii. Line Voltage Measurement using Successive Approximation

By programming successive values of ADC-REF and reading the comparator output (bit 9) from the Line/Wakeup Event Register, the voltage at ADCIN (and by calculation the Line voltage) can be determined. The technique for Successive Approximation is:

Set the MSB (bit 7) of the ADC-REF register to 1 and all other bits to 0. Read the ADC comparator level (bit 9 of the Line/Wakeup Event Register); if it is 1 then keep the MSB at 1, otherwise set it to 0. Repeat this procedure for the next most significant bit (bit 6) and continue until the LSB (bit 0). The final value represents the voltage at ADCIN, i.e. :

Measured level is: (AV_{DD} / 2) x (final value / 255)

Note that this configuration is intended to give an indication of the DC value of the line rather than a precise time-quantised value (which would require a sample-and-hold circuit to be added). Capacitor C18 de-emphasises the effect of AC signals.

1.5.12 C-BUS Interface

This block provides for the transfer of data and control or status information between the CMX878's internal registers and the µC over the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the µC which may be followed by a one or more data byte(s) sent from the µC to be written into one of the CMX878's Write Only Registers, or a one or more byte(s) of data read out from one of the CMX878's Read Only Registers, as illustrated in Figure 9.

Data sent from the µC on the Command Data line is clocked into the CMX878 on the rising edge of the Serial Clock input. Reply Data sent from the CMX878 to the µC is valid when the Serial Clock is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Figure 15 gives detailed C-BUS timing requirements.

For all C-BUS data transfers the regulated supply must be provided to AV_{DD} and DV_{DD}, powering the C-BUS circuitry and the microcontroller. The C-BUS *registers* are split between those which have their contents maintained by the Standby Supply ($SBYV_{DD}$) and those which have their contents maintained by the Regulated Supply (DV_{DD}).

In a Line-powered application it is necessary to minimise the current drawn from the Line when in the on-hook state. For this reason it is intended that power should be removed from the Regulated Supply when it is not required. This will de-power the microcontroller and the functions of the CMX878 which are not required in this mode, for example the crystal oscillator, the V_{BIAS} generator, the MODEM & TONES PROCESSOR block, the Line DAC and ADC, and the associated registers.

The Standby Supply operates independently of the Regulator and this powers the functions which must remain present in the on-hook state. These functions are the Line Reversal / Ring detectors and the WAKE input detector. It also powers the three **'Standby Supply Registers'** – these are:

The Configuration Register. This is used to: enable the standby event detectors; to enable/disable the Regulated Supply; and to define certain states. As an example, the microcontroller could program this register to enable detection of a Line Reversal and de-power the Regulated Supply. This will remove power from the microcontroller but will leave the Line Reversal detector enabled on the Standby Supply. When a Line Reversal is later detected, power to the microcontroller will be restored and it will begin its program.

The Supplementary Standby Register. A general purpose write/read register which can be used to store any values that must survive a drop-out of the Regulated Supply.

The Line/Wakeup Event Register. This is read from in order to determine which detector events have occurred and to check that the contents of the Standby Supply Registers are valid. (It also indicates the output of the Line DAC, although this additionally requires the Regulated Supply to be present.)

The CMX878 will automatically power up the microcontroller (via the Regulated Supply) when:

i. The circuit is initially plugged into Line Power. The microcontroller should then read the Line/Wakeup Event Register and will determine that the Standby Supply Registers have 'INVALID' contents. It will then proceed with programming the CMX878 registers.

ii. A Line Reversal, Ring, or WAKE input event has occurred (note that the Reversal and Ring detectors must have been previously enabled in the Configuration Register for them to operate). The microcontroller will read the Line/Wakeup Event Register, it will determine that the Standby Supply Registers have 'VALID' contents, and it will determine and act upon the Event which has occurred.

Definitions of 'VALID' and 'INVALID': These terms describe the data integrity of the Standby Supply Registers. The CMX878 monitors the Standby Supply and will set the 'VALID' bit (bit 5) of the Line/Wakeup Event Register accordingly. 1 = 'VALID'. 0 = 'INVALID'.

Upon first application of line power (or after a line interruption severe enough to drop $SBYV_{DD}$ below its acceptable level) this bit will be set to 0 to indicate 'INVALID' register contents. When the microcontroller has read this bit as being 'INVALID' it should ignore the value of all other bits read back. It should then proceed to program both the Configuration Register and the Supplementary Standby Register to the required values. The Standby Supply Register contents are now 'VALID' and bit 5 of the Line/Wakeup Event Register will be set to 1.

The microcontroller must check the 'VALID' status at the start of its program after it has powered up. Also if the microcontroller is able to detect certain fault conditions (e.g. with a brown-out detector or a watchdog timer) it should again check the 'VALID' status.

All other C-BUS Registers are concerned with the control of functions which operate from the Regulated Supply, usually with the Line off-hook; for example operation of the MODEM & TONES PROCESSOR block. Note that these registers will lose their contents whenever the Regulated Supply is de-powered.

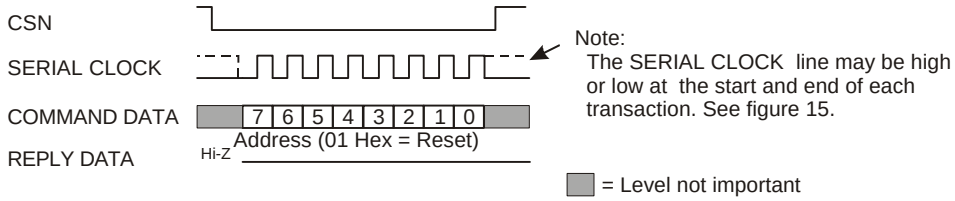
Interrupts: The only register bit which can directly cause an interrupt is bit 14 (IRQ) of the Status Register and thus all interrupts operate through this bit. When this bit and the IRQNEN bit (bit 6) of the General Control Register are both 1 then the IRQN output pin will be pulled low (to Vss).

The following C-BUS addresses and registers are used by the CMX878:

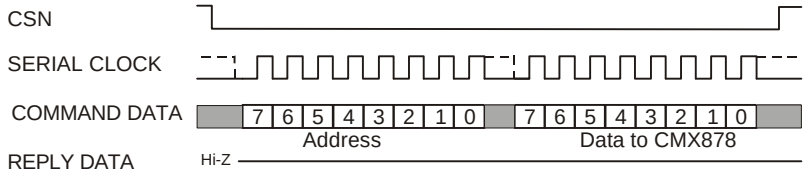
Register Name	Type	Address	From Supply: Standby [S] or Regulated [R]
General Reset Command	address only, no data	$01	R
General Control Register	16-bit write-only	$E0	R
Transmit Mode Register	16-bit write-only	$E1	R
Receive Mode Register	16-bit write-only	$E2	R
Transmit Data Register	8-bit write-only	$E3 & $E4	R
Receive Data Register	8-bit read-only	$E5	R
Status Register	16-bit read-only	$E6	R
Programming Register	16-bit write-only	$E8	R
Line Control Register	8-bit write-only	$EC	R
DAC Control Register	8-bit write-only	$ED	R
ADC Control Register	8-bit write-only	$EE	R
Configuration Register Write	16-bit write	$F0	S
Configuration Register Read	16-bit read	$F1	S
Supplementary Standby Register Write	16-bit write	$F2	S
Supplementary Standby Register Read	16-bit read	$F3	S
Line/Wakeup Event Register	16-bit read-only	$F4	S

Note: The C-BUS addresses $E9, $EA and $EB are allocated for production testing and should not be accessed in normal operation.

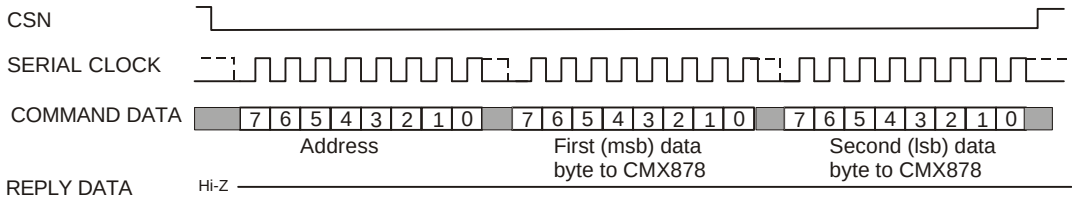
a) Single byte from µC



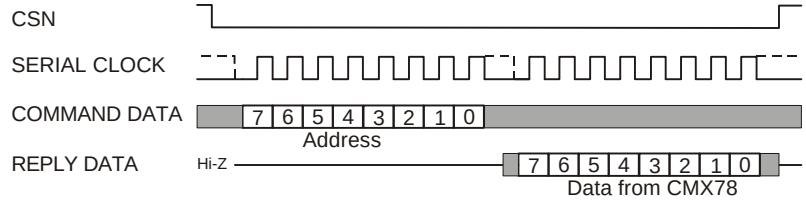
b) One Address and one Data byte from µC



c) One Address and 2 Data bytes from µC



d) One Address byte from µC and one Reply byte from CMX878



e) One Address byte from µC and 2 Reply bytes from CMX878

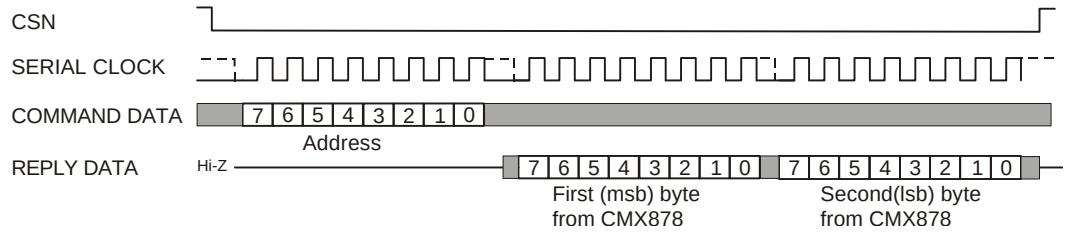


Figure 9 C-BUS Transactions

1.5.12.1 General Reset Command

General Reset Command (no data) C-BUS address $01

This command resets the device and clears all bits of the General Control, Transmit Mode, Receive Mode, Line Control, DAC Mode and ADC Mode Registers and bits 15 and 13-0 of the Status Register. It does not affect the Standby Supply Registers.

1.5.12.2 Configuration Register

Configuration Register: 16-bit read & write C-BUS addresses: write $F0 ; read $F1

This is a 'Standby Supply Register'.

Bit 0	Writing 1 enables Detection of Line Reversal Event
Bit 1	Writing 1 enables Detection of Start of Ring Event
Bit 2	Writing 1 enables Detection of End of Ring Burst Event
Bit 3	Set this bit to 0
Bit 4	Regulated Supply Enable 1 powers the Regulated Supply. 0 de-powers up the Regulated Supply. Note that this bit can get set to 1 by events other than a C-BUS write – see below.
Bits 5-15	General Purpose Bits 5-15

Whenever a C-BUS 'write' is made to this register, its contents will be deemed VALID and Line/Wakeup Event Register bit 5 will be set to 1. Any loss of the Standby Supply will invalidate the contents of this register and it will need to be (re-) programmed; read Line/Wakeup Event Register bit 5 to check if this is necessary.

Bits 0-2. Depending on which type of Line Reversal or Ring event is to be detected, set one of these bits to logic 1. If it is necessary to distinguish between a Line Reversal and a Ring then set bit 0 to 1; the microcontroller will be alerted to the first RT pin edge and can then monitor any further activity by reading the RD and RT bits from the Line/Wakeup Event Register.

Bit 3. Set this bit to 0.

When one of the above Detection Events occurs, bit 4 will be set to 1 powering the Regulated Supply and the microcontroller; also the Status Register bit 14 will be set to 1.

Bit 4. When this bit is set to 0* the Regulated Supply will be de-powered and only the circuits powered by the Standby Supply will remain active (Ring, Line Reversal Detectors, WAKE input, Standby Supply Registers). Both the microcontroller and the C-BUS will be deactivated and this state will remain until a Wake Event occurs. The contents of all non-Standby registers will be lost.

This bit should be set to 1 when the Regulated Supply is to remain in its powered state.

This bit is also gets set to 1 by:

An Event – any of Line/Wakeup Event Register bits 0-3 going to 1 (as caused by a Line Reversal, Ring or WAKE pin Event),

A Power-on-Reset – the Line/Wakeup Event Register bit 5 goes to 0 (when the contents of the Standby Registers are NOT VALID due to a previous loss of the Standby Supply).

*Note: Because an event indicated by the Line/Wakeup Event Register can set this bit, the Line/Wakeup Event Register must always be read (clearing it) before de-powering the Regulated Supply with Bit 4.

Bits 5-15 are general purpose register bits which, being powered from the Standby Supply, will retain their values even when the Regulated Supply is absent. These bits can be set by the microcontroller to represent various operating states. Consequently if the Regulated Supply is temporarily lost (e.g. a Central Office generated line break following an off-hook transition), when the Regulated Supply returns, the microcontroller can read back these values to re-establish the position in its program.

1.5.12.3 Supplementary Standby Register

Supplementary Standby Register: 16-bit read and write C-BUS addresses: write $F2 ; read $F3

This is a 'Standby Supply Register' and allows for data storage even when the Regulated Supply is removed. The bits can be used by the application for any purpose

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	a 16-bit general purpose register – set as required															

1.5.12.4 Line/Wakeup Event Register

Line/Wakeup Event Register: 16-bit read-only C-BUS address $F4

This is a 'Standby Supply Register'.

Bit 0	1 when a Line Reversal Event has occurred
Bit 1	1 when a Start of Ring Event has occurred
Bit 2	1 when an End of Ring Burst Event has occurred
Bit 3	1 when a WAKE pin Event has occurred
Bit 4	Reserved for future use. Currently set to 0
Bit 5	1 when the contents of the Standby Supply Registers are VALID.
Bit 6	RD. The equivalent logic level at the ring detector's RD input
Bit 7	RT. The equivalent logic level at the ring detector's RT input
Bit 8	1 when a Line ADC Drop-out Event has occurred
Bit 9	ADC comparator level (0 = ADCIN pin < ADC-REF, else 1)
Bits 10-15	Reserved for future use. Currently set to 000000

Bit 0. A 'Line Reversal Event' is caused by one rising edge on the RD pin.
Bit 1. A 'Start of Ring Event' is caused by two falling edges on the RD pin within the period that the RT pin is low.
Bit 2. An 'End of Ring Burst Event' is as per the 'Start of Ring Event' but it does not occur until the RT pin goes back high.
These above three Events can only occur if they were previously enabled in the Configuration Register.

Bit 3. A 'WAKE pin Event' is when the WAKE pin makes a 0 to 1 transition.

When one of Bits 0-3 goes to 1, bit 4 of the Configuration Register will be set to 1, powering up the Regulated Supply and the microcontroller; also Status Register bit 14 will be set to 1.

Bit 4. Currently set to 0.

Bit 5. This bit determines the validity of the register bits which are powered from the Standby Supply. After reading this register, the microcontroller should consider the level of this bit FIRST.

Upon any drop-out of the Standby Supply, this bit will be set to 0 to indicate that the contents of all other register bits in the Standby Supply Registers cannot be relied upon and are hence termed NOT VALID. Whenever the device is in this NOT VALID state, it will also set Configuration Register bit 4 to 1 in order to ensure that the Regulated Supply and microcontroller are powered up.

Whenever the microcontroller reads a NOT VALID state, it should proceed to program the Configuration Register and the Supplementary Standby Register. Programming the Configuration Register will make its contents VALID and Line/Wakeup Event Register bit 5 will be set to 1.

Bits 6 and 7. The equivalent logic levels on the ring detector pins RD and RT can be sampled via these bits.

Bit 8. A 'Line ADC Drop-out Event' occurs when the Line ADC voltage has fallen below the programmed ADC-REF voltage. When Bit 8 goes to 1, Status Register bit 14 will be set to 1 – this will also give an interrupt if the relevant flag bits are set. The 'Line ADC Drop-out Event' is disabled when the ADC Control Register is set to all 0's.

Bit 9. The level on the output of the Line ADC comparator.

Bits 0-3 and Bit 8 are cleared after reading this register.

1.5.12.5 Line Control Register

Line Control Register: 8-bit write-only. C-BUS address $EC

This register controls sets various logic outputs which can be used to control external circuits.

Bit 0	Logic level CLID Z EN pin (Caller Line ID Z control)
Bit 1	Logic level at GP OP1 pin (a General Purpose logic pin)
Bit 2	Logic level at GP OP2 pin (a General Purpose logic pin)
Bit 3	Logic level at GP OP3 pin (a General Purpose logic pin)
Bit 4	Logic level at GYON (Gyrator Enable)
Bit 5	Reserved for future use. Set to 0.
Bit 6	Reserved for future use. Set to 0.
Bit 7	Reserved for future use. Set to 0.

1.5.12.6 DAC Control Register

DAC Control Register: 8-bit write-only C-BUS address $ED

Bit:	7	6	5	4	3	2	1	0
	Register Value							

When the DAC is enabled, the voltage produced is:

AV_{DD} x (Register Value / 255)

via an output impedance of approximately 5kΩ.

All bits of this register are cleared to 0 by a General Reset command. A setting of all 0's will disable and powersave the DAC.

The state of the ICTRL pin is also dependent on the mode of the Regulator and Gyrator as shown in the following table:

Mode of Operation	Regulator Enabled?	Gyrator Enabled?	DAC Enabled?	ICTRL OUTPUT
On-hook, min. current	N	N	N	Vss
On-hook, Regulator ON	Y	N	N	Low Z Vss
Off-hook	Y	Y	N	Hi Z
Programmed Line Current Draw	Y	N	Y	As programmed on the DAC

1.5.12.7 ADC Control Register

ADC Control Register: 8-bit write-only. C-BUS address $EE

Bit:	7	6	5	4	3	2	1	0
	Register Value							

The ADC comprises an 8 bit programmable reference voltage, ADC-REF, which is compared with the voltage at the ADCIN pin. The output of the comparator is available in the Line/Wake Event Register.

The ADC is designed to operate with signals between 0V (Vss) and half supply (AV_{DD} / 2). The external divider will normally be configured to limit the ADCIN pin signals to within this range.

The ADC-REF voltage is: (AV_{DD} / 2) x (Register Value / 255)

All bits of this register are cleared to 0 by a General Reset command. A setting of all 0s will powersave the ADC circuit and will force the output of the comparator to 1.

The ADC can be used to measure a voltage or detect a drop-out. See Section 1.5.11 for details.

1.5.12.8 General Control Register

General Control Register: 16-bit write-only. C-BUS address $E0

This register controls general features of the MODEM & TONES PROCESSOR block such as the Powersave and Loopback modes, and the IRQ mask bits. It also allows the fixed compromise equalisers in the Tx and Rx signal paths to be disabled if desired, and sets the internal clock dividers to use either a 11.0592 or a 12.288 MHz XTAL frequency.

All bits of this register are cleared to 0 by a General Reset command.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	Xtal freq	LB	Equ	0	Pwr	Rst	Irqn en	IRQ Mask Bits					

General Control Register b15-13: Reserved, set to 000

General Control Register b12: Xtal frequency
This bit should be set according to the Xtal frequency.

b12 = 1	11.0592MHz
b12 = 0	12.2880MHz

General Control Register b11: Analogue Loopback test mode
This bit controls the analogue loopback test mode. Note that in loopback test mode both Transmit and Receive Mode Registers should be set to the same modem type and band or bit rate.

b11 = 1	Local analogue loopback mode enabled
b11 = 0	No loopback (normal modem operation)

General Control Register b10: Tx and Rx Fixed Compromise Equalisers
This bit allows the Tx and Rx fixed compromise equalisers in the modem transmit and receive filter blocks to be disabled.

b10 = 1	Disable equalisers
b10 = 0	Enable equalisers (600, 1200 or 2400bps modem modes)

General Control Register b9: Reserved, set to 0

General Control Register b8: Powerup
This bit controls the internal power supply to most of the internal circuits, including the Xtal oscillator, V_{BIAS} supply and the MODEM & TONES PROCESSOR block. It does not affect the DAC and ADC. It does not affect the circuits which run off the Standby Supply.

Note that the General Reset command clears this bit, putting the MODEM & TONES PROCESSOR block into Powersave mode.

When the device is switched from Powersave mode to normal operation by setting the Powerup bit to 1, the Reset bit should also be set to 1 and should be held at 1 for about 20ms while the internal circuits, Xtal oscillator and V_{BIAS} stabilise before starting to use the transmitter or receiver.

Changing the Powerup bit from 0 to 1 clears all bits of the Transmit Mode and Receive Mode Registers and clears b15 and b13-0 of the Status Register.

b8 = 1	MODEM & TONES PROCESSOR BLOCK powered up normally
b8 = 0	MODEM & TONES PROCESSOR BLOCK Powersave

General Control Register b7: Reset
Setting this bit to 1 resets the CMX878's internal circuitry, clearing all bits of the Transmit and Receive Mode Registers and b13-0 of the Status Register.

b7 = 1	Internal circuitry in a reset condition.
b7 = 0	Normal operation

General Control Register b6: IRQNEN (IRQN O/P Enable)
Setting this bit to 1 enables the IRQN output pin.

b6 = 1	IRQN pin driven low (to V_{SS}) if the IRQ bit of the Status Register = 1
b6 = 0	IRQN pin disabled (high impedance)

General Control Register b5-0: IRQ Mask bits
These bits affect the operation of the IRQ bit of the Status Register as described in section 1.5.12.13.

1.5.12.9 Transmit Mode Register

Transmit Mode Register: 16-bit write-only. C-BUS address $E1

This register controls the CMX878 transmit signal type and level. All bits of this register are cleared to 0 by a General Reset command or when b7 (Reset) of the General Control Register is 1.

Bit:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx mode = modem				Tx level			Guard tone		Scrambler		Start-stop / synch data		# data bits / synch data source		
Tx mode = DTMF/Tones				Tx level			Unused, set to 0000				DTMF or Tone select				
Tx mode = Disabled				Set to 0000 0000 0000											

Tx Mode Register b15-12: Tx mode

These 4 bits select the transmit operating mode.

b15	b14	b13	b12		
1	1	1	1	V.22bis 2400 bps QAM	High band (Answering modem)
1	1	1	0	"	Low band (Calling modem)
1	1	0	1	V.22/Bell 212A 1200 bps DPSK	High band (Answering modem)
1	1	0	0	"	Low band (Calling modem)
1	0	1	1	V.22 600 bps DPSK	High band (Answering modem)
1	0	1	0	"	Low band (Calling modem)
1	0	0	1	V.21 300 bps FSK	High band (Answering modem)
1	0	0	0	"	Low band (Calling modem)
0	1	1	1	Bell 103 300 bps FSK	High band (Answering modem)
0	1	1	0	"	Low band (Calling modem)
0	1	0	1	V.23 FSK	1200 bps
0	1	0	0	"	75 bps
0	0	1	1	Bell 202 FSK	1200 bps
0	0	1	0	"	150 bps
0	0	0	1	DTMF / Tones	
0	0	0	0	Transmitter disabled	

Tx Mode Register b11-9: Tx level

These 3 bits set the gain of the Tx Level Control block.

b11	b10	b9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Tx Mode Register b8-7: Tx Guard tone (QAM, DPSK modes)
These 2 bits select the guard tone to be transmitted together with highband QAM or DPSK. Set both bits to 0 in FSK modes.

b8	b7	
1	1	Tx 550Hz guard tone
1	0	Tx 1800Hz guard tone
0	x	No Tx guard tone

Tx Mode Register b6-5: Tx Scrambler (QAM, DPSK modes)
These 2 bits control the operation of the Tx scrambler used in QAM and DPSK modes. Set both bits to 0 in FSK modes.

b6	b5	
1	1	Scrambler enabled, 64 ones detect circuit enabled (normal use)
1	0	Scrambler enabled, 64 ones detect circuit disabled
0	x	Scrambler disabled

Tx Mode Register b4-3: Tx Data Format (QAM, DPSK, FSK modes)
These two bits select Synchronous or Start-stop mode and the addition of a parity bit to transmitted characters in Start-stop mode.

b4	b3	
1	1	Synchronous mode
1	0	Start-stop mode, no parity
0	1	Start-stop mode, even parity bit added to data bits
0	0	Start-stop mode, odd parity bit added to data bits

Tx Mode Register b2-0: Tx Data and Stop bits (QAM, DPSK, FSK Start-Stop modes)
In Start-stop mode these three bits select the number of Tx data and stop bits.

b2	b1	b0	
1	1	1	8 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
0	1	0	6 data bits, 1 stop bit
0	0	1	5 data bits, 2 stop bits
0	0	0	5 data bits, 1 stop bit

Tx Mode Register b2-0: Tx Data source (QAM, DPSK, FSK Synchronous mode)
In Synchronous mode (b4-3 = 11) these three bits select the source of the data fed to the Tx FSK or QAM/DPSK scrambler and modulator.

b2	b1	b0	
1	x	x	Data bytes from Tx Data Buffer
0	1	1	Continuous 1s
0	1	0	Continuous 0s
0	0	x	Continuous V.22bis handshake S1 pattern dibits ’00,11’ in DPSK and QAM modes, continuous alternating 1s and 0s in all other modes.

Tx Mode Register b8-0: DTMF/Tones mode

If DTMF/Tones transmit mode has been selected (Tx Mode Register b15-12 = 0001) then b8-5 should be set to 0000 and b4-0 will select a DTMF signal or a fixed tone or one of four programmed tones or tone pairs for transmission.

b4 = 0: Tx fixed tone or programmed tone pair

b3	b2	b1	b0	Tone frequency (Hz)	
0	0	0	0	No tone	
0	0	0	1	697	
0	0	1	0	770	
0	0	1	1	852	
0	1	0	0	941	
0	1	0	1	1209	
0	1	1	0	1336	
0	1	1	1	1477	
1	0	0	0	1633	
1	0	0	1	1300	(Calling tone)
1	0	1	0	2100	(Answer tone)
1	0	1	1	2225	(Answer tone)
1	1	0	0	Tone pair TA	Programmed Tx tone or tone pair, see 1.5.12.14
1	1	0	1	Tone pair TB	“
1	1	1	0	Tone pair TC	“
1	1	1	1	Tone pair TD	“

b4 = 1: Tx DTMF

b3	b2	b1	b0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

1.5.12.10 Receive Mode Register

Receive Mode Register: 16-bit write-only. C-BUS address $E2

This register controls the CMX878 receive signal type and level.

All bits of this register are cleared to 0 by a General Reset command or when b7 (Reset) of the General Control Register is 1.

Bit:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rx mode = modem				Rx level			Eq	Descrambl		Start-stop/Synch			No. of bits and parity		
Rx mode = Tones detect				Rx level			DTMF/Tones/Call Progress select								
Rx mode = Disabled				Set to 0000 0000 0000											

Rx Mode Register b15-12: Rx mode
These 4 bits select the receive operating mode.

b15	b14	b13	b12		
1	1	1	1	V.22bis 2400 bps QAM	High band (Calling modem)
1	1	1	0	"	Low band (Answering modem)
1	1	0	1	V.22/Bell 212A 1200 bps DPSK	High band (Calling modem)
1	1	0	0	"	Low band (Answering modem)
1	0	1	1	V.22 600 bps DPSK	High band (Calling modem)
1	0	1	0	"	Low band (Answering modem)
1	0	0	1	V.21 300 bps FSK	High band (Calling modem)
1	0	0	0	"	Low band (Answering modem)
0	1	1	1	Bell 103 300 bps FSK	High band (Calling modem)
0	1	1	0	"	Low band (Answering modem)
0	1	0	1	V.23 FSK	1200 bps
0	1	0	0	"	75 bps
0	0	1	1	Bell 202 FSK	1200 bps
0	0	1	0	"	150 bps
0	0	0	1	DTMF, Programmed tone pair, Answer Tone, Call Progress detect	
0	0	0	0	Receiver disabled	

Rx Mode Register b11-9: Rx level
These three bits set the gain of the Rx Gain Control block.

b11	b10	b9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Rx Mode Register b8: Rx Auto-equalise (DPSK/QAM modem modes)
This bit controls the operation of the receive DPSK/QAM auto-equaliser. Set to 0 in FSK modes. Set to 1 in 2400bps QAM mode.

b8 = 1	Enable auto-equaliser
b8 = 0	DPSK mode: Auto-equaliser disabled QAM mode : Auto-equaliser settings frozen

Rx Mode Register b7-6: Rx Scrambler (DPSK/QAM modem modes)
These 2 bits control the operation of the Rx descrambler used in QAM and DPSK modes. Set both bits to 0 in FSK modes

b7	b6	
1	1	Descrambler enabled, 64 ones detect circuit enabled (normal use)
1	0	Descrambler enabled, 64 ones detect circuit disabled
0	x	Descrambler disabled

Rx Mode Register b5-3: Rx USART Setting (QAM, DPSK, FSK modem modes)
These three bits select the Rx USART operating mode. The 1% and 2.3% overspeed options apply to DPSK/QAM modes only.

b5	b4	b3	
1	1	1	Rx Synchronous mode
1	1	0	Rx Start-stop mode, no overspeed
1	0	1	Rx Start-stop mode, +1% overspeed (1 in 8 missing Stop bits allowed)
1	0	0	Rx Start-stop mode, +2.3% overspeed (1 in 4 missing Stop bits allowed)
0	x	x	Rx USART function disabled

Rx Mode Register b2-0: Rx Data bits and parity (QAM, DPSK, FSK Start-Stop modem modes)
In Start-stop mode these three bits select the number of data bits (plus any parity bit) in each received character. These bits are ignored in Synchronous mode.

b2	b1	b0	
1	1	1	8 data bits + parity
1	1	0	8 data bits
1	0	1	7 data bits + parity
1	0	0	7 data bits
0	1	1	6 data bits + parity
0	1	0	6 data bits
0	0	1	5 data bits + parity
0	0	0	5 data bits

Rx Mode Register b2-0: Tones Detect mode
In Tones Detect Mode (Rx Mode Register b15-12 = 0001) b8-3 should be set to 000000
Bits 2-0 select the detector type.

b2	b1	b0	
1	0	0	Programmable Tone Pair Detect
0	1	1	Call Progress Detect
0	1	0	2100, 2225Hz Answer Tone Detect
0	0	1	DTMF Detect
0	0	0	Disabled

1.5.12.11 Tx Data Register

Tx Data Register: 8-bit write-only. C-BUS addresses $E3 and $E4

Bit:	7	6	5	4	3	2	1	0
	Data bits to be transmitted							

In Synchronous Tx data mode this register contains the next 8 data bits to be transmitted. Bit 0 is transmitted first.

In Tx Start-Stop mode the specified number of data bits will be transmitted from this register (b0 first). A Start bit, a Parity bit (if required) and Stop bit(s) will be added automatically.

This register should only be written to when the Tx Data Ready bit of the Status Register is 1.

C-BUS address $E3 should normally be used, $E4 is for implementing the V.14 overspeed transmission requirement in Start-Stop mode, see section 1.5.1.

1.5.12.12 Rx Data Register

Rx Data Register: 8-bit read-only. C-BUS address $E5

Bit:	7	6	5	4	3	2	1	0
	Received data bits							

In unformatted Rx data mode this register contains 8 received data bits, b0 of the register holding the earliest received bit, b7 the latest.

In Rx Start-Stop data mode this register contains the specified number of data bits from a received character, b0 holding the first received bit.

1.5.12.13 Status Register

Status Register: 16-bit read-only. C-BUS address $E6

Bits 13-0 of this register are cleared to 0 by a General Reset command or when b7 (Reset) of the General Control Register is 1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ	RD	PF	See below for uses of these bits												

The meanings of the Status Register bits 12-0 depend on whether the receive circuitry is in Modem or Tones Detect mode.

Status Register bits:

	Rx Modem modes	**Rx Tones Detect modes**	**** IRQ Mask bit**
b15	IRQ		
b14	Set to 1 when a Line/Wakeup Event has occurred		b5
b13	Programming Flag bit. See 1.5.12.14		b4
b12	Set to 1 on Tx data ready. Cleared by write to Tx Data Register		b3
b11	Set to 1 on Tx data underflow. Cleared by write to Tx Data Register		b3
b10	1 when energy is detected in Rx modem signal band	1 when energy is detected in Call Progress band or when both programmable tones are detected	b2
b9	1 when S1 pattern (double DPSK dibit 00,11) is detected in DPSK or QAM modes, or when '1010..' pattern is detected in FSK modes	0	b1
b8	See following table	0	b1
b7	See following table	1 when 2100Hz answer tone or the second programmable tone is detected	b1
b6	Set to 1 on Rx data ready. Cleared by read from Rx Data Register	1 when 2225Hz answer tone or the first programmable tone is detected	b0
b5	Set to 1 on Rx data overflow. Cleared by read from Rx Data Register	1 when DTMF code is detected	b0
b4	Set to 1 on Rx framing error	0	-
b3	Set to 1 on even Rx parity	Rx DTMF code b3, see table	-
b2	QAM/DPSK Rx signal quality b2	Rx DTMF code b2	-
b1	QAM/DPSK Rx signal quality b1	Rx DTMF code b1	-
b0	QAM/DPSK Rx signal quality b0 or FSK frequency demodulator output	Rx DTMF code b0	-

Notes: ** This column shows the corresponding IRQ Mask bits in the General Control Register. A 0 to 1 transition on any of the Status Register bits 14-5 will cause the IRQ bit b15 to be set to 1 if the corresponding IRQ Mask bit is 1. The IRQ bit is cleared by a read of the Status Register or a General Reset command or by setting b7 or b8 of the General Control Register to 1.

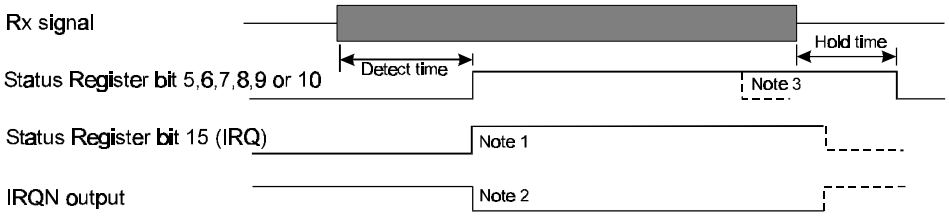
A spurious 'continuous 0s' detect may be generated within 4msec of changing the Rx Mode Register to any of the QAM or DPSK modes.

The operation of the data demodulator and pattern detector circuits within the CMX878 does not depend on the state of the Rx energy detect function.

Decoding of Status Register b8,7 in Rx Modem Modes, see also Figure 8a

b8	b7	Descrambler disabled	Descrambler enabled (DPSK/QAM modes only)
1	1	-	Continuous scrambled 1s (see note)
1	0	Continuous unscrambled 0s	Continuous scrambled 0s
0	1	Continuous unscrambled 1s	Continuous unscrambled 1s
0	0	-	-

When the descrambler is enabled then detection of continuous unscrambled 1s will inhibit the continuous scrambled 1s detector.



Notes:
1. IRQ will go high only if appropriate IRQ Mask bit in General Control Register is set. The IRQ bit is cleared by a read of the Status Register.
2. IRQN o/p will go low when IRQ bit high if IRQNEN bit of General Control Register is set
3. In Rx Modem modes Status Register bits 5 and 6 are set by a Rx Data Ready or Rx Data Underflow event and cleared by a read of the Rx Data Register

Figure 10a Operation of Status Register bits 5-10

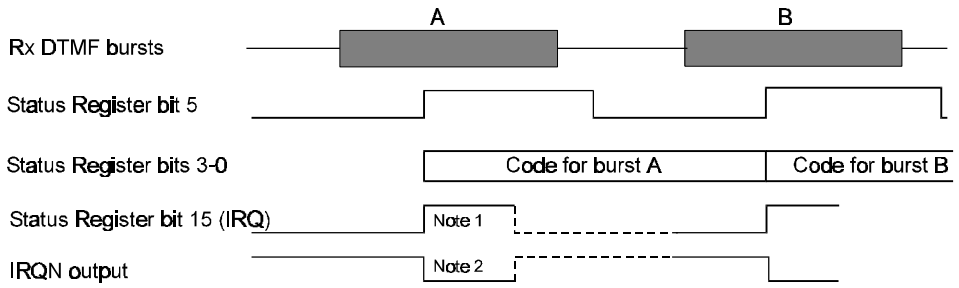
The IRQN output pin will be pulled low (to V_{SS}) when the IRQ bit of the Status Register and the IRQNEN bit (b6) of the General Control Register are both 1.

Changes to Status Register bits caused by a change of Tx or Rx operating mode can take up to 150µs to take effect.

In Powersave mode or when the Reset bit (b7) of the General Control Register is 1 bit 15 of the Status Register continues to operate.

The 'continuous 0' and 'continuous 1' detectors monitor the Rx signal after the QAM/DPSK descrambler, (see Figure 8a) and hence will detect continuous 1s or 0s if the descrambler is disabled, or continuous scrambled 1s or 0s if the descrambler is enabled.

In QAM or DPSK Rx modem modes b2-0 of the Status Register contain a value indicative of the received signal BER, see Figure 11. In Rx FSK modem modes bits 2 and 1 will be zero and b0 will show the output of the frequency demodulator, updated at 8 times the nominal data rate.



Notes: 1. IRQ will go high only if the IRQ Mask bit b0 in the General Control Register is set. The IRQ bit is cleared by a read of the Status Register.
2. IRQN o/p will go low when IRQ bit high if IRQNEN bit of General Control Register is set

Figure 10b Operation of Status Register in DTMF Rx Mode

b3	b2	b1	b0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

Received DTMF Code: b3-0 of Status Register

Bit 14: This bit is the logical-OR of Line/Wakeup Event Register bits 0,1,2,3 & 8. It will go to 1 to indicate that a Line/Wakeup Event has occurred – this could be a Line Reversal/Ring Event, a WAKE pin Event, or a Line ADC Drop-out Event. The Regulated Supply and microcontroller will be powered-up (if not already) by such an event.

Bit 14 going to 1 can also produce an IRQ if the appropriate mask bits have been set – although this is only possible in the case where the Regulated Supply has not been de-powered since the setting of the mask bits.

The microcontroller is therefore made aware of the Line/Wakeup Event by being powered up or with an interrupt. Following this powerup/IRQ, the microcontroller should read the Status Register to clear any interrupt. It should then read the Line/Wakeup Event Register to determine which Line/Wakeup Event had occurred.

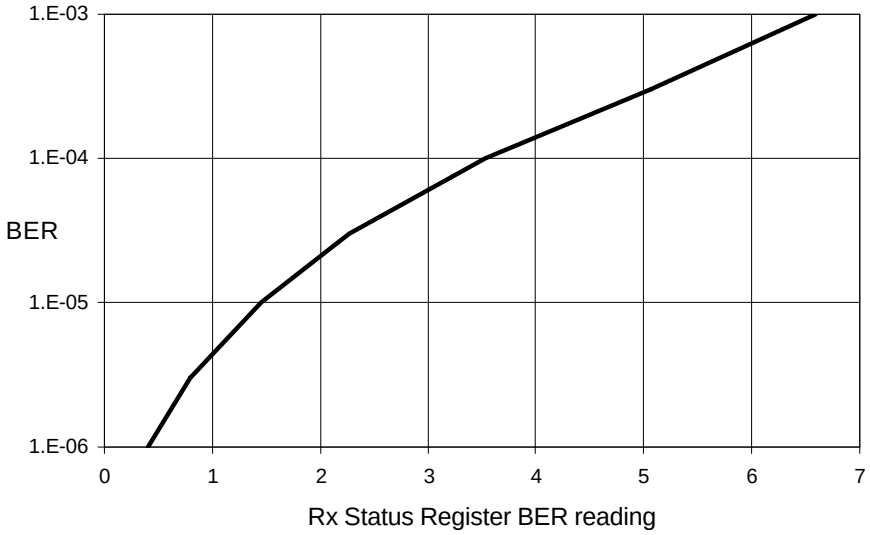


Figure 11 Typical Rx BER vs. Average Status Register BER Reading (b2-0)

1.5.12.14 Programming Register

Programming Register : 16-bit write-only. C-BUS address $E8

This register is used to program the transmit and receive programmed tone pairs by writing appropriate values to RAM locations within the CMX878. Note that these RAM locations are cleared by Powersave or Reset.

The Programming Register should only be written to when the Programming Flag bit (b13) of the Status Register is 1. The act of writing to the Programming Register clears the Programming Flag bit. When the programming action has been completed (normally within 150µs) the CMX878 will set the bit back to 1.

When programming Transmit or Receive Tone Pairs, do not change the Transmit or Receive Mode Registers until programming is complete and the Programming Flag bit has returned to 1.

Transmit Tone Pair Programming

4 transmit tone pairs (TA to TD) can be programmed.

The frequency (max 3.4kHz) and level must be entered for each tone to be used.

Single tones are programmed by setting both level and frequency values to zero for one of the pair.

Programming is done by writing a sequence of up to seventeen 16-bit words to the Programming Register.
The first word should be 32768 (8000 hex), the following 16-bit words set the frequencies and levels and are in the range 0 to 16383 (0-3FFF hex)

Word	Tone Pair	Value written
1		32768
2	TA	Tone 1 frequency
3	TA	Tone 1 level
4	TA	Tone 2 frequency
5	TA	Tone 2 level
6	TB	Tone 1 frequency
7	TB	Tone 1 level
- - -	- - -	- - - - - - - - - -
- - -	- - -	- - - - - - - - - -
16	TD	Tone 2 frequency
17	TD	Tone 2 level

The Frequency values to be entered are calculated from the formula:

Value to be entered = desired frequency (Hz) * 3.414

i.e. for 1kHz the value to be entered is 3414 (or 0D56 in Hex).

The Level values to be entered are calculated from the formula:

Value to be entered = desired Vrms * 93780 / V_{DD}

i.e. for 0.5Vrms at VDD = 3.0V, the value to be entered is 15630 (3D0E in Hex)

Note that allowance should be made for the transmit signal filtering in the CMX878 which attenuates the output signal for frequencies above 2kHz by 0.25dB at 2.5kHz, by 1dB at 3kHz and by 2.2dB at 3.4kHz.

On powerup or after a reset, the tone pairs TA-TC are set to notone, and TD set to generate 2130Hz + 2750Hz at approximately –20dBm each.

Receive Tone Pair Programming

The programmable tone pair detector is implemented as shown in Figure 12a. The filters are 4th order IIR sections. The frequency detectors measure the time taken for a programmable number of complete input signal cycles and compare this time against programmable upper and lower limits.

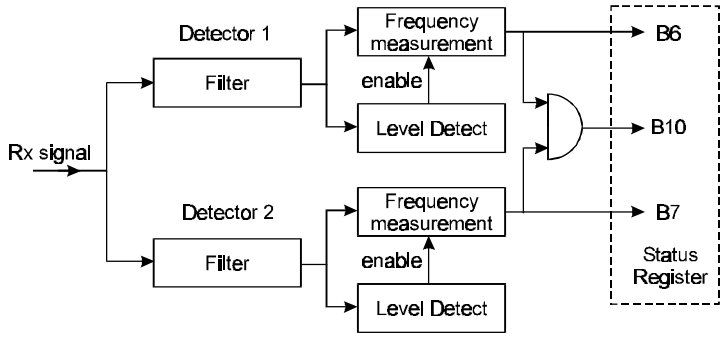


Figure 12a Programmable Tone Detectors

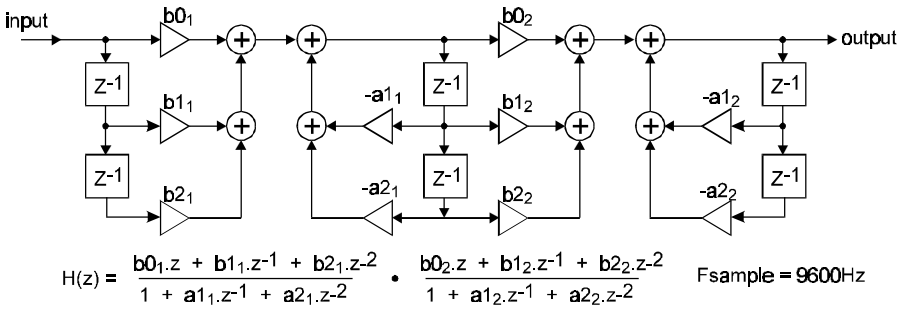


Figure 12b Filter Implementation

Programming is done by writing a sequence of twenty-seven 16-bit words to the Programming Register. The first word should be 32769 (8001 hex), the following twenty-six 16-bit words set the frequencies and levels and are in the range 0 to 32767 (0000-7FFF hex).

Word	Value written	Word	Value written
1	32769		
2	Filter #1 coefficient $b2_1$	15	Filter #2 coefficient $b2_1$
3	Filter #1 coefficient $b1_1$	16	Filter #2 coefficient $b1_1$
4	Filter #1 coefficient $b0_1$	17	Filter #2 coefficient $b0_1$
5	Filter #1 coefficient $a2_1$	18	Filter #2 coefficient $a2_1$
6	Filter #1 coefficient $a1_1$	19	Filter #2 coefficient $a1_1$
7	Filter #1 coefficient $b2_2$	20	Filter #2 coefficient $b2_2$
8	Filter #1 coefficient $b1_2$	21	Filter #2 coefficient $b1_2$
9	Filter #1 coefficient $b0_2$	22	Filter #2 coefficient $b0_2$
10	Filter #1 coefficient $a2_2$	23	Filter #2 coefficient $a2_2$
11	Filter #1 coefficient $a1_2$	24	Filter #2 coefficient $a1_2$
12	Freq measurement #1 ncycles	25	Freq measurement #2 ncycles
13	Freq measurement #1 mintime	26	Freq measurement #2 mintime
14	Freq measurement #1 maxtime	27	Freq measurement #2 maxtime

The coefficients are entered as 15-bit signed (two's complement) integer values (the most significant bit of the 16-bit word entered should be zero) calculated as 8192 * coefficient value from the user's filter design program (i.e. this allows for filter design values of -1.9999 to +1.9999).

The design of the IIR filters should make allowance for the fixed receive signal filtering in the CMX878 which has a low pass characteristic above 1.5kHz of 0.4dB at 2kHz, 1.2dB at 2.5kHz, 2.6dB at 3kHz and 4.1dB at 3.4kHz.

'ncycles' is the number of signal cycles for the frequency measurement.

'mintime' is the smallest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'mintime' = 9600 * ncycles / high frequency limit

'maxtime' is the highest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'maxtime' = 9600 * ncycles / low frequency limit

The level detectors include hysteresis. The threshold levels - measured on the line with unity gain filters, using the line interface circuit shown in Figure 4a, and with the Rx Gain Control block set to 0dB - are nominally:

'Off' to 'On' -44.5dBm
'On' to 'Off' -47.0dBm

Note that if any changes are made to the programmed values while the CMX878 is running in Programmed Tone Detect mode they will not take effect until the CMX878 is next switched into Programmed Tone Detect mode.

On a MODEM & TONES PROCESSOR BLOCK powerup or reset, the programmable tone pair detector is set to act as a simple 2130Hz + 2750Hz detector.

1.6 Application Notes

1.6.1 Controlling the Phone Line

The CMX878 needs to control the phone line in various operating states. The main states are summarised in the following table.

Mode of Operation	Explanation
On-hook, min. current	This is the On-hook or Standby state. The regulator is disabled and therefore also the microcontroller. Only the Standby circuits remain active. The device may have previously been primed for detection of a ring or line reversal event. It will also respond to a WAKE pin event.
On-hook, Regulator ON	In this state the regulated supply is active but the gyrator / off-hook current draw is disabled. There will be a current drawn from the line by the regulator, providing a 3.3V for the CMX878, the microcontroller and any additional application. The current taken will not be sufficient to take the line off-hook.
Off-hook taking line current (DC Mask)	This is the off-hook state when the line is in-use. The regulator and gyrator are enabled. Current will be drawn from the line to take the line off-hook. It will also present the correctly matched impedance to AC signals. The CMX878 can now be programmed to transmit and receive tones and modem signals. The line voltage can be monitored by the ADC.
Programmed Line Current Draw	In this state the regulator is enabled and will draw a small line current (regulator + microcontroller + active CMX878 circuitry). An additional line current draw can be set by controlling the level of the DAC. This feature can assist with characterising the line. Whilst progressively increasing the line current, measure the line voltage with the ADC and check for the presence of a Dial Tone with the Call Progress Detector. When Dial Tone is detected, store a representation of the line voltage in one of the Standby Supply registers. This knowledge of the line voltage at below which the line is off-hook can be used to determine if an extension has already seized the line.

The next table shows which circuits will need to be enabled.

Mode of Operation	Regulator Enabled?	Gyrator Enabled?	DAC Enabled?	ADC Enabled?
On-hook, min. current	N	N	N	N
On-hook, Regulator ON	Y	N	N	Y if want to measure line voltage
Off-hook on DC Mask	Y	Y	N	Y to detect an extension going off-hook
Programmed Line Current Draw	Y	N	Y	Y

Note that in order to use any of the MODEM & TONES PROCESSOR functions of the CMX878, bit 7 of the General Control Register ‘Pwr’ must also be set to 1 (otherwise the MODEM & TONES PROCESSOR will be powersaved).

1.6.2 Microcontroller Boot-up Routines

The microcontroller will normally be powered from the Regulated Supply. There are two main cases of when power will be applied to the microcontroller causing it to jump to the start point in its program:

i. When the application is first plugged into line power.
ii. When the sleeping CMX878 is woken by the detection of a Ring, Line Reversal or the WAKE input going high.

Both of these events will power up the regulated supply and the microcontroller must deal with both cases. The following is an example of a suitable routine:

(Microcontroller powers up, program starts)
1. Read CMX878 Status Register to clear any IRQ
2. Read Line/Wakeup Event Register
3. If Line/Wakeup Event Register Bit 5 is 0, a loss of Standby Supply had occurred making the contents of the Standby Supply Registers invalid; begin programming CMX878 registers from scratch, starting with the Configuration Register.
4. Otherwise, consider the remaining Line/Wakeup Event bits to check for a Line Reversal/Ring/WAKE input event – proceed accordingly.
5. Otherwise, read back the Configuration Register. General Purpose bits 5-15 * may hold a value representing a state which existed before the Regulated Supply failed then returned (e.g. the line was in an off-hook state, when the Central Office generated a temporary line break). If this is the case, proceed accordingly – perhaps returning to the previous state.

To take the line off-hook:

6. Define the state of the system by writing a code to the General Purpose * bits of the Configuration Register (these bits will survive a drop-out of the Regulated Supply).
7. Take the line off-hook by setting high the gyrator output bit in the Line Control Register.
8. The program can now proceed to power-up the MODEM & TONES PROCESSOR and associated circuits, starting with the programming of the General Control Register.

* Note that the Supplementary Standby Register can also be used to store a code.

In common with many embedded systems, it is recommended that precautions are taken to minimise the potential of the program crashing due to a software bug or a power supply disturbance. Watchdog timers and brown-out detectors can be employed to assist with this. It is recommended that following such a disturbance, a General Reset is issued to the CMX878 before proceeding to re-program it.

1.6.3 V.22bis Calling Modem Application

This section describes how the CMX878 can be used in a V.22bis Calling modem application, employing V.25 automatic answering and the V.22bis recommended handshake sequence. This attempts to establish a 2400bps connection but may fall back to 1200bps if the answering modem is not capable of 2400bps operation.

1. Ensure that the CMX878 is fully powered up. Set the Tx Mode Register to DTMF/Tones mode (set to ‘No Tone’ at this time), and the Rx Mode Register to Call Progress Detect mode.

2. Connect the line (go off hook) then dial the required number using the DTMF generator, monitoring for call progress signals (dial tone, busy, etc). Change to Answer Tone Detect mode.

3. On detection of the 2100Hz answer tone wait for it to end then wait for the 2225Hz answer tone detector to respond. (The '2225Hz' answer tone detector will recognise unscrambled binary 1s at 1200bps High Band as well as 2225Hz). When unscrambled binary 1s or 2225Hz have been received for 155ms set a 456ms timer.

4. When the 456ms timer expires check that the 2225Hz or unscrambled 1s is still being received, then set the Tx Mode Register for V.22 1200bps Low Band transmission of S1 signal and set a 100ms timer. Also set the Rx Mode register to V.22 1200bps High Band receive, descrambler enabled and Rx USART disabled.

5. When the 100ms timer expires set the Tx Mode Register for V.22 1200bps Low Band transmission of scrambled 1s (continuous 1s with the scrambler enabled) and look for received S1 signal.

6. If the S1 signal is not detected within 270ms then go to step 14 as the answering modem is not capable of 2400bps operation.

7. If S1 signal is detected wait for it to end then set a 450ms timer.

8. When the 450ms timer expires set the Rx Mode Register to V.22bis 2400bps High Band (this will begin 16-way decisions) with the auto-equaliser and descrambler enabled. Start to monitor for Rx scrambled 1s. Set a 150ms timer.

9. Once 32 consecutive bits of received scrambled 1s at 2400bps have been detected, enable the Rx USART.

10. When the 150ms timer expires set the Tx Mode Register for V.22bis 2400bps scrambled 1s, set a 200ms timer.

11. Load the Tx Data Register with the first data to be transmitted.

12. When the 200ms timer expires set the Tx Mode Register for Start-Stop or Synchronous transmission of data from the Tx Data Buffer. This will start transmission of the data loaded in step 11.

13. A 2400bps data connection has now been established.

14. If the S1 signal had not been detected within 270ms after step 5 then monitor for scrambled 1s at 1200bps.

15. When scrambled 1s (at 1200bps) have been received for 270ms enable the Rx USART, set a 765ms timer and load the Tx Data Register with the first data to be transmitted.

16. When the timer expires set the Tx Mode Register for Start-Stop or Synchronous transmission of data from the Tx Data Buffer. This will start transmission of the data loaded in step 15.

17. A 1200bps data connection has now been established.

1.6.4 V.22bis Answering Modem Application

This section describes how the CMX878 can be used in a V.22bis Answering modem application, employing V.25 automatic answering and the V.22bis recommended handshake sequence. A 1200 or 2400 bps connection will be established depending on the signals received from the calling modem.

1. It is assumed that the CMX878 has powered up the regulator after detecting a ringing signal. The microcontroller confirms this by reading the Line/Wakeup Event Register. It then powers up the xtal and MODEM & TONES PROCESSOR circuits.

2. Connect the line (go off hook), set a 2150ms timer and power up the CMX878, setting the Tx Mode Register to DTMF/Tones mode (set for 'no tone' at this time) and the Rx Mode Register to V.22 1200bps Low Band receive, descrambler enabled, Rx USART disabled.

3. When the 2150ms timer expires set the Tx Mode Register to transmit the 2100Hz answer tone and set a 3300ms timer.

4. When the 3300ms timer expires set the Tx Mode Register to no tone and set a 75ms timer.

5. When the 75ms timer expires set the Tx Mode Register for V.22 High Band 1200bps transmission of unscrambled 1s. Monitor the received signal for the S1 signal or scrambled 1s.

6. If scrambled 1s are detected for 270ms go to step 15.

7. If the S1 signal is received wait for it to end then set the Tx Mode Register for V.22 High Band 1200bps transmission of the S1 signal and set a 100ms timer.

8. When the 100ms timer expires set the Tx Mode Register for V.22 High Band 1200bps transmission of scrambled 1s and set a 350ms timer.

9. When the 350ms timer expires set the Rx Mode Register for V.22bis Low Band 2400bps receive (this will begin 16-way decisions) with the auto-equaliser and descrambler enabled and the Rx USART disabled, set a 150ms timer and start to monitor for Rx scrambled 1s.

10. When the 150ms timer expires set the Tx Mode Register for V.22bis High Band 2400bps transmission of scrambled 1s and set a 200ms timer.

11. Load the Tx Data Buffer with the first data to be transmitted.

12. Once 32 consecutive bits of received scrambled 1s at 2400bps have been detected, enable the Rx USART.

13. When the 200ms timer expires set the Tx Mode Register for Start-Stop or Synchronous transmission of data from the Tx Data Buffer. This will start transmission of the data loaded in step 11.

14. A 2400bps data connection has now been established.

15. If scrambled 1s had been detected for 270ms in step 6, set the Tx Mode Register to V.22 High Band 1200bps scrambled 1s transmission and set a 765ms timer and enable the Rx USART.

16. Load the Tx Data Buffer with the first data to be transmitted.

17. When the 765ms timer expires set the Tx Mode Register for Start-Stop or Synchronous transmission of data from the Tx Data Buffer. This will start transmission of the data loaded in step 16.

18. A 1200bps data connection has now been established.

1.7 Performance Specification

1.7.1 Electrical Performance

1.7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Notes	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}) or (DV_{DD} - DV_{SS})	i	-0.3	7.0	V
Voltage on any pin to ground	i, ii	-0.3	AV_{DD} + 0.3	V
Voltage on WAKE, RD, RT, VFB and REGENAB pins to ground	i, iii	-0.3	$SBYV_{DD}$ + 0.3	V
Current into or out of V_{DD} and V_{SS} pins		-50	+50	mA
Current into or out of any other pin		-20	+20	mA

Notes:
i. The negative supply rails AV_{SS} and DV_{SS} ('ground') are electrically connected on-chip and therefore must not have different potentials applied to them. They should also be connected together externally, having regard to the recommended grounding techniques described in Section 1.4. $AV_{DD} \approx DV_{DD}$.
ii. Excludes pins which are connected to the Standby Supply (i.e. $SBYV_{DD}$, WAKE, RD, RT, VFB and REGENAB).
iii. It is possible that during the peaks of large ringing signals, the voltage at the RD pin could exceed $SBYV_{DD}$ + 0.3V. This is acceptable because on-chip diode clamps will limit the voltage to approximately $SBYV_{DD}$ + 0.7V and high value resistors should be employed in the external circuit to limit the current.

	Min.	Max.	Units
Total Allowable Power Dissipation at Tamb = 25°C			
D1 package		800	mW
D6 package		550	mW
E1 package		400	mW
... Derating			
D1 package		13	mW/°C
D6 package		9	mW/°C
E1 package		5.3	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

1.7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (AV_{DD} - V_{SS}) or (DV_{DD} - DV_{SS})	iv	2.7	5.5	V
Operating Temperature		-40	+85	°C

Notes:
iv. The circuit shown in Figure 4a will give a regulated supply of nominally 3.3V which is within the specified range.

1.7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
AV_{DD} = 3.3V. Circuit as in Figure 4a. Line Voltage = 50V DC.
CMX878 operational temp. range = -40 to +85°C.
Xtal Frequency = 11.0592 or 12.288MHz ± 0.01% (100ppm). 0dBm corresponds to 775mVrms.

DC Parameters	Notes	Min.	Typ.	Max.	Units
Regulated Supply at AV_{DD} (regulator on)	1a	3.1	3.3	3.5	V
Standby Supply at $SBYV_{DD}$ (regulator off)	1a, 1b	2.9	3.4	3.9	V
On-hook Supply Current from Line (regulator off)	1a	-	6.7	10	µA
Regulated Supply Current from Line (regulator on, all other functions powersaved, no other load)	1a	-	1.0	1.4	mA
Currents into the device via I_{DD} = AV_{DD} + DV_{DD} currents with regulator running at 3.3V :					
I_{DD} (MODEM Powersaved, i.e. 'Pwr' bit =0)	1c, 2	-	100	130	µA
I_{DD} (MODEM Reset but not powersaved)	1c, 3	-	2.0	3.0	mA
I_{DD} (MODEM Running)	1c	-	3.5	5.5	mA
I_{DD} (DAC and ADC only running)	1c	-	1.0	2.0	mA
Logic '1' Input Level	4	70%	-	-	DV_{DD}
Logic '0' Input Level	4	-	-	30%	DV_{DD}
Logic Input Leakage Current (Vin = 0 to V_{DD}), (excluding XTAL/CLOCK input)		-1.0	-	+1.0	µA
Output Logic '1' Level (I_{OH} = 2 mA)		80%	-	-	DV_{DD}
Output Logic '0' Level (I_{OL} = -3 mA)		-	-	0.4	V
IRQN O/P 'Off' State Current (Vout = V_{DD})		-	-	1.0	µA
RD and RT pin Schmitt trigger input high-going threshold (Vthi) (see Figure 13)		0.56 x $SBYV_{DD}$	-	0.56 x $SBYV_{DD}$ + 0.6V	V
RD and RT pin Schmitt trigger input low-going threshold (Vtlo) (see Figure 13)		0.44 x $SBYV_{DD}$ - 0.6V	-	0.44 x $SBYV_{DD}$	V

Notes:
1a. With the application circuit at Tamb = 0 to 40°C.
1b. With the regulator on and the gyrator on (line off-hook) the minimum value for $SBYV_{DD}$ will be AV_{DD} – D6 diode drop.
1c. At 25°C, not including any current drawn from the CMX878 pins by external circuitry other than X1, C1 and C2. 'MODEM' means the MODEM & TONES PROCESSOR block.
2. All logic inputs at V_{SS} except for RT and CSN inputs which are at V_{DD}.
3. General Mode Register b8 and b7 both set to 1.
4. Excluding RD, RT and WAKE pins.

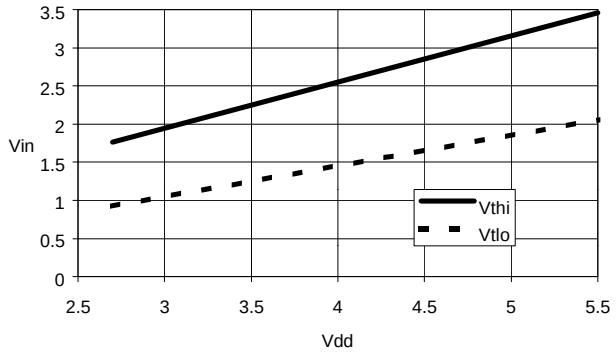


Figure 13 Typical Schmitt Trigger Input Voltage Thresholds vs. $SBYV_{DD}$

XTAL/CLOCK Input (timings for an external clock input)	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
'High' Pulse Width		30	-	-	ns
'Low' Pulse Width		30	-	-	ns

Transmit QAM and DPSK Modes (V.22, Bell 212A, V.22bis)	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Carrier frequency, high band	5	-	2400	-	Hz
Carrier frequency, low band	5	-	1200	-	Hz
Baud rate	6	-	600	-	Baud
Bit rate (V.22, Bell 212A)	6	-	1200/600	-	bps
Bit rate (V.22bis)	6	-	2400	-	bps
550Hz guard tone frequency		548	550	552	Hz
550Hz guard tone level wrt data signal		-4.0	-3.0	-2.0	dB
1800Hz guard tone frequency		1797	1800	1803	Hz
1800Hz guard tone level wrt data signal		-7.0	-6.0	-5.0	dB

Transmit V.21 FSK Mode	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Baud rate	6	-	300	-	Baud
Mark (logical 1) frequency, high band		1647	1650	1653	Hz
Space (logical 0) frequency, high band		1847	1850	1853	Hz
Mark (logical 1) frequency, low band		978	980	982	Hz
Space (logical 0) frequency, low band		1178	1180	1182	Hz

Transmit Bell 103 FSK Mode	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Baud rate	6	-	300	-	Baud
Mark (logical 1) frequency, high band		2222	2225	2228	Hz
Space (logical 0) frequency, high band		2022	2025	2028	Hz
Mark (logical 1) frequency, low band		1268	1270	1272	Hz
Space (logical 0) frequency, low band		1068	1070	1072	Hz

Transmit V.23 FSK Mode	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Baud rate	6	-	1200/75	-	Baud
Mark (logical 1) frequency, 1200 baud		1298	1300	1302	Hz
Space (logical 0) frequency, 1200 baud		2097	2100	2103	Hz
Mark (logical 1) frequency, 75 baud		389	390	391	Hz
Space (logical 0) frequency, 75 baud		449	450	451	Hz

Transmit Bell 202 FSK Mode	Notes	Min.	Typ.	Max.	Units
Baud rate	6	-	1200/150	-	Baud
Mark (logical 1) frequency, 1200 baud		1198	1200	1202	Hz
Space (logical 0) frequency, 1200 baud		2197	2200	2203	Hz
Mark (logical 1) frequency, 150 baud		386	387	388	Hz
Space (logical 0) frequency, 150 baud		486	487	488	Hz

DTMF/Single Tone Transmit	Notes	Min.	Typ.	Max.	Units
Tone frequency accuracy		-0.2	-	+0.2	%
Distortion	7	-	1.0	2.0	%

Transmit Output Level	Notes	Min.	Typ.	Max.	Units
Modem and Single Tone modes	7	-11.0	-10.0	-9.0	dBm
DTMF mode, Low Group tones	7	-9.0	-8.0	-7.0	dBm
DTMF: level of High Group tones wrt Low Group	7	+1.0	+2.0	+3.0	dB
Tx output buffer gain control accuracy	7	-0.25	-	+0.25	dB

Notes: 5. % carrier frequency accuracy is the same as XTAL/CLOCK % frequency accuracy.

6 Tx signal % baud or bit rate accuracy is the same as XTAL/CLOCK % frequency accuracy.

7. Measured on a matched line with Tx Level Control gain set to 0dB, at A V_{DD} = 3.3V (levels are proportional to V_{DD}). Level measurements for all modem modes are performed with random transmitted data and without any guard tone. 0dBm = 775mVrms.

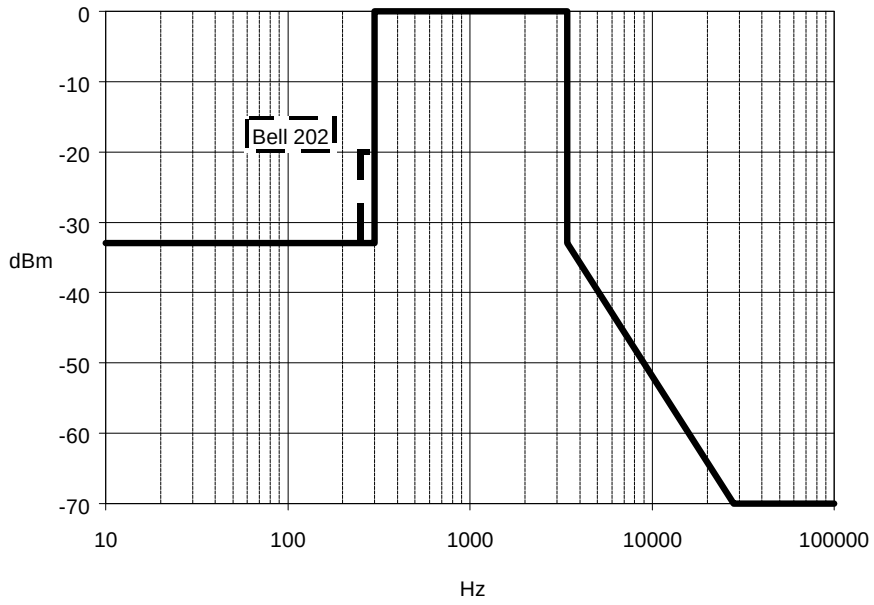


Figure 14 Maximum Out of Band Tx Line Energy Limits (see note 8)

Notes: 8. Measured on the line with the Tx line signal level set to -10dBm for QAM, DPSK, FSK or single tones, -6dBm and -8dBm for DTMF tones. Excludes any distortion due to external components.

Receive QAM and DPSK Modes (V.22, Bell 212A, V.22bis)	Notes	Min.	Typ.	Max.	Units
Carrier frequency (high band)		2392	2400	2408	Hz
Carrier frequency (low band)		1192	1200	1208	Hz
Baud rate	9	-	600	-	Baud
Bit rate (V.22, Bell 212A)	9	-	1200/600	-	bps
Bit rate (V.22bis)	9	-	2400	-	bps

Notes: 9. These are the bit and baud rates of the line signal, the acceptable tolerance is ±0.01%.

Receive V.21 FSK Mode	Notes	Min.	Typ.	Max.	Units
Acceptable baud rate		297	300	303	Baud
Mark (logical 1) frequency, high band		1638	1650	1662	Hz
Space (logical 0) frequency, high band		1838	1850	1862	Hz
Mark (logical 1) frequency, low band		968	980	992	Hz
Space (logical 0) frequency, low band		1168	1180	1192	Hz

Receive Bell 103 FSK Mode	Notes	Min.	Typ.	Max.	Units
Acceptable baud rate		297	300	303	Baud
Mark (logical 1) frequency, high band		2213	2225	2237	Hz
Space (logical 0) frequency, high band		2013	2025	2037	Hz
Mark (logical 1) frequency, low band		1258	1270	1282	Hz
Space (logical 0) frequency, low band		1058	1070	1082	Hz

Receive V.23 FSK Mode	Notes	Min.	Typ.	Max.	Units
1200 baud					
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1280	1300	1320	Hz
Space (logical 0) frequency		2080	2100	2120	Hz
75 baud					
Acceptable baud rate		74	75	76	Baud
Mark (logical 1) frequency		382	390	398	Hz
Space (logical 0) frequency		442	450	458	Hz

Receive Bell 202 FSK Mode	Notes	Min.	Typ.	Max.	Units
1200 baud					
Acceptable baud rate		1188	1200	1212	Baud
Mark (logical 1) frequency		1180	1200	1220	Hz
Space (logical 0) frequency		2180	2200	2220	Hz
150 baud					
Acceptable baud rate		148	150	152	Baud
Mark (logical 1) frequency		377	387	397	Hz
Space (logical 0) frequency		477	487	497	Hz

Rx Modem Signal (FSK, DPSK and QAM Modes)	Notes	Min.	Typ.	Max.	Units
Signal level	10	-45	-	-9	dBm
Signal to Noise Ratio (noise flat 300-3400Hz)		20	-	-	dB

Rx Modem S1 Pattern Detector (DPSK and QAM modes)	Notes	Min.	Typ.	Max.	Units
Will detect S1 pattern lasting for		90.0	-	-	ms
Will not detect S1 pattern lasting for				72.0	
Hold time (minimum detector 'On' time)		5.0	-	-	ms

Rx Modem Energy Detector	Notes	Min.	Typ.	Max.	Units
Detect threshold ('Off' to 'On)	10,11	-	-	-43.0	dBm
Undetect threshold ('On' to 'Off')	10,11	-48.0	-	-	dBm
Hysteresis	10,11	2.0	-	-	dB
Detect ('Off' to 'On') response time					
QAM and DPSK modes	10,11	10.0	-	35.0	ms
300 and 1200 baud FSK modes	10,11	8.0	-	30.0	ms
150 and 75 baud FSK modes	10,11	16.0	-	60.0	ms
Undetect ('On' to 'Off') response time					
QAM and DPSK modes	10,11	10.0	-	55.0	ms
300 and 1200 baud FSK modes	10,11	10.0	-	40.0	ms
150 and 75 baud FSK modes	10,11	20.0	-	80.0	ms

Rx Answer Tone Detectors	Notes	Min.	Typ.	Max.	Units
Detect threshold ('Off' to 'On)	10,12	-	-	-43.0	dBm
Undetect threshold ('On' to 'Off')	10,12	-48.0	-	-	dBm
Detect ('Off' to 'On') response time	10,12	30.0	33.0	45.0	ms
Undetect ('On' to 'Off') response time	10,12	7.0	18.0	25.0	ms
2100Hz detector					
'Will detect' frequency		2050	-	2160	Hz
'Will not detect' frequency		-	-	2000	Hz
2225Hz detector					
'Will detect' frequency		2160	-	2285	Hz
'Will not detect' frequency		2335	-	-	Hz

Rx Call Progress Energy Detector	Notes	Min.	Typ.	Max.	Units
Bandwidth (-3dB points) See Figure 7a		275	-	665	Hz
Detect threshold ('Off' to 'On)	10,13	-	-	-37.0	dBm
Undetect threshold ('On' to 'Off')	10,13	-42.0	-	-	dBm
Detect ('Off' to 'On') response time	10,13	30.0	36.0	45.0	ms
Undetect ('On' to 'Off') response time	10,13	6.0	8.0	50.0	ms

Notes:
10. Gain Control block set to 0dB
11. Thresholds and times measured with random data for QAM and DPSK modes, continuous binary '1' for all FSK modes. Fixed compromise line equaliser enabled. Signal switched between off and -33dBm
12. 'Typical' value refers to 2100Hz or 2225Hz signal switched between off and -33dBm. Times measured wrt. received line signal
13. 'Typical' values refers to 400Hz signal switched between off and -33dBm

DTMF Decoder	Notes	Min.	Typ.	Max.	Unit
Valid input signal levels (each tone of composite signal)	10	-30.0	-	0.0	dBm
Not decode level (either tone of composite signal)	10	-	-	-36.0	dBm
Twist = High Tone/Low Tone		-10.0	-	6.0	dB
Frequency Detect Bandwidth		±1.8	-	-	%
Frequency Not Detect Bandwidth		-	-	±3.5	%
Max level of low frequency noise (i.e. dial tone)					
Interfering signal frequency <= 550Hz	14	-	-	0.0	dB
Interfering signal frequency <= 450Hz	14	-	-	10.0	dB
Interfering signal frequency <= 200Hz	14	-	-	20.0	dB
Max. noise level wrt. signal	14,15	-	-	-10.0	dB
DTMF detect response time		-	-	40.0	ms
DTMF de-response time		-	-	30.0	ms
Status Register b5 high time		14.0	-	-	ms
'Will Detect' DTMF signal duration		40.0	-	-	ms
'Will Not Detect' DTMF signal duration		-	25.0	-	ms
Pause length detected		30.0	-	-	ms
Pause length ignored		-	-	15.0	ms

Notes: 14. Referenced to DTMF tone of lower amplitude.
15 Flat Gaussian Noise in 300-3400Hz band.

Receive Input Amplifier	Notes	Min.	Typ.	Max.	Units
Input impedance (at 100Hz)		10.0			Mohm
Open loop gain (at 100Hz)			10000		V/V
Rx Gain Control Block accuracy		-0.25		+0.25	dB

C-BUS Timings (See Figure 15)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN-Enable to Clock-High time		100	-	-	ns
t_{CSH}	Last Clock-High to CSN-High time		100	-	-	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	-	-	ns
t_{HIZ}	CSN-High to Reply Output 3-state time		-	-	1.0	µs
t_{CSOFF}	CSN-High Time between transactions		1.0	-	-	µs
t_{NXT}	Inter-Byte Time		200	-	-	ns
t_{CK}	Clock-Cycle time		200	-	-	ns
t_{CH}	Serial Clock-High time		100	-	-	ns
t_{CL}	Serial Clock-Low time		100	-	-	ns
t_{CDS}	Command Data Set-Up time		75.0	-	-	ns
t_{CDH}	Command Data Hold time		25.0	-	-	ns
t_{RDS}	Reply Data Set-Up time		50.0	-	-	ns
t_{RDH}	Reply Data Hold time		0.0	-	-	ns

Maximum 30pF load on each C-BUS interface line.

Note: These timings are for the latest version of the C-BUS as embodied in the CMX878, and allow faster transfers than the original C-BUS timings given in CML Publication D/800/Sys/3 July 1994.

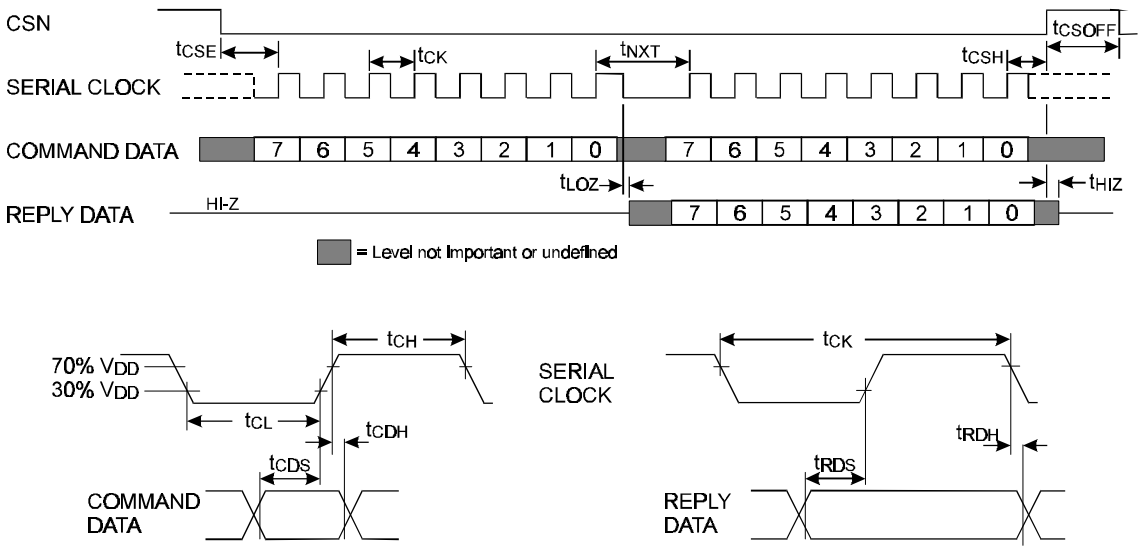
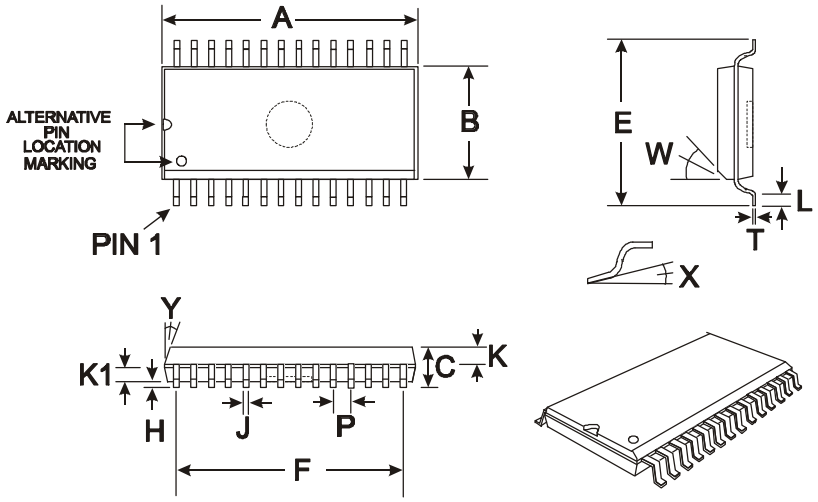


Figure 15 C-BUS Timing

1.7.2 Packaging



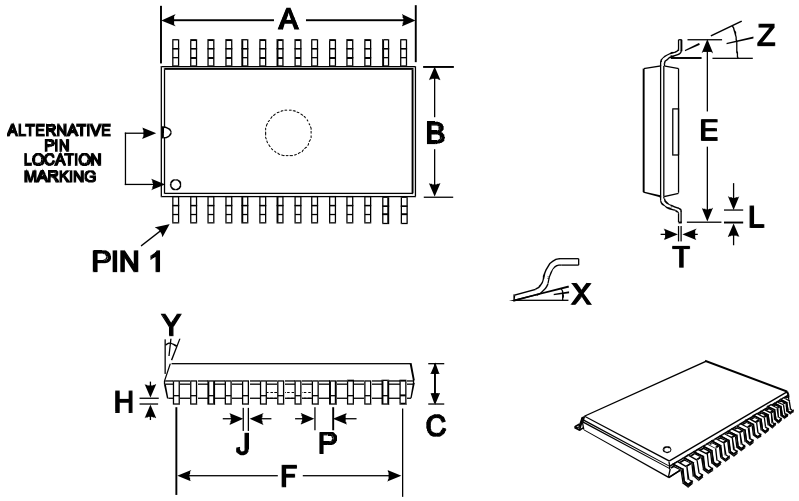
	DIM.	MIN.	TYP.	MAX.
*	A	0.697 (17.70)		0.711 (18.06)
*	B	0.286 (7.26)		0.299 (7.59)
	C	0.088 (2.24)		0.105 (2.67)
	E	0.390 (9.90)		0.419 (10.64)
	F		0.650 (16.51)	
	H	0.003 (0.08)		0.020 (0.51)
	J	0.013 (0.33)		0.018 (0.46)
	K		0.041 (1.04)	
	K1		0.041 (1.04)	
	L	0.016 (0.41)		0.050 (1.27)
	P		0.050 (1.27)	
	T	0.009 (0.23)		0.0125 (0.32)
	W		45°	
	X	0°		10°
	Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 16 28-pin SOIC (D1) Mechanical Outline: *Order as part no. CMX878D1*



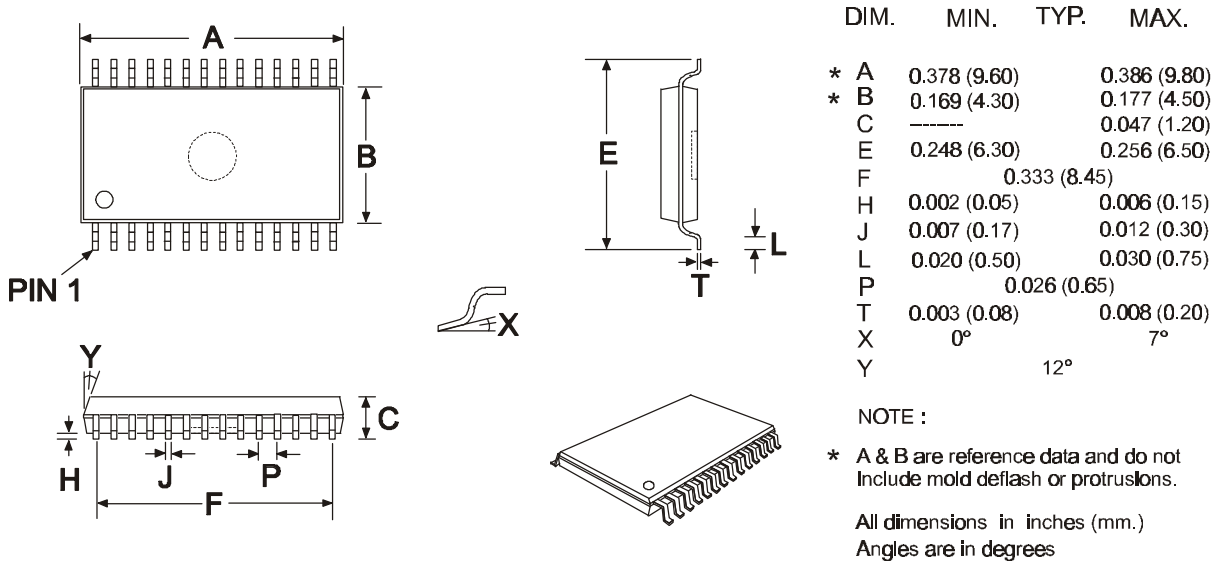
	DIM.	MIN.	TYP.	MAX.
*	A	0.396 (10.06)		0.407 (10.34)
*	B	0.205 (5.21)		0.213 (5.39)
	C	0.066 (1.67)		0.079 (2.00)
	E	0.301 (7.65)		0.312 (7.90)
	F		0.333 (8.45)	
	H	0.002 (0.05)		0.008 (0.21)
	J	0.010 (0.25)		0.015 (0.38)
	L	0.022 (0.56)		0.037 (0.94)
	P		0.026 (0.65)	
	T	0.005 (0.13)		0.009 (0.23)
	X	0°		8°
	Y	7°		9°
	Z	4°		10°

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 17 28-pin SSOP (D6) Mechanical Outline: *Order as part no. CMX878D6*



DIM.	MIN.	TYP.	MAX.
* A	0.378 (9.60)		0.386 (9.80)
* B	0.169 (4.30)		0.177 (4.50)
C	------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
F		0.333 (8.45)	
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.026 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
X	0°		7°
Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 18 28-pin TSSOP (E1) Mechanical Outline: *Order as part no. CMX878E1*

Handling precautions: This product includes input protection, however, precautions should be taken to prevent device damage from electro-static discharge. CML does not assume any responsibility for the use of any circuitry described. No IPR or circuit patent licences are implied. CML reserves the right at any time without notice to change the said circuitry and this product specification. CML has a policy of testing every product shipped using calibrated test equipment to ensure compliance with this product specification. Specific testing of all circuit parameters is not necessarily performed.

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