

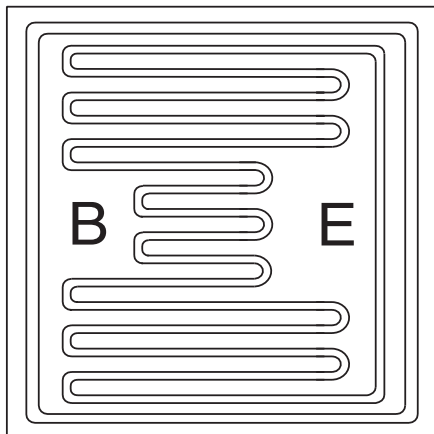
**PROCESS CP314**  
**Small Signal Transistor**  
NPN - High Current Transistor Chip

**Central**<sup>TM</sup>  
**Semiconductor Corp.**

**PROCESS DETAILS**

Process	EPITAXIAL PLANAR
Die Size	40 x 40 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	7.9 x 8.7 MILS
Emitter Bonding Pad Area	9.0 x 14 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

**GEOMETRY**



BACKSIDE COLLECTOR R0

**GROSS DIE PER 4 INCH WAFER**

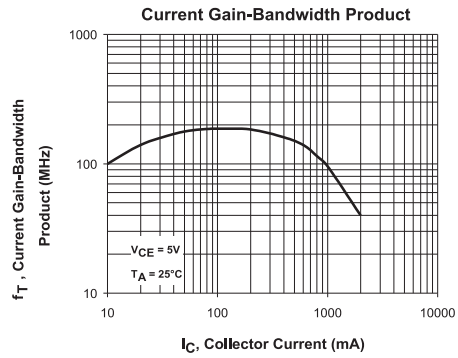
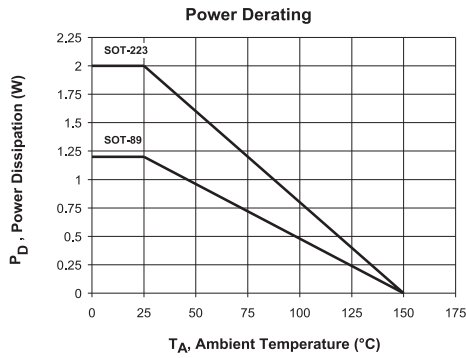
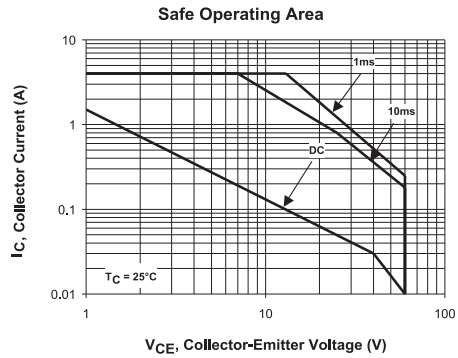
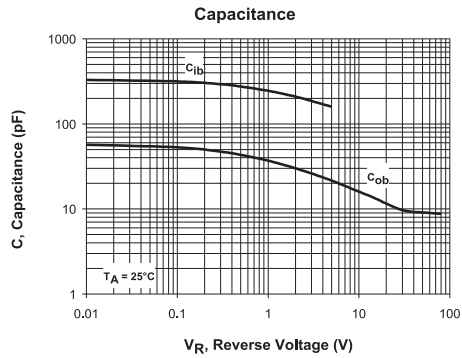
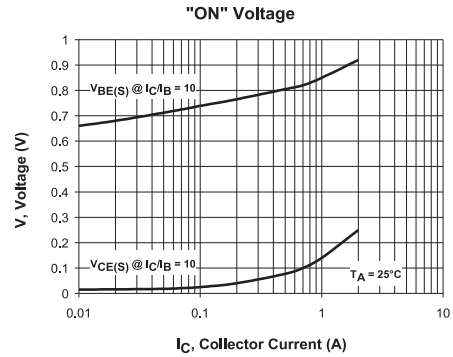
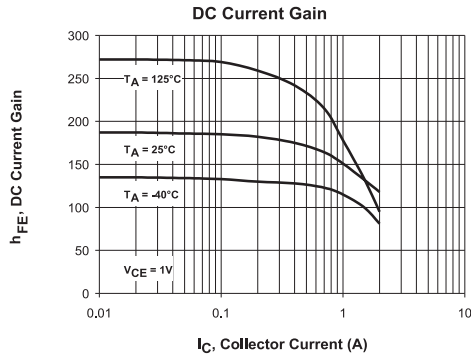
7,070

**PRINCIPAL DEVICE TYPES**

CBCP68  
CBCX68  
CZT651  
MPS650  
MPS651

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R2 (1-August 2002)



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