Central™
Semiconductor Corp.

PROCESS CP329V

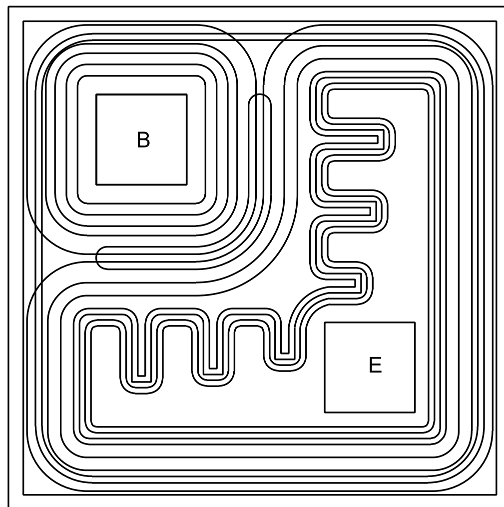
Small Signal Transistor

NPN- Silicon Darlington Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	27 x 27 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	4.2 x 4.2 MILS
Emitter Bonding Pad Area	4.3 x 4.3 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 13,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 4 INCH WAFER
15,980

PRINCIPAL DEVICE TYPES
CMPTA29
CZTA29
MPSA29

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

R0 (20 -January 2006)