SONY

CXA3252N

All Band TV Tuner IC with On-chip PLL

Description

The CXA3252N is a monolithic TV tuner IC which integrates local oscillator and mixer circuits for VHF band, local oscillator and mixer circuits for UHF band, an IF amplifier and a tuning PLL onto a single chip, enabling further miniaturization of the tuner.

Features

- Superior cross modulation
- Supports both IF double-tuned filter and adjacent channel trap.
- Balanced UHF oscillator (4 pins) with excellent oscillation stability
- Supports both I²C and 3-wire bus modes
- Automatic identification of 18, 19 or 27-bit control (during 3-wire bus mode)
- On-chip high voltage drive transistor for charge pump
- Reference frequency selectable from 31.25, 50 or 62.5 kHz (when using a 4 MHz crystal)
- Low-phase noise synthesizer
- On-chip 4-output band switch (supports output voltages from 5 to 9 V)
- 32 pin SSOP

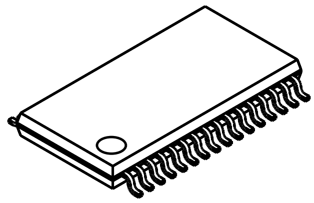
Applications

- TV tuners
- VCR tuners
- CATV tuners

Structure

Bipolar silicon monolithic IC

32 pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	$V_{CC}1$, $V_{CC}2$	–0.3 to + 5.5	V
	$V_{CC}3$	–0.3 to +10.0	V
• Storage temperature	Tstg	–55 to + 150	°C
• Allowable power dissipation			

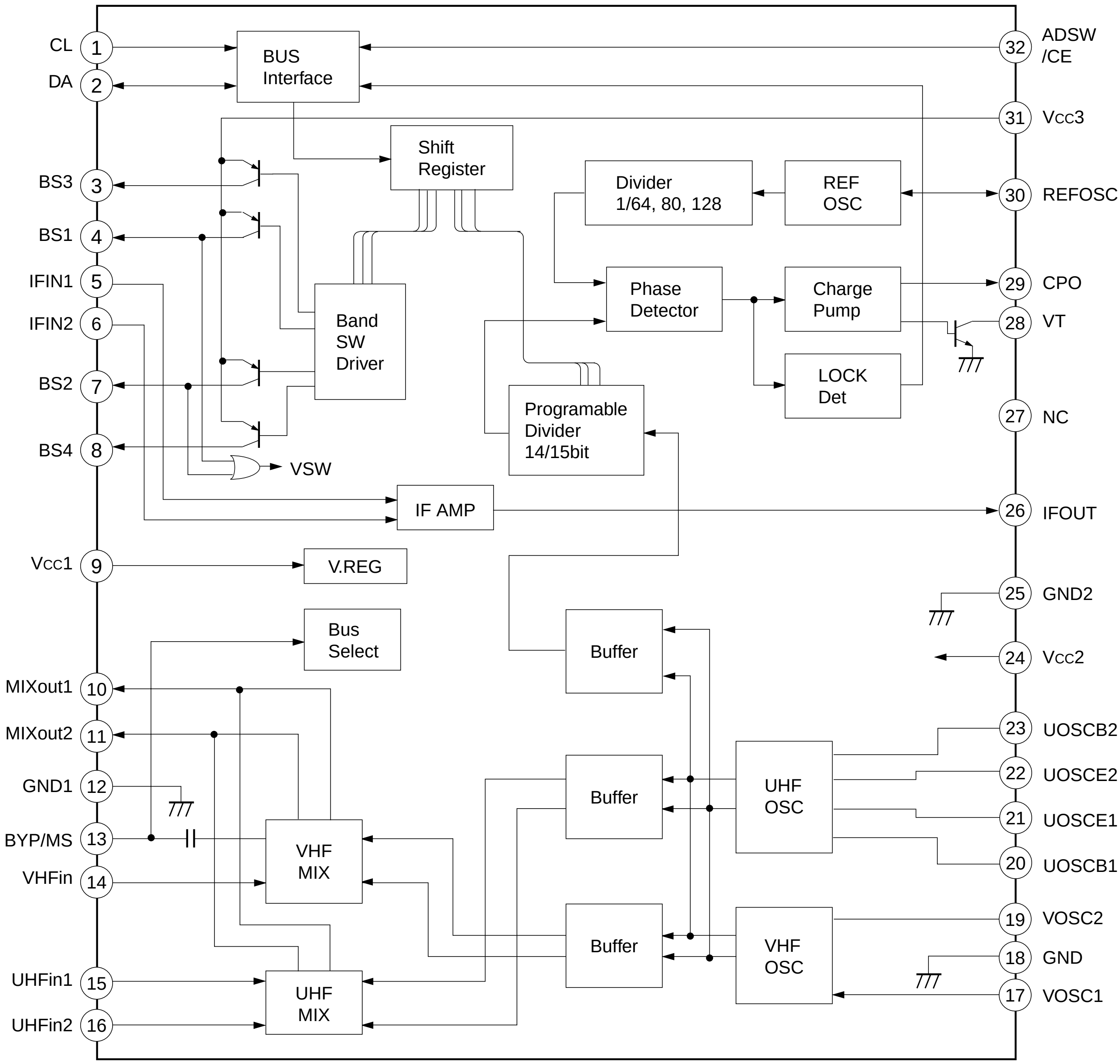
Operating Conditions

• Supply voltage	$V_{CC}1$, $V_{CC}2$	4.75 to 5.30	V
	$V_{CC}3$	4.75 to 9.45	V
• Operating temperature	Topr	–25 to +75	°C
	P_D	580	mW

(when mounted on a printed circuit board)

This IC has the pins whose electrostatic discharge strength is weak as the operating frequency is high and the high-frequency process is used for this IC.
Take care of handling the IC.

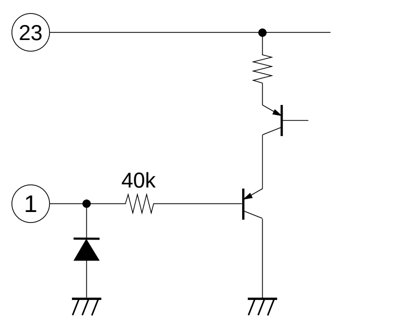
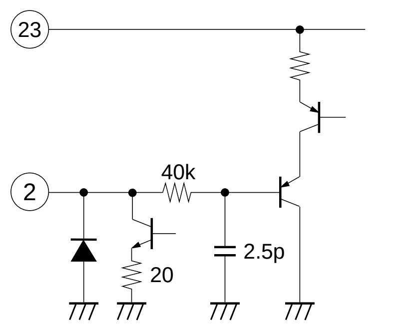
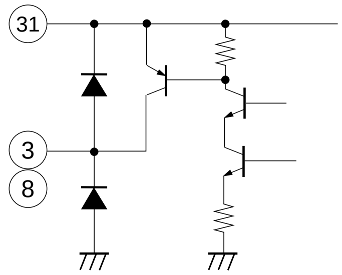
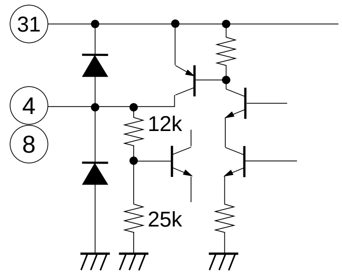
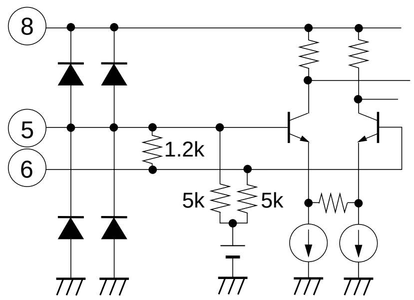
Block Diagram and Pin Configuration

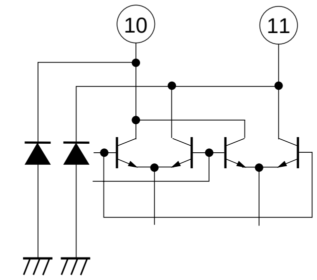
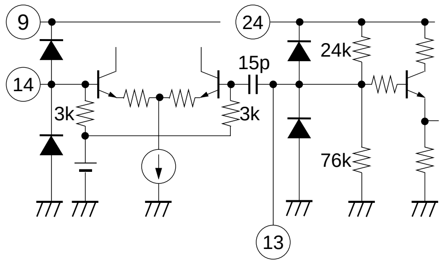
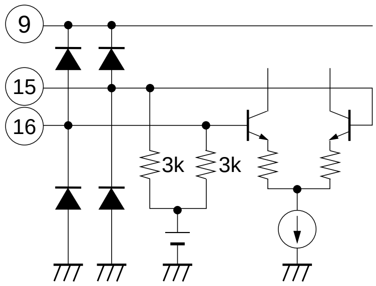
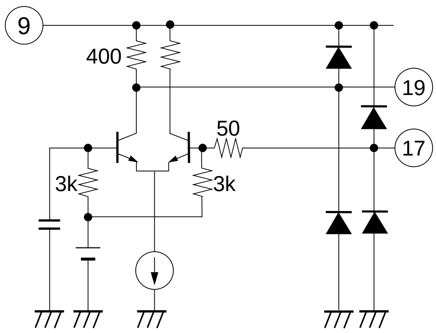


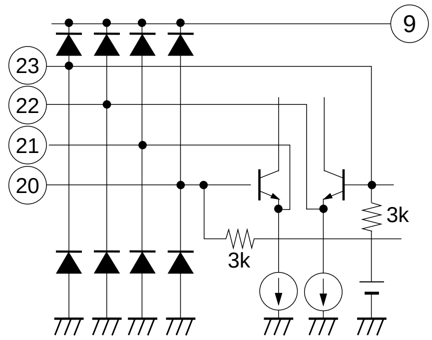
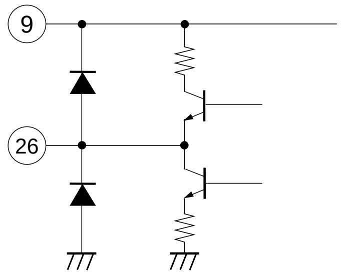
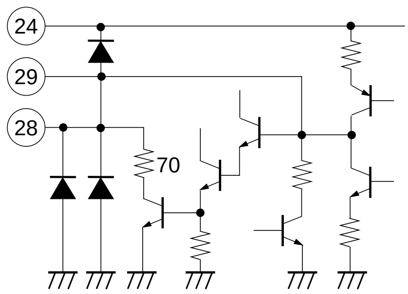
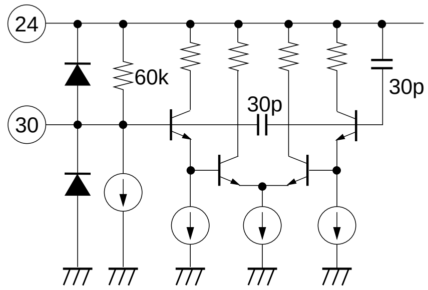
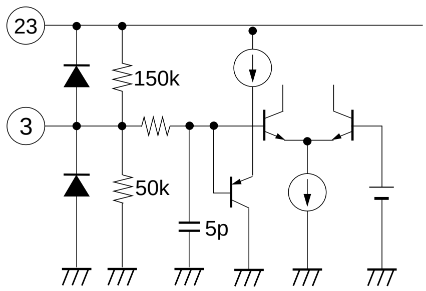
Pin Description

Pin No.	Symbol	Description
1	CL	CLOCK/SCL (I^2C bus)
2	DA	DATA/SDA (I^2C bus)
3	BS3	Band switch output 3
4	BS1	Band switch output 1 (VHF low band)
5	IFIN1	IF amplifier input 1
6	IFIN2	IF amplifier input 2
7	BS2	Band switch output 2 (VHF high band)
8	BS4	Band switch output 4
9	VCC1	Analog circuit Vcc
10	MIXOUT1	MIX output (open collector)
11	MIXOUT2	MIX output (open collector)
12	GND1	Analog circuit GND
13	BYP/MS	VHF input GND and control bus switching
14	VHFIN	VHF input
15	UHFIN1	UHF input
16	UHFIN2	UHF input
17	VOSC1	VHF oscillator (base input)
18	GND	GND
19	VOSC2	VHF oscillator (collector output)
20	UOSCB1	UHF oscillator (base pin)
21	UOSCE1	UHF oscillator (emitter pin)
22	UOSCE2	UHF oscillator (emitter pin)
23	UOSCB2	UHF oscillator (base pin)
24	VCC2	PLL circuit Vcc
25	GND2	PLL circuit GND
26	IFOUT	IF amplifier output
27	NC	OPEN
28	VT	Tuning voltage output (open collector)
29	CPO	Charge pump output (loop filter connection)
30	REFOSC	Crystal connection
31	VCC3	Band switch power supply
32	ADSW/CE	Enable/address selection (I^2C bus)

Pin Description and Equivalent Circuit

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin Voltage [V]</th><th>Equivalent circuit</th><th>Description</th></tr>
<tr><td>1</td><td>CL</td><td>—</td><td>
</td><td>Clock input.</td></tr>
<tr><td>2</td><td>DA</td><td>—</td><td>
</td><td>DATA input.</td></tr>
<tr><td>3</td><td>BS3</td><td rowspan="2">ON : 4.8
OFF : 0.0</td><td rowspan="2">
</td><td rowspan="4">Band switch outputs.
The pin corresponding to the selected band goes High.</td></tr>
<tr><td>8</td><td>BS4</td></tr>
<tr><td>4</td><td>BS1</td><td rowspan="2">2.1</td><td rowspan="2">
</td></tr>
<tr><td>7</td><td>BS2</td></tr>
<tr><td>5</td><td>IFIN1</td><td rowspan="2">2.1</td><td rowspan="2">
</td><td rowspan="2"></td></tr>
<tr><td>6</td><td>IFIN2</td></tr>
<tr><td>9</td><td>VCC1</td><td>—</td><td></td><td>Analog circuit power supply.</td></tr>
</table>

Pin No.	Symbol	Pin Voltage [V]	Equivalent circuit	Description
10	MIXOUT1	—		Mixer output. These pins output the signal with open collector, and they must be connected to the power supply via the load.
11	MIXOUT2	—		
12	GND1	—	—	Analog circuit GND.
13	BYP/MS	3.8 during VHF reception 3.8 during UHF reception		Pin 12 : VHF input grounding and control bus switching. Pin 13 : VHF input. Input format is the unbalanced input.
14	VHFin	2.6 during VHF reception 0.1 during UHF reception		
15	UHFin1	2.6 during UHF reception 0.1 during VHF reception		UHF inputs. Input the signal to Pins 14 and 15 symmetrically or ground either of Pin 14 or 15 with the capacitor and input the signal to the rest.
16	UHFin2	2.6 during UHF reception 0.1 during VHF reception		
17	VOSC1	2.1 during VHF reception 2.3 during UHF reception		External resonance circuit connection for VHF oscillator.
19	VOSC2	4.2 during VHF reception 5.0 during UHF reception		
18	GND	—	—	GND for separating the analog and PLL systems.

Pin No.	Symbol	Pin Voltage [V]	Equivalent circuit	Description
20	UOSCB1	2.1 during UHF reception 2.3 during VHF reception		External resonance circuit connection for UHF oscillator.
21	UOSCE1	1.4 during UHF reception 1.8 during VHF reception		
22	UOSCE2	1.4 during UHF reception 1.8 during VHF reception		
23	UOSCB2	2.1 during UHF reception 2.3 during VHF reception		
24	VCC2	—	—	PLL circuit power supply
25	GND2	—	—	PLL circuit GND.
26	IFOUT	2.7		I/F output.
27	NC	—	—	
28	VT	—		Varicap drive voltage output. This pin outputs the signal with open collector, and this must be connected to the tuning power supply via the load. Charge pump output. Connects the loop filter.
29	CPO	2.0		
30	REFOSC	4.3		Crystal connection for reference oscillator.
31	VCC3	—	—	Power supply for external supply.
32	ADSW/CE	1.25 (when open)		I^2C bus setting : Address selection. Bits 1 and 2 of the address byte are controlled. 3-wire bus setting : Enable input.

Electrical Characteristics

Circuit Current (VCC=5 V, Ta=25°C)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Circuit current A	AI_{CCV}	V_{CC}1 current, band switch output open during VHF operation				mA
	AI_{CCU}	V_{CC}1 current, band switch output open during UHF operation				mA
Circuit current D	DI_{CC}	V_{CC}2 current				mA

OSC/MIX/IF Amplifier Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Conversion gain	CG1	VHF operation f_{RF}=55 MHz				dB
	CG2	VHF operation f_{RF}=360 MHz				dB
	CG3	UHF operation f_{RF}=360 MHz				dB
	CG4	UHF operation f_{RF}=800 MHz				dB
Noise figure *1, *2	NF1	VHF operation f_{RF}=55 MHz				dB
	NF2	VHF operation f_{RF}=360 MHz				dB
	NF3	UHF operation f_{RF}=360 MHz				dB
	NF4	UHF operation f_{RF}=800 MHz				dB
1% cross modulation *1,*3	CM1	VHF operation f_D=55 MHz, f_{UD}=±12 MHz				dBµ
	CM2	VHF operation f_D=360 MHz, f_{UD}=±12 MHz				dBµ
	CM3	UHF operation f_D=360 MHz, f_{UD}=±12 MHz				dBµ
	CM4	UHF operation f_D=800 MHz, f_{UD}=±12 MHz				dBµ
Maximum output power	Pomax	50 Ω load saturation output				dBm
Switch ON drift *4	Δ fsw1	VHF operation f_{OSC}=100 MHz Δ f from 3 s to 3 min after switch ON				kHz
	Δ fsw2	VHF operation f_{OSC}=405 MHz Δ f from 3 s to 3 min after switch ON				kHz
	Δ fsw3	UHF operation f_{OSC}=405 MHz Δ f from 3 s to 3 min after switch ON				kHz
	Δ fsw4	UHF operation f_{OSC}=845 MHz Δ f from 3 s to 3 min after switch ON				kHz

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Supply voltage *4 drift	Δ fst1	VHF operation fosc=100 MHz Δ f when Vcc 5 V changes ±5%				kHz
	Δ fst2	VHF operation fosc=405 MHz Δ f when Vcc 5 V changes ±5%				kHz
	Δ fst3	UHF operation fosc=405 MHz Δ f when Vcc 5 V changes ±5%				kHz
	Δ fst4	UHF operation fosc=845 MHz Δ f when Vcc 5 V changes ±5%				kHz
Oscillator phase noise	C/N V	10 kHz offset				dBc/Hz
	C/N U	10 kHz offset				dBc/Hz
Reference leak	REFL	Phase comparison frequency of 62.5 kHz, CP : 1				dB
Lock-up time	LUT 1					msec
	LUT 2					msec

*1 Value measured with untuned input.

*2 NF meter direct-reading value (DSB measurement).

*3 Value with a desired reception signal input level of –30 dBm, an interference signal of 100 kHz/30 % AM, and an interference signal level where S/I=46 dB measuered with a spectrum analyzer.

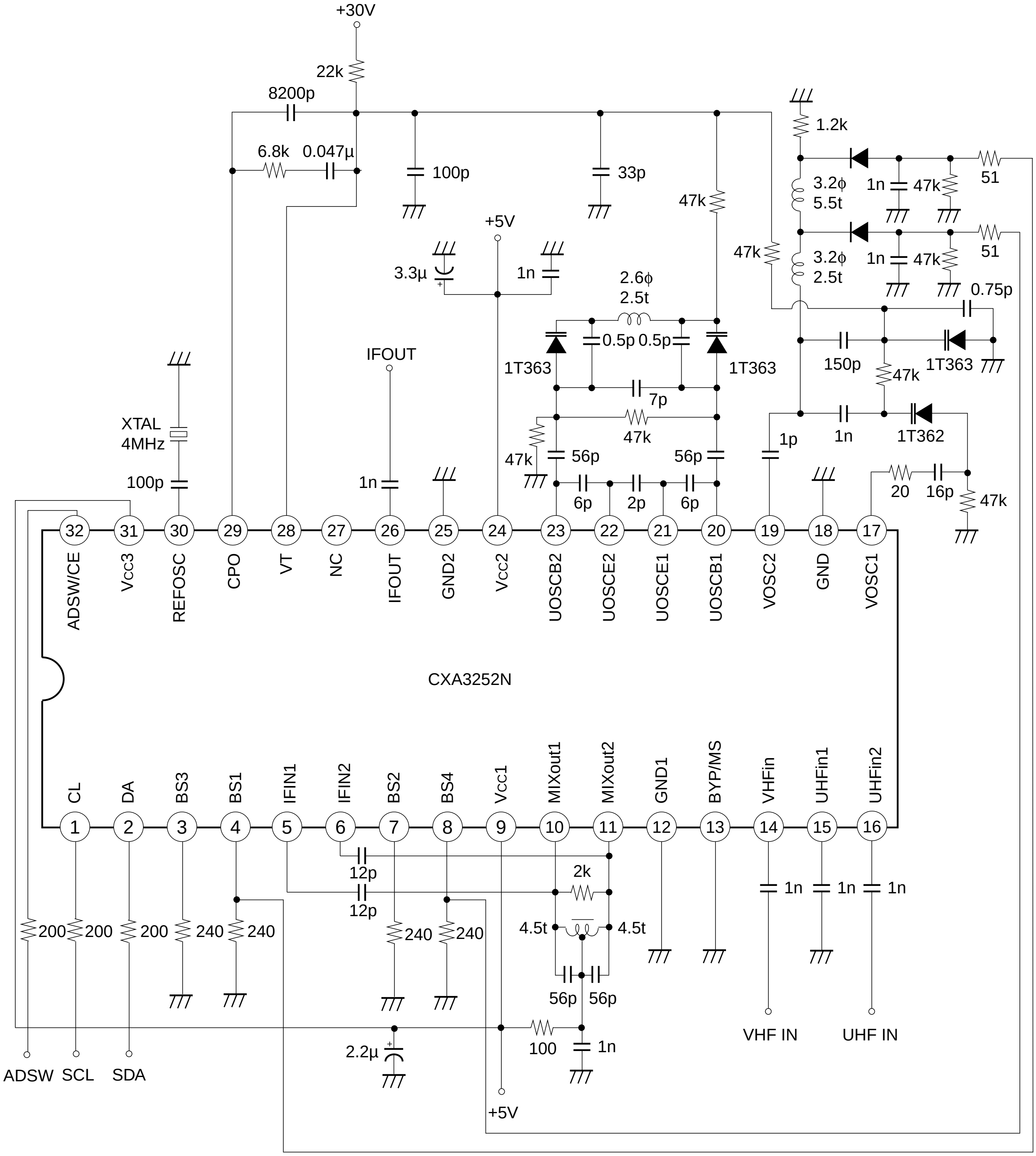
*4 Value when the PLL is not operating.

PLL Block

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
CL, DA pins						
"H" level input voltage	V_{IH}		3		V_{CC}	V
"L" level input voltage	V_{IL}		GND		1.5	V
"H" level input current	I_{IH}	V_{IH}=V_{CC}		0	–0.1	µA
"L" level input current	I_{IL}	V_{IL}=GND		–0.3	–4	µA
CE input						
"H" level input voltage	V_{IH}		3		V_{CC}	V
"L" level input voltage	V_{IL}		GND		1.5	V
"H" level input current	I_{IH}	V_{IH}=V_{CC}		–100	–200	µA
"L" level input current	I_{IL}	V_{IL}=GND		35	100	µA
SDA output						
"H" output leak current	V_{IH}	Vin=5.5 V			5	V
"L" output voltage	V_{IL}	Iout=–3 mA	GND		0.4	V
CPO (charge pump)						
Output current 1	I_{CPO1}	Byte4/Bit6=0	±35	±50	±75	µA
Leak current 1	LeakCP1	Byte4/Bit6=0			30	nA
Output current 2	I_{CPO2}	Byte4/Bit6=1	±140	±200	±300	µA
Leak current 2	LeakCP2	Byte4/Bit6=1			100	nA
VT (VC voltage output)						
Maximum output voltage	V_{TH}				33	V
Minimum output voltage	V_{TL}			0.5	0.8	V
LOCK						
"H" output voltage	V_{LOCKH}	When locked	V_{CC}-0.5		V_{CC}	V
"L" output voltage	V_{LOCKL}	When unlocked	0		0.5	V
REFOSC						
Oscillation frequency range	F_{XTOSC}		3		12	MHz
Input capacitance	C_{XTOSC}		22	24	26	pF
Negative resistance	R_{NEG}	Crystal source impedance		–2	–1	kΩ
Band SW						
Output current	I_{BS}	When ON			–25	mA
Saturation voltage	V_{SAT}	When ON Source current=20 mA		120	240	mV
Leak current	LeakBS	When OFF		0.5	3	µA

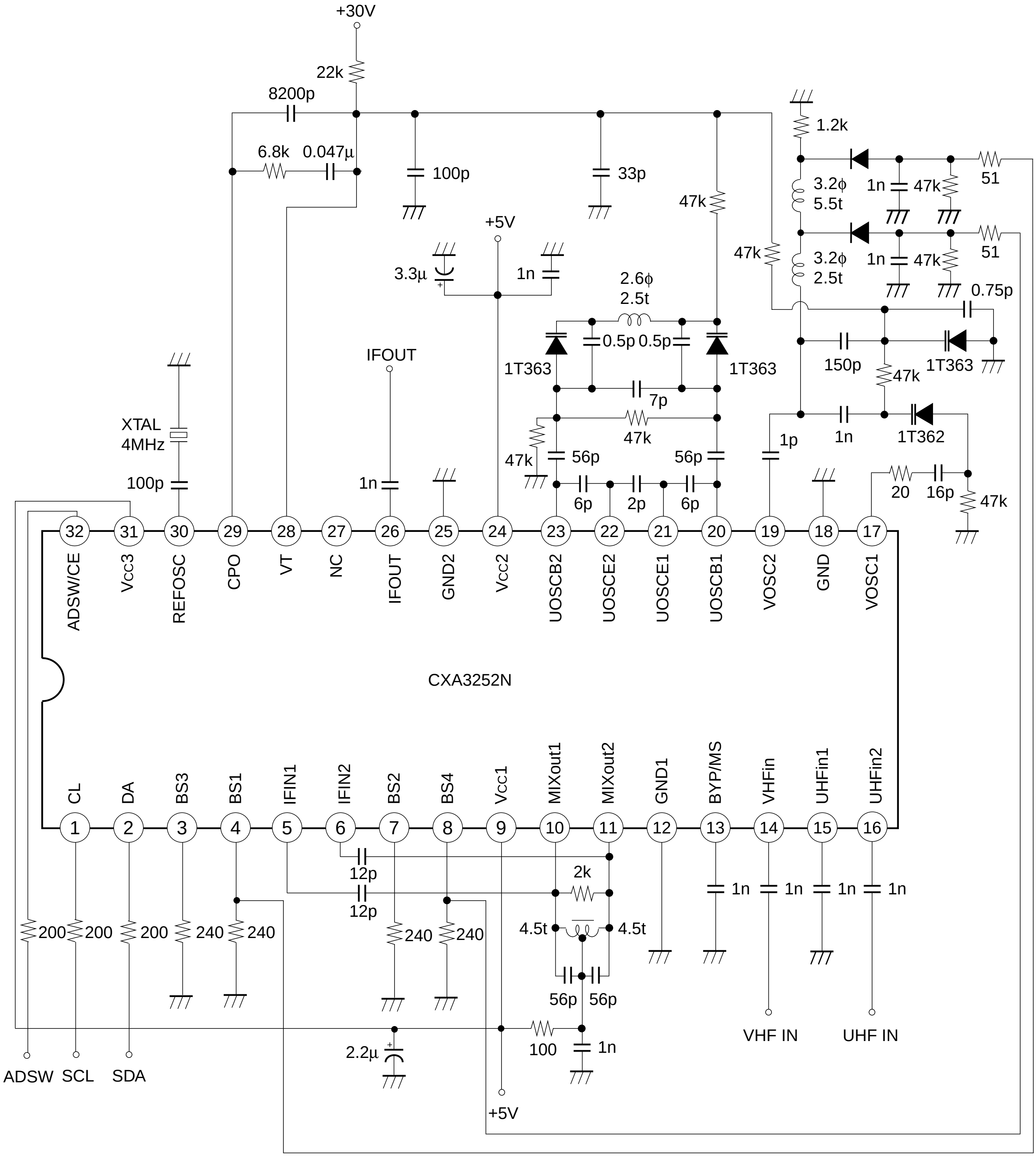
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Bus timing (I^2C bus)						
SCL clock frequency	f_{SCL}		0		400	kHz
Start waiting time	t_{WSTA}		1300			ns
Start hold time	t_{HSTA}		600			ns
"L" hold time	t_{LOW}		1300			ns
"H" hold time	t_{HIGH}		600			ns
Start setup time	t_{SSTA}		600			ns
Data hold time	ta_{HDAT}		1300			ns
Data setup time	t_{SDAT}		600			ns
Rise time	t_R				300	ns
Fall time	t_F				300	ns
Stop setup time	t_{SSTO}		600			ns
Bus timing (3-wire bus)						
Data setup time	t_{SD}		300			ns
Data hold time	t_{HD}		600			ns
Enable waiting time	t_{WE}		300			ns
Enable setup time	t_{SE}		300			ns
Enable hold time	t_{HE}		600			ns

Electrical Characteristics Measurement Circuit (I^2C bus control)



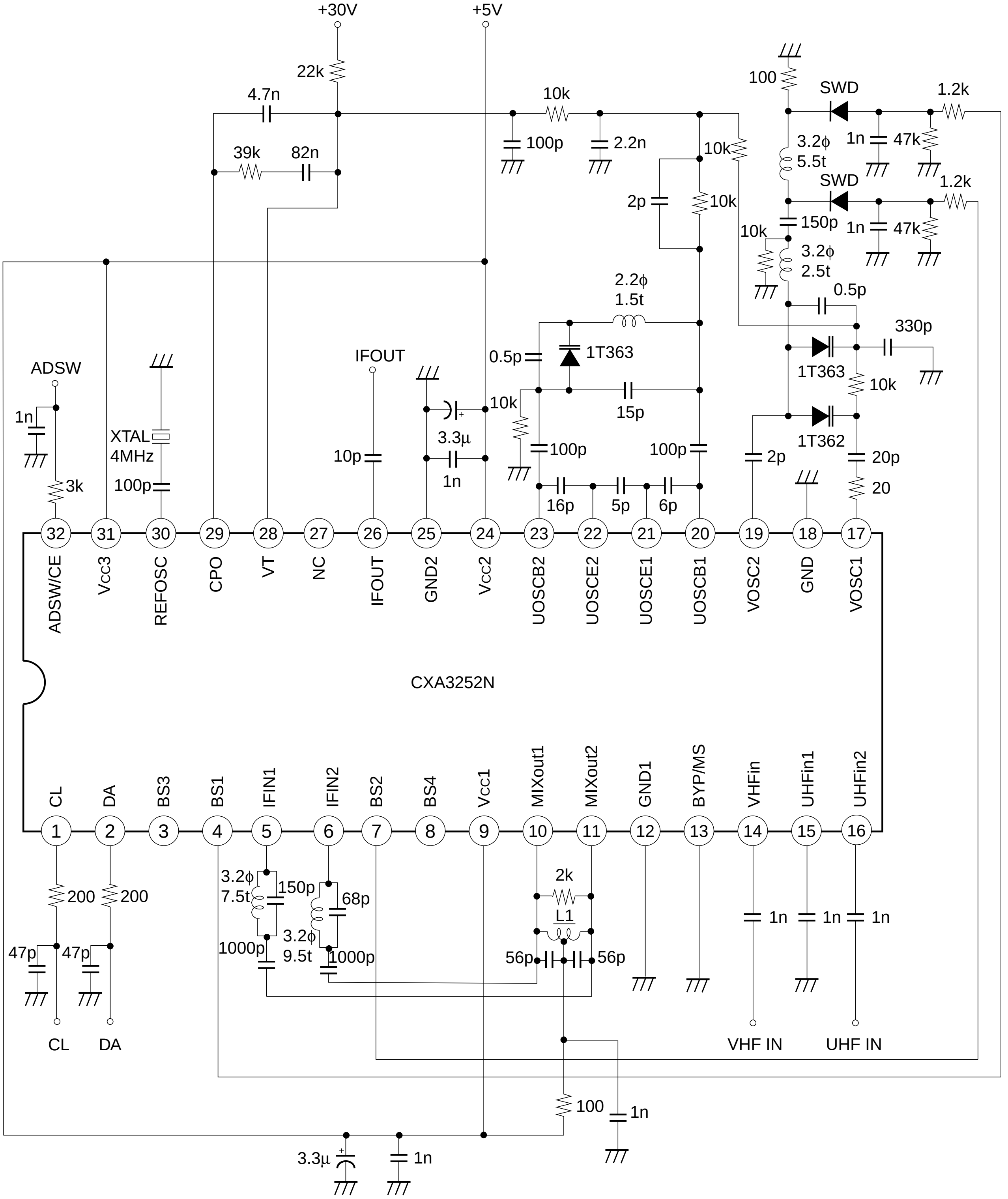
Unmarked Ls are air coils with a wire diameter of 0.5 mm.

Electrical Characteristics Measurement Circuit (3-wire bus control)



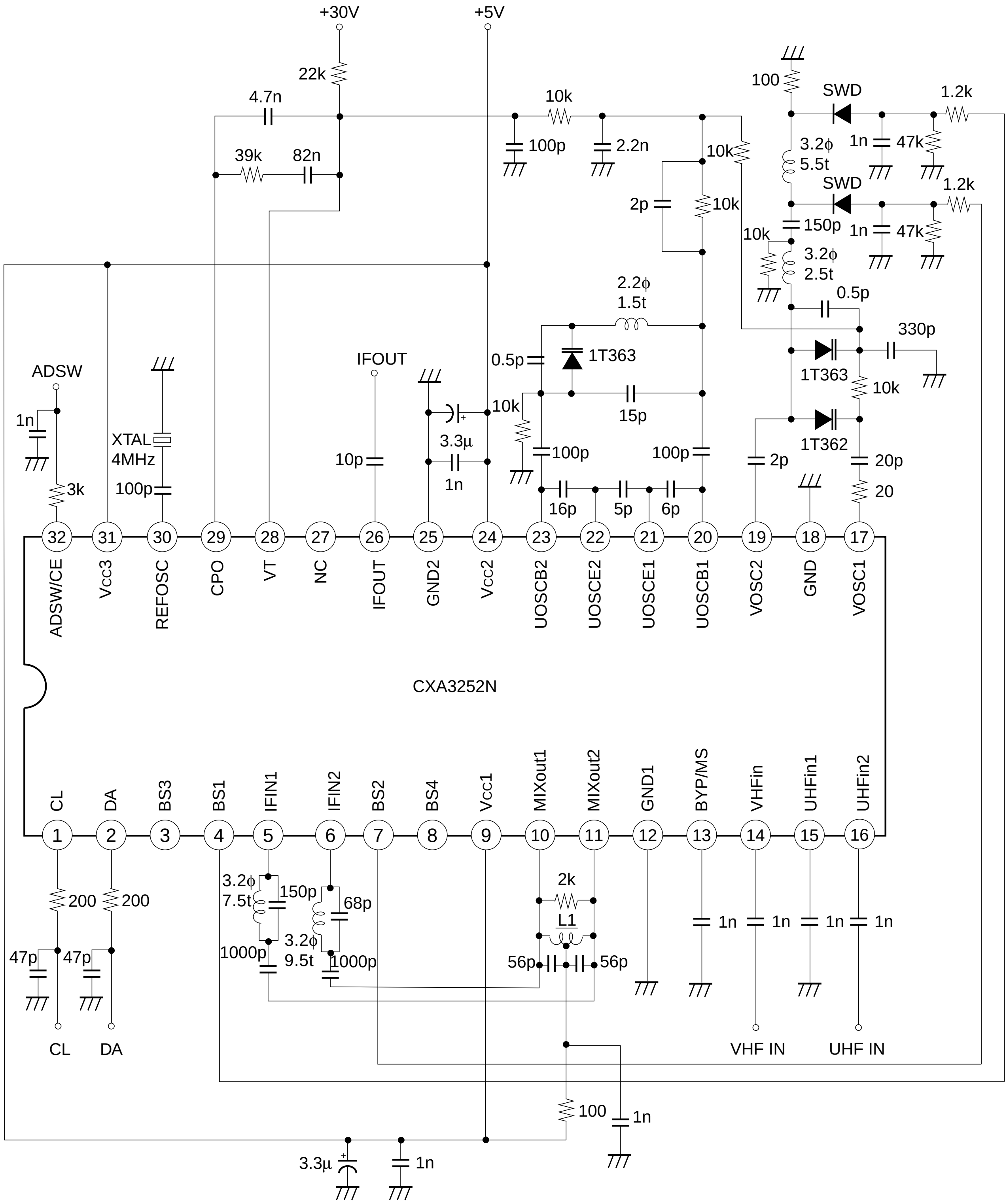
Unmarked Ls are air coils with a wire diameter of 0.5 mm.

Application Circuit (I^2C bus control)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (3-wire bus control)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Functions

The CXA3252N is a ground wave broadcast tuner IC which converts frequencies to IF in order to tune and detect only the desired reception frequency of VHF, CATV and UHF band signals.
In addition to the mixer, local oscillation and IF amplifier circuits required for frequency conversion to IF, this IC also integrates a PLL circuit for local oscillation frequency control onto a single chip.
The functions of the various circuits are described below.

1. Mixer circuit
   This circuit outputs the frequency difference between the signal input to VHFIN or UHFIN and the local oscillation signal.

2. Local oscillation circuit
   A VCO is formed by externally connecting an LC resonance circuit composed of a varicap diode and inductance.

3. IF amplifier circuit
   This circuit amplifies the mixer IF output, and consists of an amplifier stage and low impedance output stage.

4. PLL circuit
   This PLL circuit fixes the local oscillation frequency to the desired frequency. It consists of a programmable divider, reference divider, phase detector, charge pump and reference oscillator. The control format supports both the I^2C bus and 3-wire bus formats.
   During I^2C bus control, the frequency steps of 31.25, 50 or 62.5 kHz can be selected by the frequency division setting value of the data-based referencedivider.
   During 3-wire bus control, these frequency steps can be selected by the combination of the data length (18 or 19 bits) and the voltage applied to the BYP/MS pin.

5. Band switch circuit
   The CXA3252N has four sets of built-in PNP transistors for switching between the VL, VH and UHF bands and for switching the FM trap, etc. These PNP transistors can be controlled by the bus data.
   The emitters for these PNP transistors are connected to an independent power supply pin ($V_{CC}3$) from the oscillator, mixer and PLL circuits, and support either 5 V or 9 V as the RF amplifier power supply.

Description of Analog Block Operation

(See the Electrical Characteristics Measurement Circuit.)

VHF oscillator circuit

- This circuit is a differential amplifier type oscillator circuit. Pin 19 is the output and Pin 17 is the input. Oscillation is performed by connecting an LC resonance circuit including a varicap to Pin 19 via coupled capacitance, inputting to Pin 17 with feedback capacitance, and applying positive feedback.
- The amplifier between Pins 17 and 19 has an extremely high gain. Therefore, care should be taken to avoid creating parasitic capacitance, resistance or other feedback loops as this may produce abnormal oscillation.

VHF mixer circuit

- The mixer circuit employs a double balanced mixer with little local oscillation signal leakage.
  The input format is base input type, with Pin 13 grounded via a capacitor and the RF signal input to Pin 14. (Pin 13 can also be used to switch the PLL mode according to the applied DC voltage value.)
- The RF signal is converted to IF frequency by oscillator signal and output from Pins 10 and 11.
  Pins 10 and 11 are open collectors, so external power supply is necessary. In addition, single-tuned filters are connected to Pins 10 and 11.

UHF oscillator circuit

- This oscillator circuit is designed so that two collector ground type Colpitts oscillators perform differential oscillation operation via an LC resonance circuit including a varicap.
- Resonance capacitance is connected between Pins 20 and 21, Pins 21 and 22, and Pins 22 and 23, and an LC resonance circuit including a varicap is connected between Pins 20 and 23.

UHF mixer circuit

- This circuit employs a double balanced mixer like the VHF mixer circuit.
  The input format is base input type, with Pins 15 and 16 as the RF input pins. The input method can be selected from balanced input consisting of differential input to Pins 15 and 16 or unbalanced input consisting of grounding Pin 15 via a capacitor and input to Pin 16.
- Pins 10 and 11 are the mixer outputs. Pins 10 and 11 are open collectors, so external power supply is necessary. In addition, single-tuned filters are connected to Pins 10 and 11.

IF amplifier circuit

- Pins 5 and 6 are IF amplifier inputs with an input impedance of approximately 1 kΩ.
- The signals frequency converted by the mixer are output from Pins 10 and 11, so Pins 10 and 11 are connected to Pins 5 and 6 via capacitors. (A neighboring channel trap circuit can be formed by connecting a L and C parallel circuit instead of capacitors.)
- The signal amplified by the IF amplifier is output from Pin 26.
  The output impedance is approximately 75 Ω.

Description of PLL Block

This IC supports both I²C bus and 3-wire bus control.
The I²C bus conforms to the standard I²C bus format, and bidirectional bus control is possible consisting of a write mode in which various data are received and a read mode in which various data are sent.
The 3-wire bus is equipped with an 18- or 19-bit auto identify function, and the frequency step can be switched according to the voltage applied to the BYP/MS pin.
The PLL of this IC does not have a fixed frequency division circuit and performs high-speed phase comparison, providing low reference leak and quick lock-up time characteristics.

Pin Function Table

Symbol	I²C bus	3-wire bus
CL	SCL input	CLOCK input
DA	SDA I/O	DATA input
ADSW/CE	Address selection	ENABLE input

1) PLL Mode Setting Method

The selected control bus is set according to the BYP/MS pin (Pin 13) voltage.

BYP/MS pin	Control bus
GND	I²C Bus
OPEN	3-wire bus
Vcc	3-wire bus

During 3-wire bus control, the transferred bit length (18, 19 or 27 bits) is automatically identified.
During 18- or 19-bit transfer, the frequency steps in the table below are set according to the combination of the BYP/MS pin voltage and the bit length. This IC does not have a fixed frequency division circuit, so the phase comparison frequency becomes the frequency step.

BYP/MS Pin voltage	Transfer bit length	Reference Divider	Phase comparison frequency	Frequency Step*
	18	64	62.5 kHz	62.5 kHz
OPEN	19	128	31.25 kHz	31.25 kHz
OPEN or VCC	27	Selectable from 64, 80 or 128	62.5 kHz/ 50.0 kHz/ 31.25 kHz	62.5 kHz/ 50.0 kHz/ 31.25 kHz
VCC	18	80	50.0 kHz	50.0 kHz
VCC	19	80	50.0 kHz	50.0 kHz

* Phase comparison frequency and frequency step are for when the crystal oscillation=4 MHz.

2) Programming

The VCO lock frequency is obtained according to the following formula.

$fosc = fref \times (32\,M + S)$

fosc : local oscillator frequency
fref : phase comparison frequency
M : main divider frequency division ratio
S : swallow counter frequency division ratio

The variable frequency division ranges of M and S are as follows, and are set as binary.

$S < M \leq 1023$ ($S < M \leq 511$ during 18-bit transfer)
$0 \leq S \leq 31$

3) I²C Bus Control

This IC conforms to the standard I²C bus format, and bidirectional bus control is possible consisting of a write mode in which various data are received and a read mode in which various data are sent. Write and read modes are recognized according to the setting of the final bit (R/W bit) of the address byte. Write mode is set when the R/W bit is “0” and read mode is set when the R/W bit is “1”.

3-1) Address settings

Up to four addresses can be selected by the hardware bit settings, so that multiple PLL can exist within one system.

The responding address can be set according to the ADSW/CE pin voltage.

1	1	0	0	0	MA1	MA0	R/W

Address

"CE" pin voltage	MA1	MA0
0 to 0.1 VCC	0	0
OPEN or 0.2 VCC to 0.3 VCC	0	1
0.4 VCC to 0.6 VCC	1	0
0.9 VCC to VCC	1	1

Hardware bits

3-2) Write mode

Write mode is used to receive various data. In this mode, byte 1 contains the address data, bytes 2 and 3 contain the frequency data, byte 4 contains the control data, and byte 5 contains the band switch data. These data are latch transferred in the manner of byte 1, byte 2 + byte 3, and byte 4 + byte 5.

When the correct address is received and acknowledged, the data is recognized as frequency data if the first bit of the next byte is "0", and as control data and band switch data if this bit is "1".

Also, when data transmission is stopped part-way, the previously programmed data is valid. Therefore, once the control and band switch data have been programmed, 3-byte commands consisting of the address and frequency data are possible.

Further, even if the I^2C bus stop conditions are not met, data can be input by sending the start conditions and the new address.

The control format is as shown in the table below.

Write-mode : Slave Receiver

	MSB							LSB	
MODE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address byte	1	1	0	0	0	MA1	MA0	0	A
Divider byte 1	0	M9	M8	M7	M6	M5	M4	M3	A
Divider byte 2	M2	M1	M0	S4	S3	S2	S1	S0	A
Control byte	1	CP	0	CD	X	R1	R0	OS	A
Band SW byte	X	X	X	X	BS4	BS3	BS2	BS1	A

X : Don't care

A : Acknowledge bit
MA0, MA1 : address setting
M0 to : main divider frequency division ratio setting
S0 to : swallow counter frequency division ratio setting
CD : charge pump OFF (when "1")
OS : varicap output OFF (when "1")
CP : charge pump current switching (200 µA when "1", 50 µA when "0")
BS1 to BS4 : band switch control (output PNP transistor ON when "1")
R0, R1 : reference divider frequency division ratio setting.
(see the Reference Divider Frequency Division Ratio Table)

Reference Divider Frequency Division Ratio Table

R1	R0	Reference divider
0	1	128
1	1	64
X	0	80

X : Don't care

3-3) Read mode

In read mode, power- on reset operation status the phase comparator locked/unlocked status and 5-level A/D converter input pin voltage status are transmitted and output to the master.

The read data format is as shown in the table below.

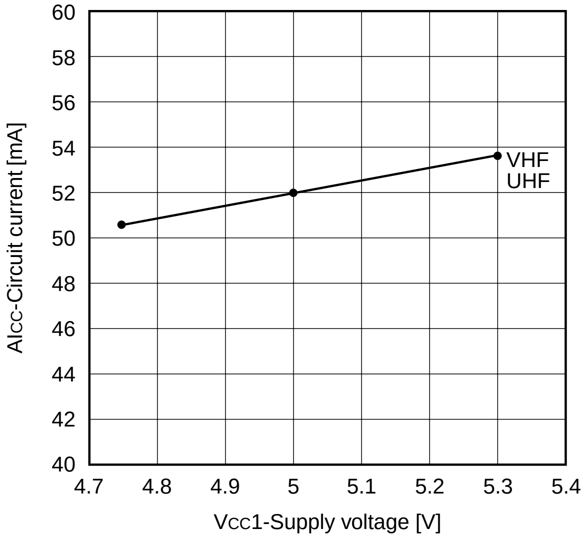
Read mode : Slave Transmitter

MODE	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte	X	FL	1	1	1	0	0	0	A

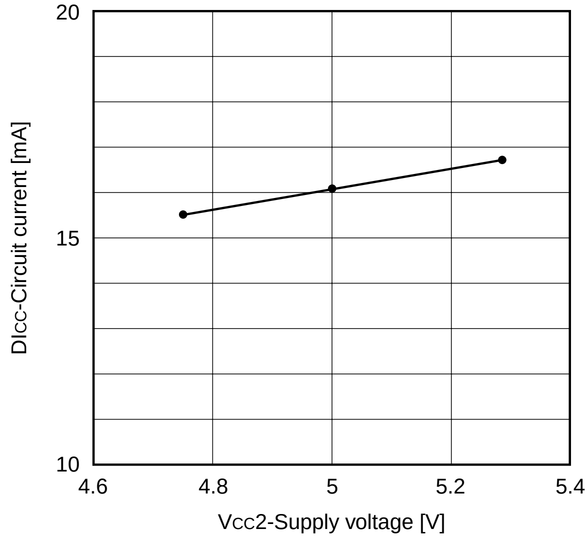
A : Acknowledge bit
MA0, MA1 : address setting
FL : lock detection signal (1 : locked, 0 : unlocked)

Example of Representative Characteristics

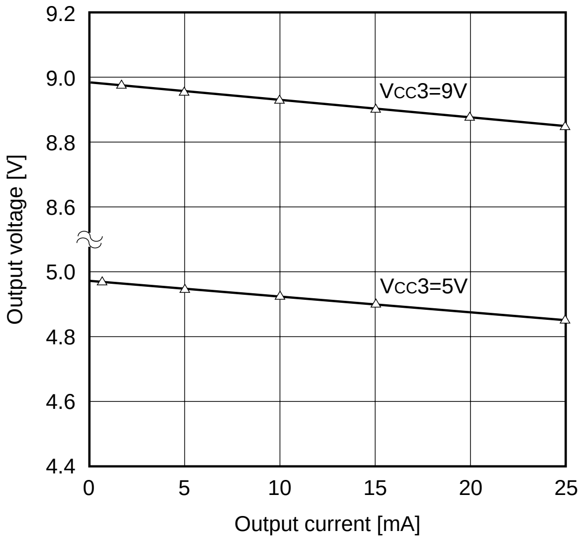
Circuit current vs. Supply voltage 1



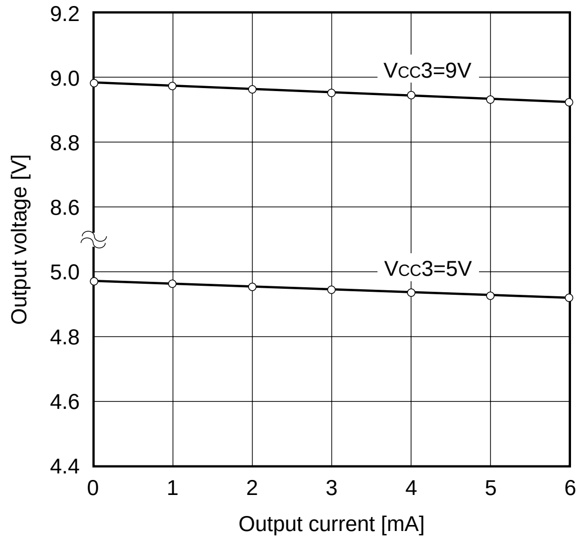
Circuit current vs. Supply voltage 2



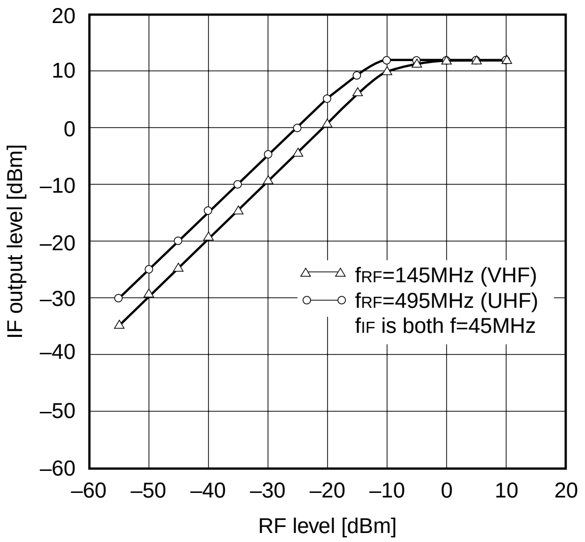
Band SW output voltage vs. Output current (BS1, BS2, BS3, BS4)



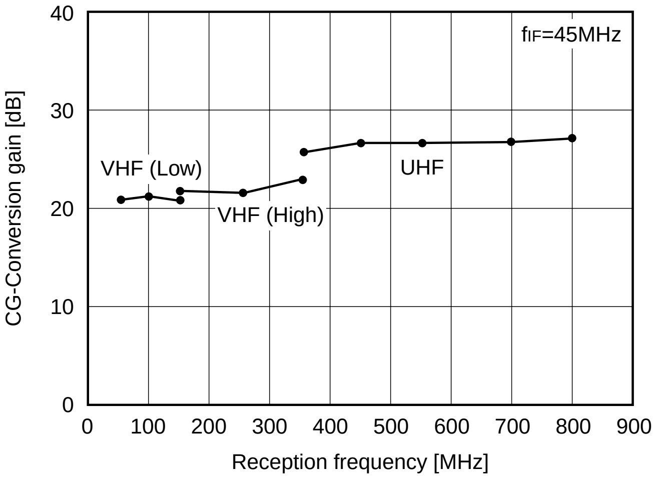
Band SW output voltage vs. Output current



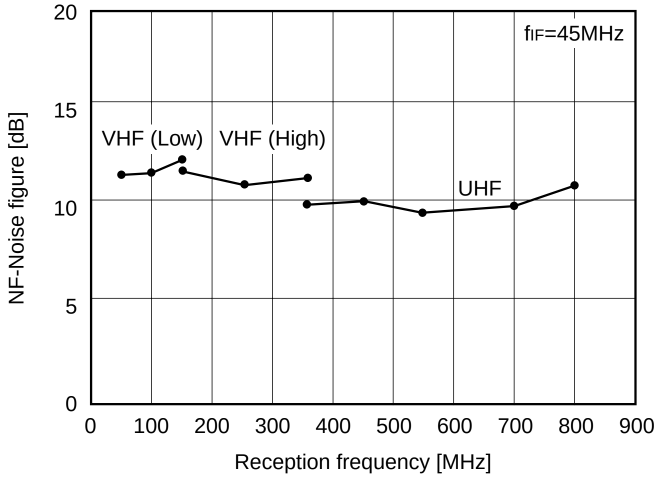
I/O characteristics (Untuned input)



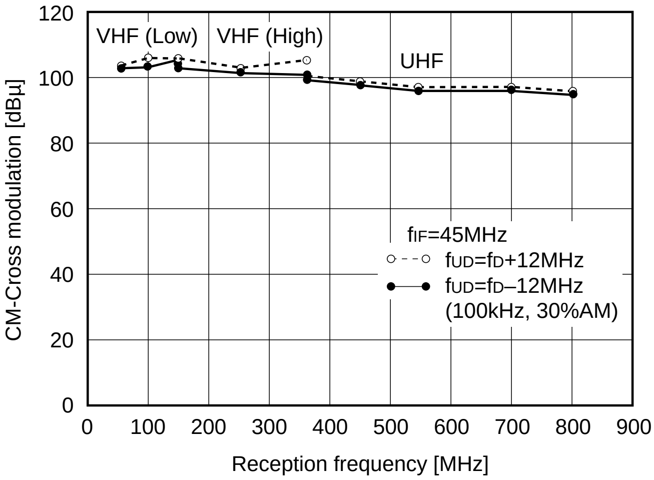
Conversion gain vs. Reception frequency (Untuned input)



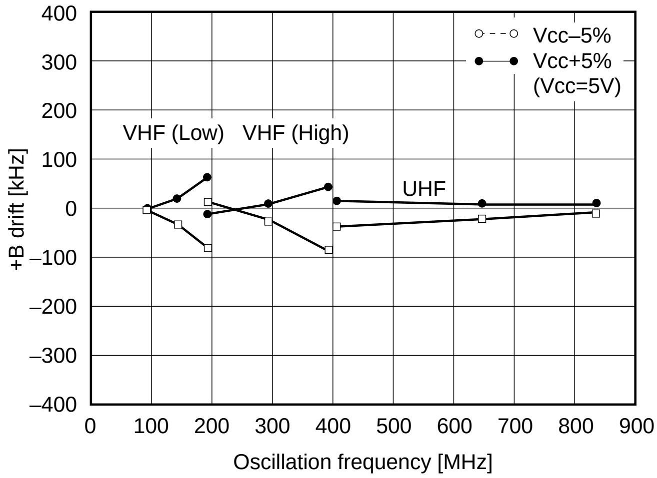
Noise figure vs. Reception frequency (Untuned input, in DSB)



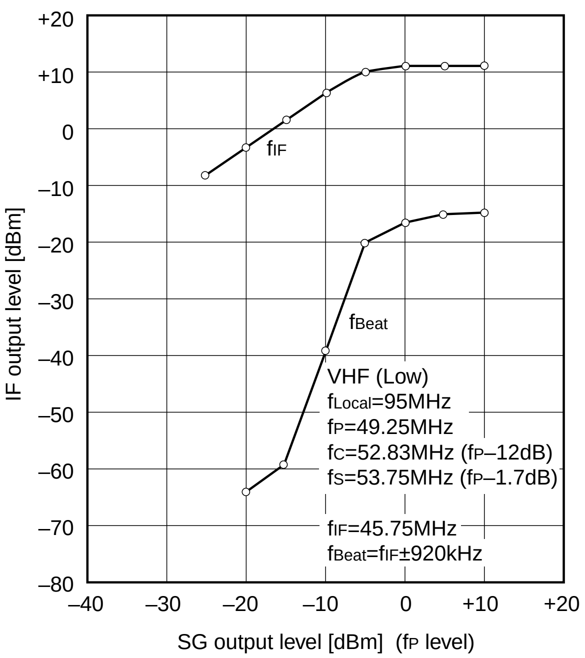
Next adjacent cross modulation vs. Reception frequency (Untuned input)



Oscillation frequency power supply fluctuation (PLL off)

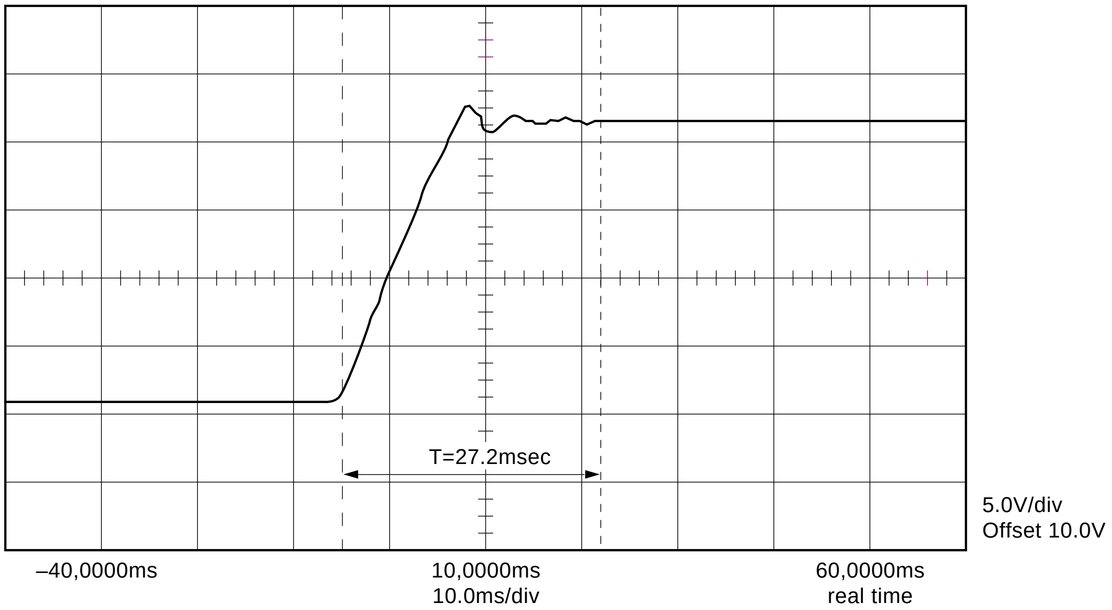


PCS beat characteristics

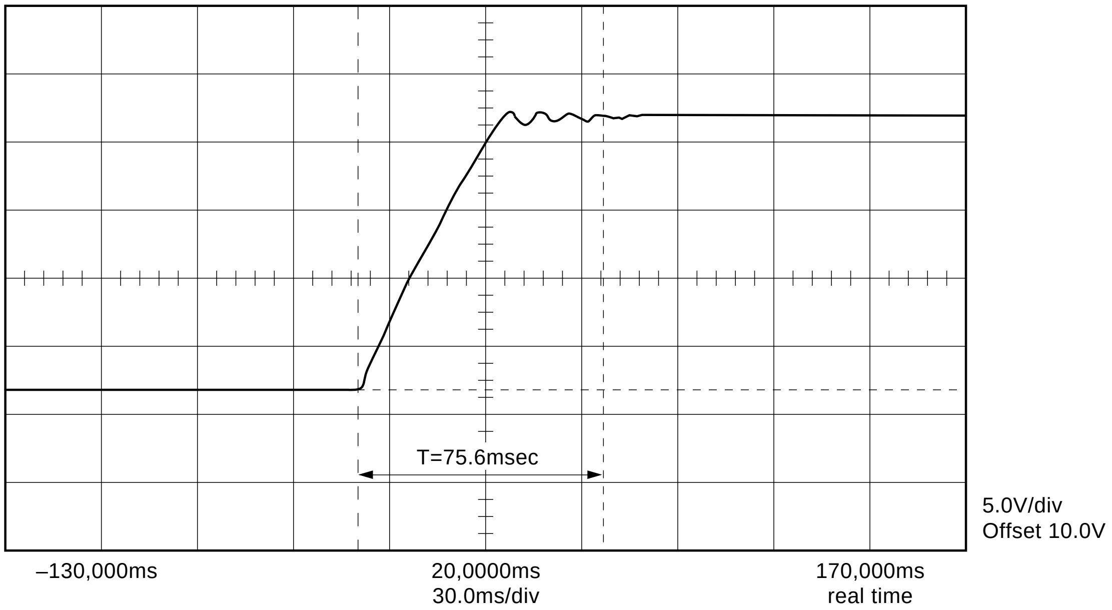


Tuning Response Time 1

VHF (Low) 95MHz → VHF (High) 395MHz (CP=1)

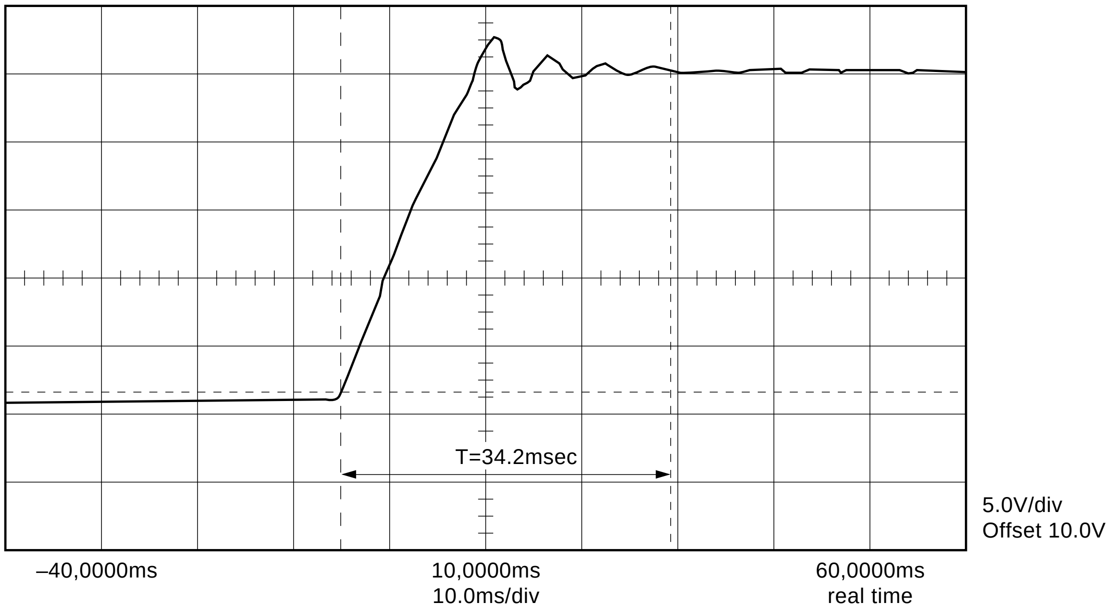


VHF (Low) 95MHz → VHF (High) 395MHz (CP=0)

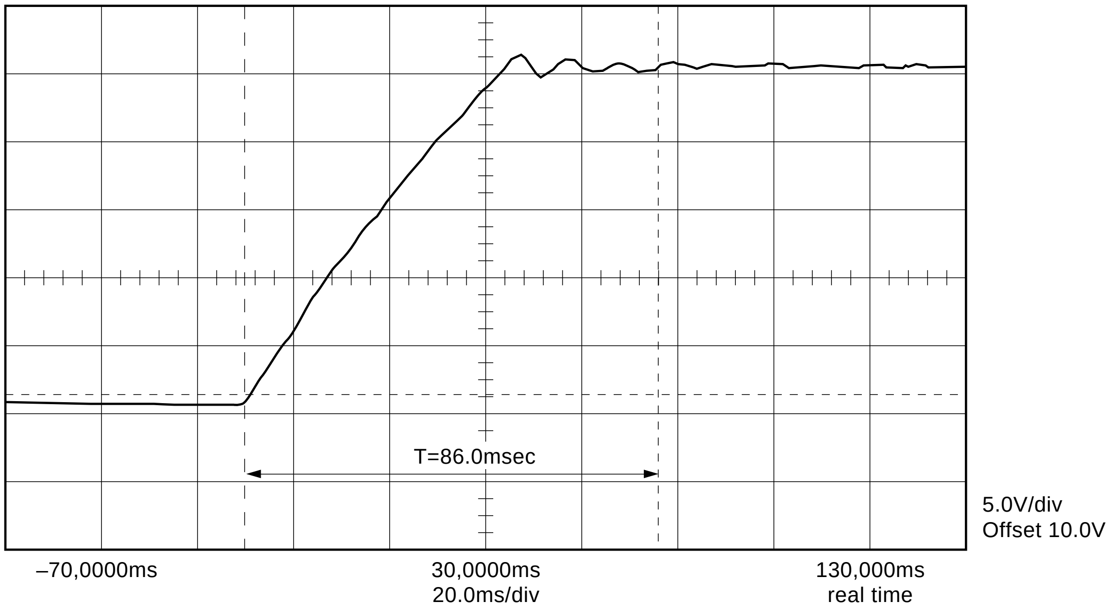


Tuning Response Time 2

UHF 413MHz → UHF 847MHz (CP=1)

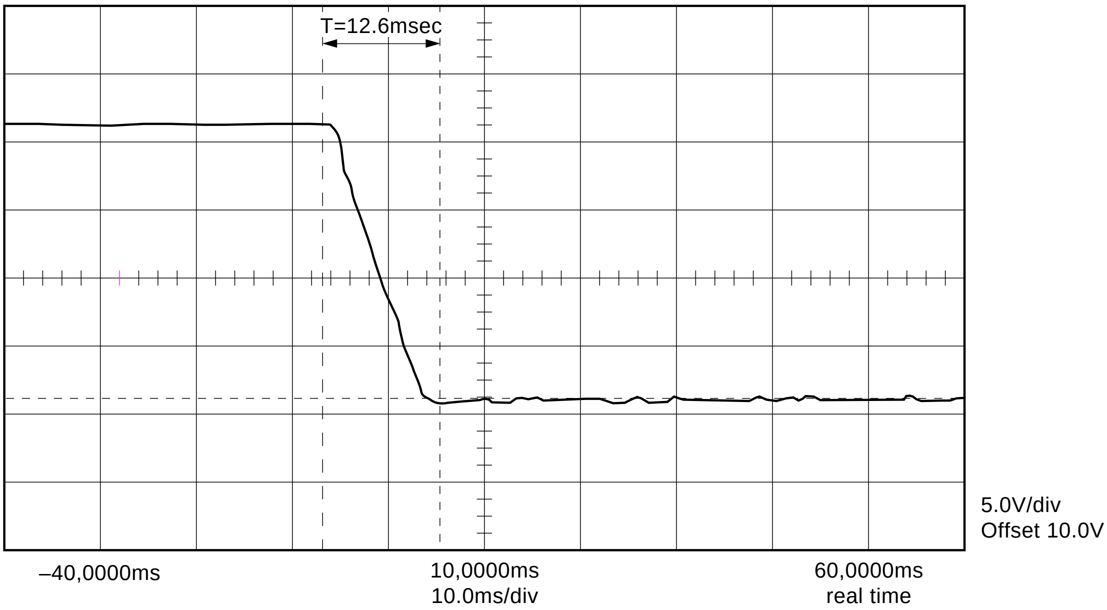


UHF 413MHz → UHF 847MHz (CP=0)

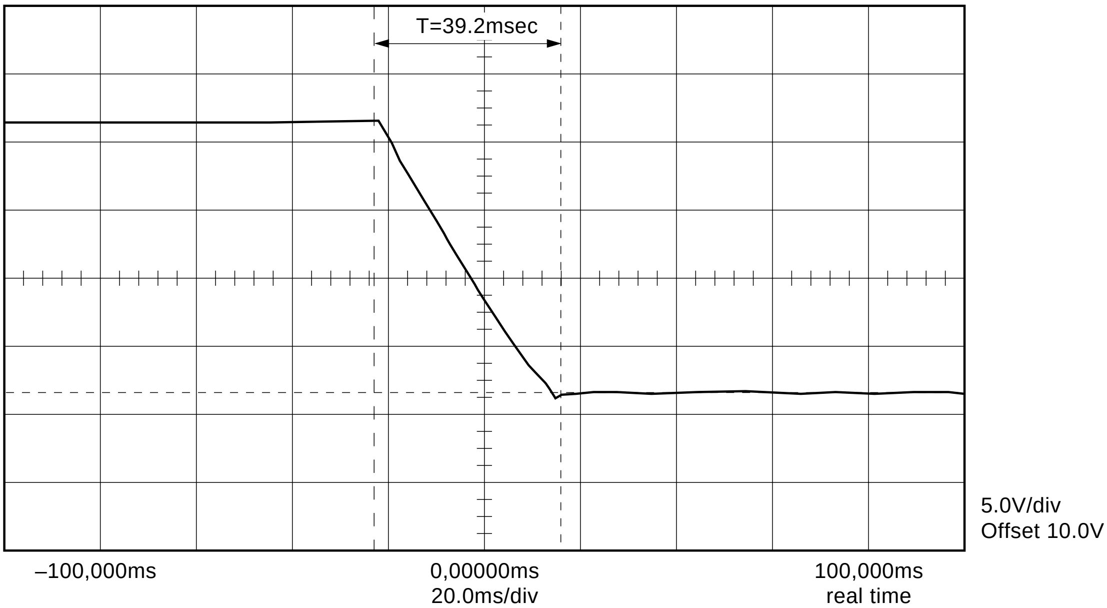


Tuning Response Time 3

VHF (High) 395MHz → VHF (Low) 95MHz (CP=1)

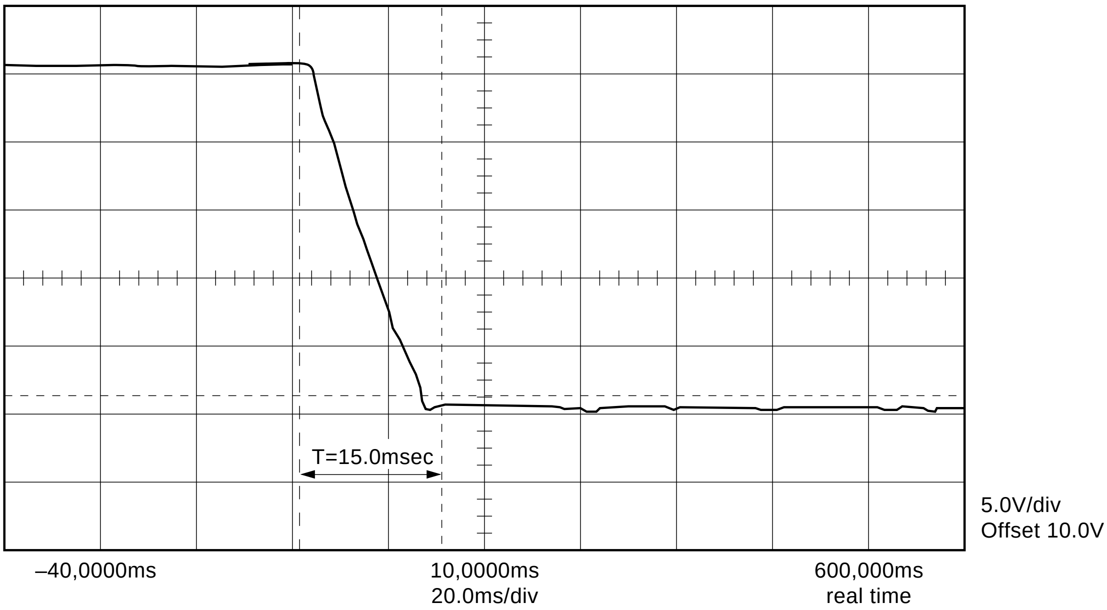


VHF (High) 395MHz → VHF (Low) 95MHz (CP=0)

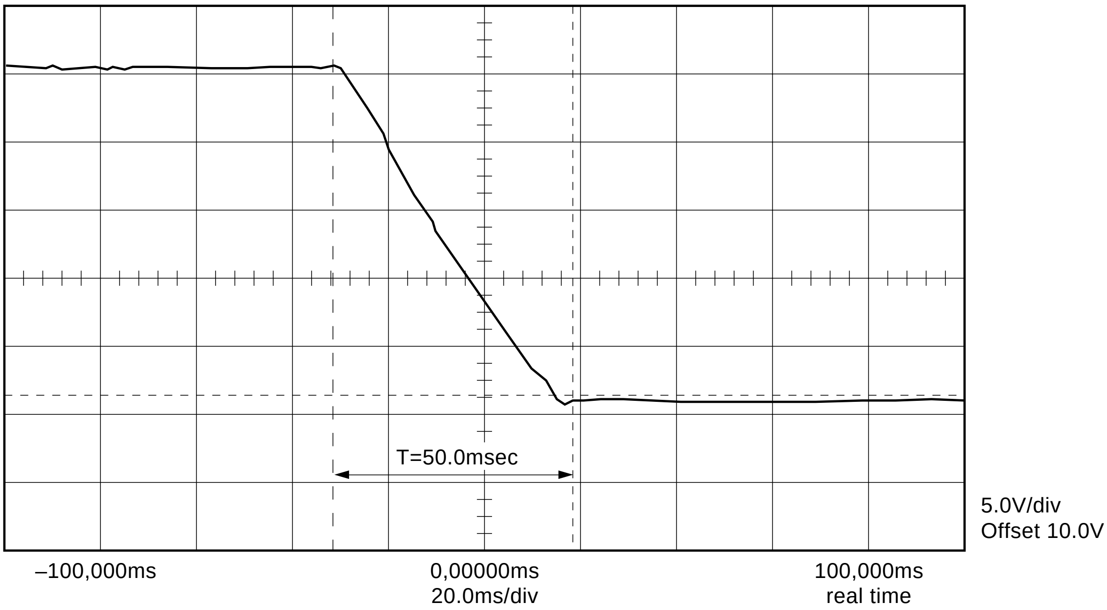


Tuning Response Time 4

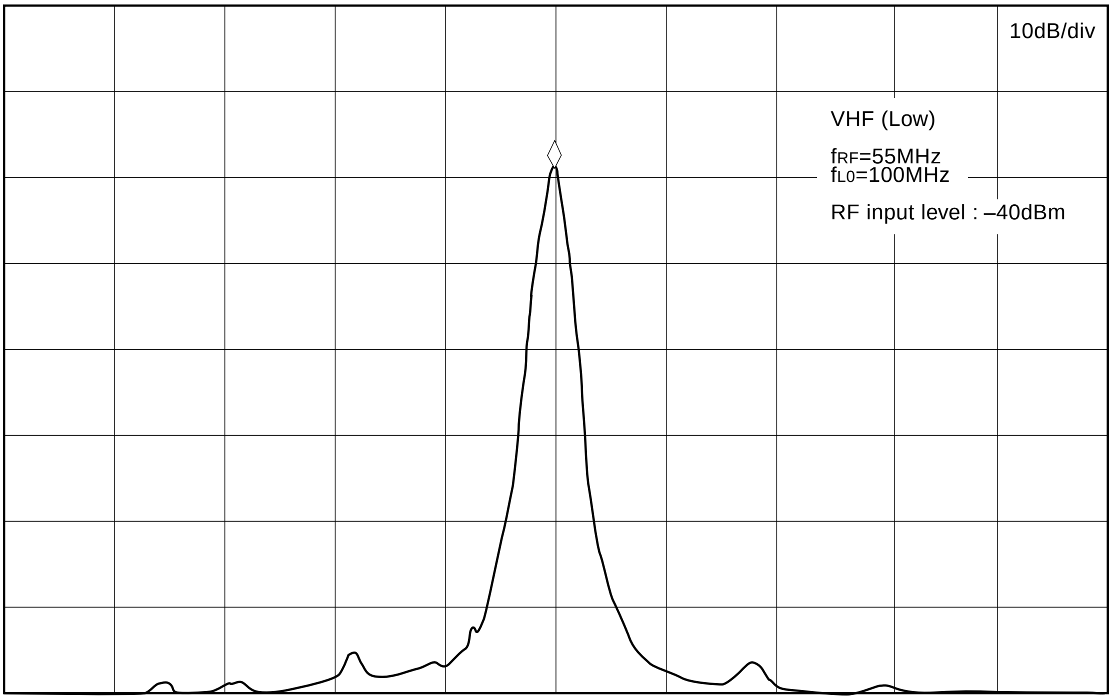
UHF 847MHz → UHF 413MHz (CP=1)



UHF 847MHz → UHF 413MHz (CP=0)

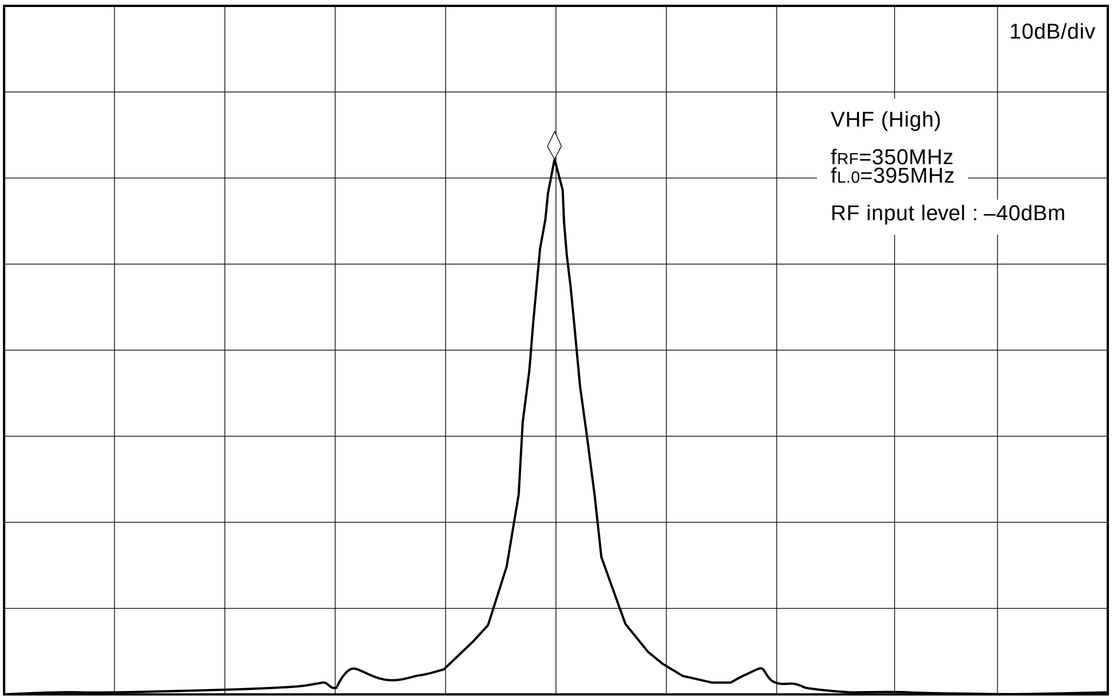


IF output spectrum



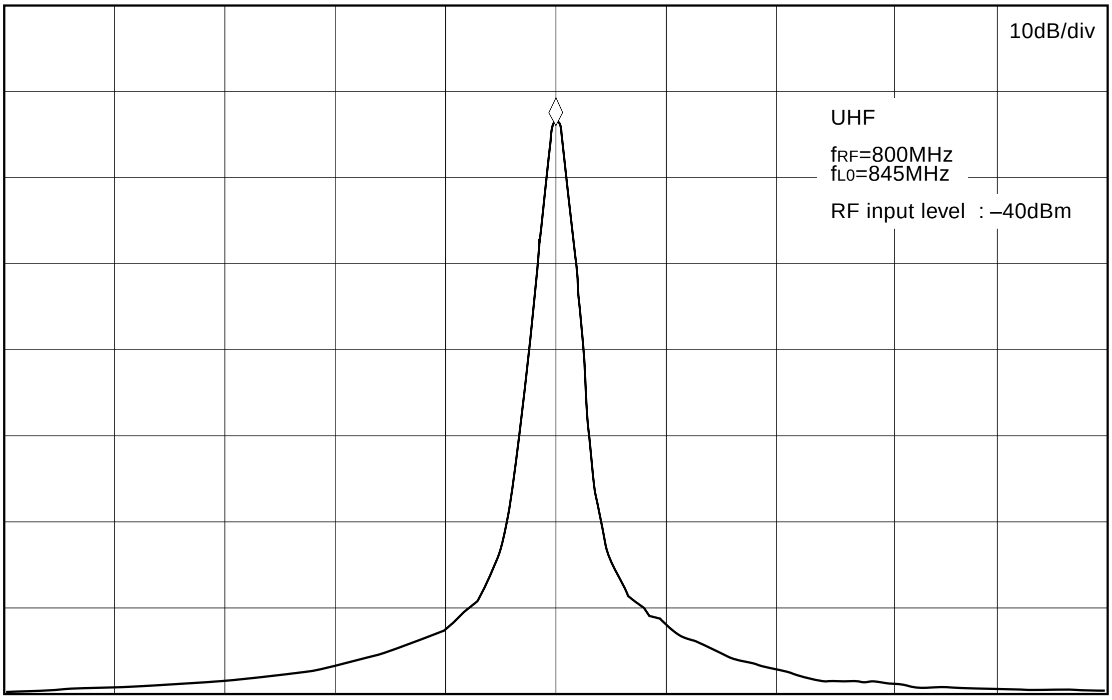
CENTER 45.0MHz SPAN 100.0kHz
#RES BW 1.0kHz #VBW 10Hz SWP 30.0 sec

IF output spectrum



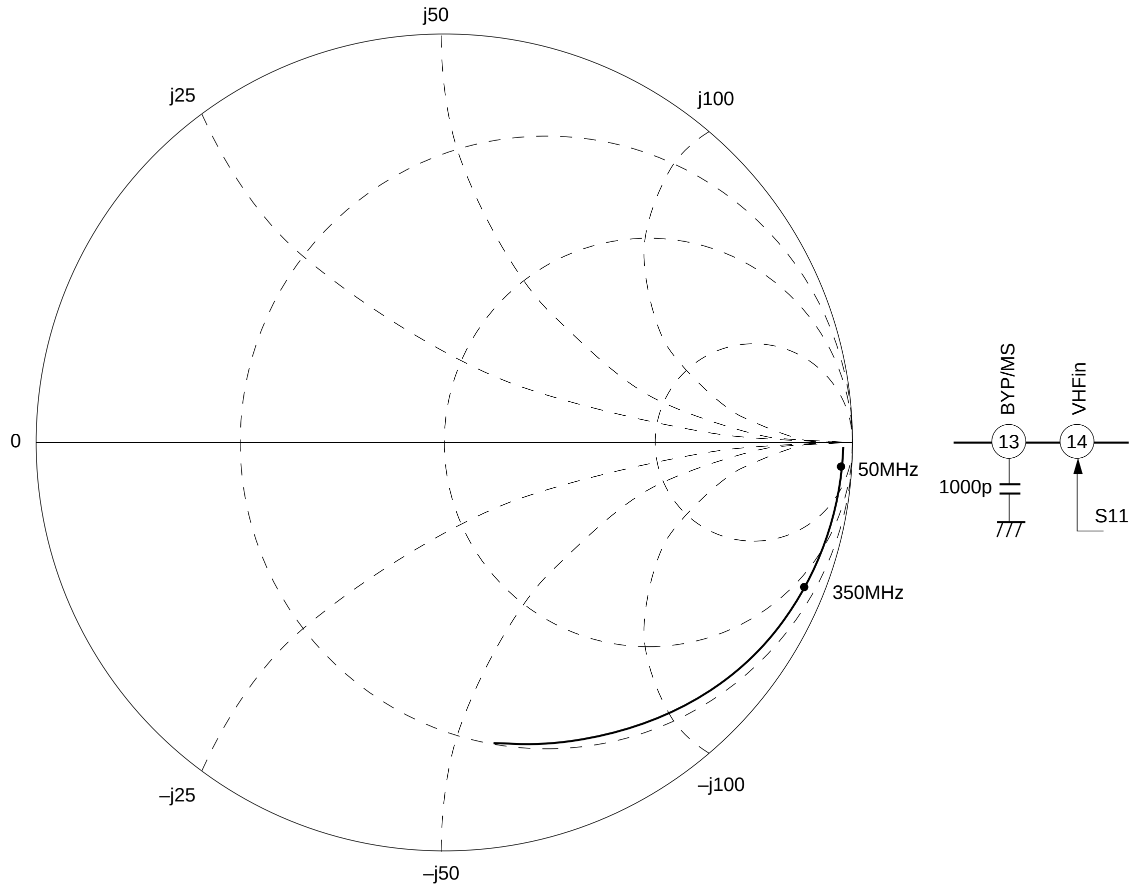
CENTER 45.0MHz SPAN 100.0kHz
#RES BW 1.0kHz #VBW 10Hz SWP 30.0 sec

IF output spectrum

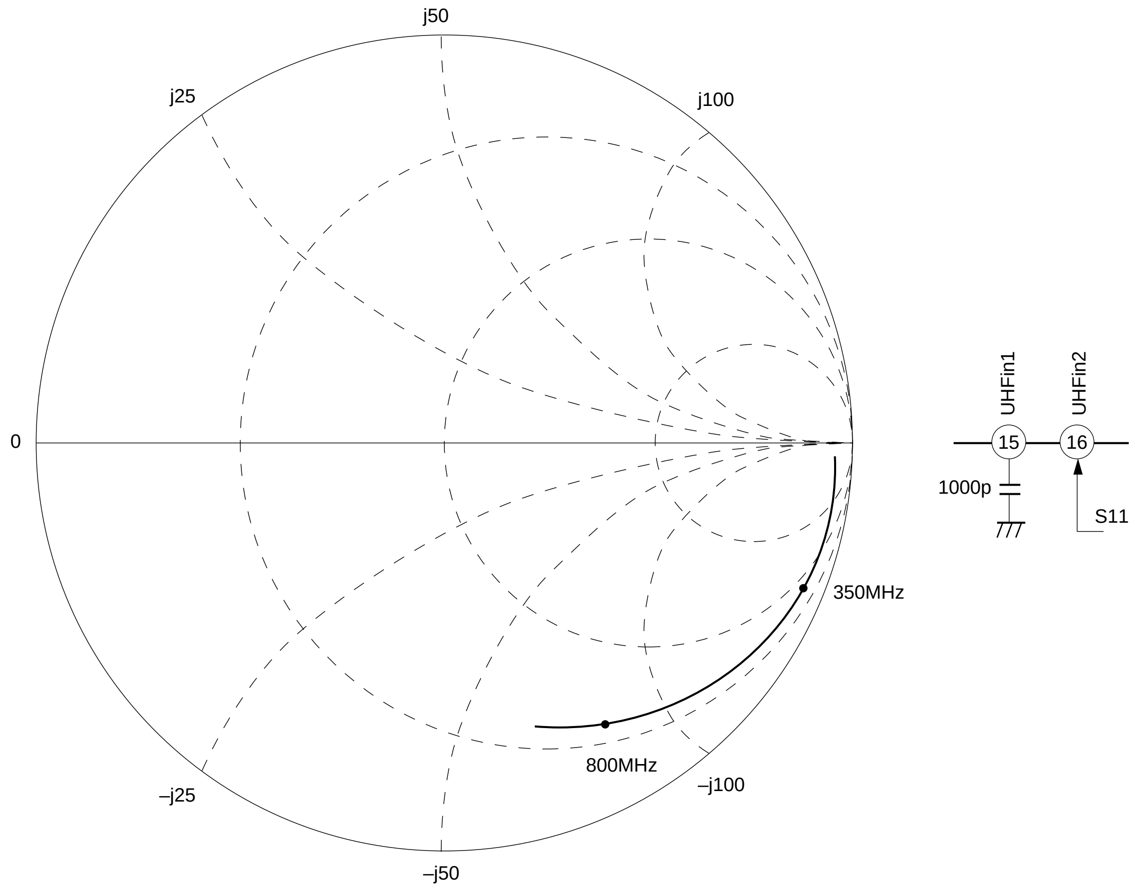


CENTER 45.0 270MHz
#RES BW 1.0kHz
#VBW 10Hz
SPAN 100.0kHz
SWP 30.0 sec

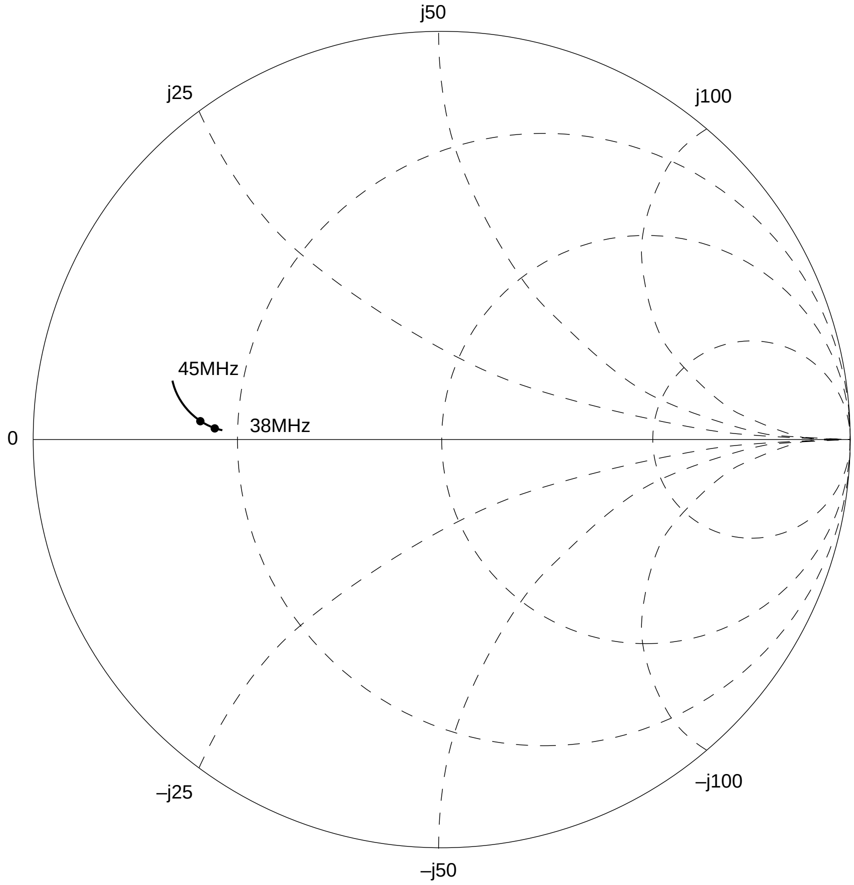
VHF Input Impedance



UHF Input Impedance

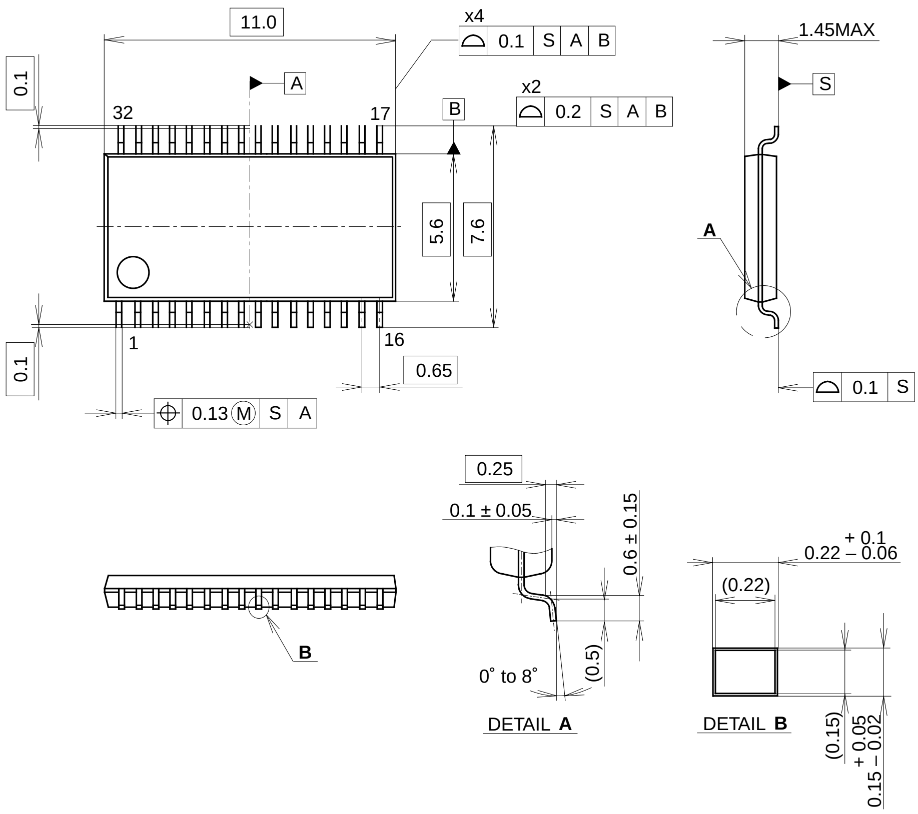


IF Output Impedance



Package Outline Unit : mm

32PIN SSOP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	SSOP-32P-L01
EIAJ CODE	SSOP032-P-0056
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUMA PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g