MOTOROLA
Semiconductor Products Sector Engineering Bulletin

Order Number EB346/D:
Rev. 2
4/20/2001

Functional Differences Between DSP56302 and DSP56309 (formerly DSP56302A)

Contents

1 Purpose of this Document

To meet the increasing demands for higher performance and lower power consumption, an advanced DSP56302 has been designed; it is was formerly known as DSP302A; it is now designated DSP56309. The new part is designed to be a functional replacement for the DSP56302. This document summarizes the differences between the DSP56302 and the DSP56309.

2 Differences Overview

The primary functional differences between the DSP56302 and the DSP56309 are due to inherent differences between the two design technologies. **Table 1.** compares the two chips.

Table 1. Functional Comparison of DSP56302 and DSP56309

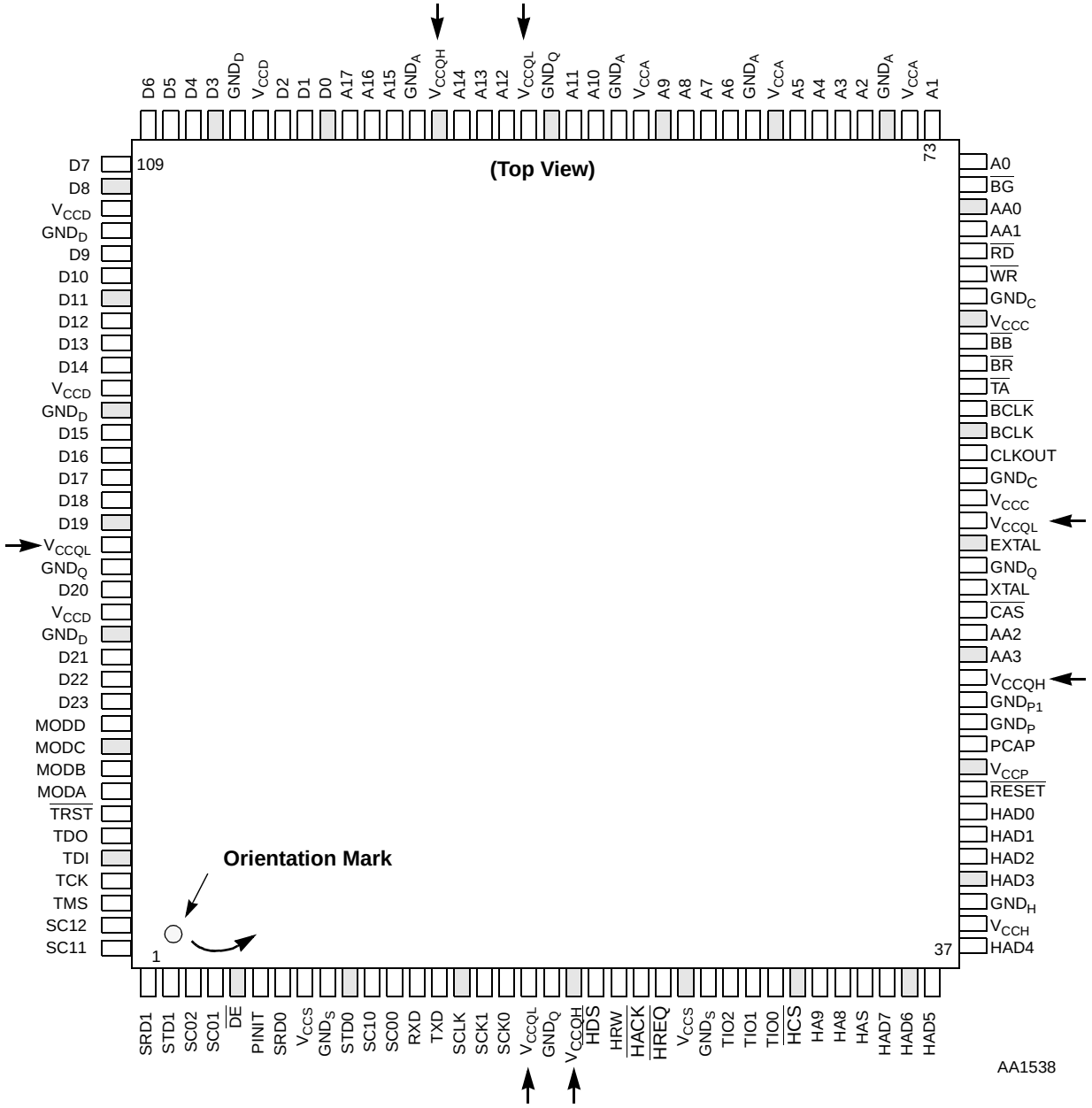
Feature	DSP56302	DSP56309
Operating frequency	≤ 66 MHz down to 0 Hz	≤ 100 MHz down to 0 Hz
Technology	0.5 micron	Sub 0.4 micron
Input power	V_{CC} = 3.0-3.6 V combined core and I/O power and ground	Split power: Core V_{CC} (3.0–3.6 V currently) I/O V_{CC} (3.0–3.6 V currently) A pinout change is required to support the split power configuration. See **Section 3** for more information and a description of the pinout change for the 144-pin TQFP package.
I/O pins	5 V tolerant (exceptions: see data sheet)	Tolerant up to 3.6 V
Package	144-pin TQFP	144-pin TQFP or 196-pin PBGA
PLL input capacitor (C_{PCAP})	Uses the following rules: For MF ≤ 4: C_{PCAP} = [(500 × MF) – 150] pF For MF > 4: C_{PCAP} = (690 × MF) pF	Uses the following rules: For MF ≤ 4: C_{PCAP} = [(680 × MF) – 120] pF For MF > 4: C_{PCAP} = (1100 × MF) pF
Operating modes		See **Table 3** for details.
Other functionality	All memory, control functions, and peripherals are identical. Refer to the *DSP56309 Technical Data Sheet* (order by DSP56309/D) for a detailed description of these features.	

3 Input Power Changes

One method to increase the operating frequency of an integrated circuit is to “shrink” the die (that is, reduce the die dimensions, both linearly and vertically). Reducing the die size can yield additional benefits, such as a reduction of power consumption, but can also result in other functional changes. The DSP56309 is a “shrink” of the DSP56302. This die size reduction enables the DSP56309 to achieve higher operating frequencies. Decreasing the die size, however, requires a reduction of the thickness of the oxide dielectrics, which also reduces the maximum allowable voltages across some oxides within the die. To support future “shrinks” of the DSP56309 while maximizing system level compatibility, Motorola has elected to separate the power supply networks on the die. This split allows the I/O pins to operate over a voltage range which is different from that used by the core digital logic. Although the initial release of this product specifies the same voltage ranges for the I/O pins and the core logic, future versions of the DSP56309 or its derivatives are likely to have reduced core logic V_{CC} requirements (for example, 2.5 V and lower voltages) while the I/O levels use a higher level (for example, 3.3 V). This allows Motorola to continue aggressively to “shrink” the device, while preserving the ability to maintain system level compatibility.

The split-power design requires a modification in the chip pinout. A top view of the DSP56309 TQFP package is shown in **Figure 1**. **Table 2** lists the pin differences between the DSP56302 and the DSP56309.

Note: The power input for the core logic is designated V_{CCQ} for the DSP56302. For the DSP56309, the independent core logic input voltage is designated V_{CCQL}, while the independent I/O input voltage is designated V_{CCQH}. V_{CCQL} should be connected to the core input power supply. V_{CCQH} and all other input power (V_{CCA}, V_{CCC}, V_{CCD}, V_{CCH}, V_{CCP}, and V_{CCS}) should be connected to the external input power supply.



Note: Arrows (→) indicate the pins that are different from the DSP56302, as listed in **Table 2.** on page 4.

Figure 1. DSP56309 Thin Quad Flat Pack (TQFP), Top View

Table 2. Pin Differences between DSP56302 and DSP56309 (144-pin TQFP package)

Pin	Pin Name	
	DSP56302	DSP56309
18	V_{CCQ}	V_{CCQL}
20	NC	V_{CCQH}
49	NC	V_{CCQH}
56	V_{CCQ}	V_{CCQL}
91	V_{CCQ}	V_{CCQL}
95	V_{CCA}	V_{CCQH}
126	V_{CCQ}	V_{CCQL}
V_{CCQ} = input voltage for core logic V_{CCQL} = independent input voltage for core logic NC = not connected V_{CCQH} = independent input voltage for I/O lines V_{CCA} = voltage for external address lines Unlisted pins are the same for both chips.		

A pinout for the 196-pin PBGA package is included in the DSP56309 Technical Data Sheet. This package will include the split power configuration described for the 144-pin TQFP package.

4 I/O Power Changes

The DSP56302 supports 5 V inputs for its peripherals. Complete requirements are described in the DSP56302 Technical Data Sheet.

The DSP56309 supports 3.3 V inputs. Detailed voltage requirements are included in the DSP56309 Technical Data Sheet.

5 PLL Input Capacitor (C_{PCAP})

The process change results in a changed requirement for computing the size of C_{PCAP}, the capacitor used with the PCAP input. **Table 1** lists the new formulas for computing the value of this input capacitor for the DSP56309.

6 Operating Modes

The operating modes of the DSP56302 are documented in the DSP56302 User's Manual. **Table 3.** documents the operating modes of the DSP56309. Modes that differ from those of the DSP56302 are highlighted in the table.

Table 3. DSP56309 Operating Modes

Mode	MODD	MODC	MODB	MODA	Reset Vector	Description
0	0	0	0	0	$C00000	Expanded mode
1	0	0	0	1	$FF0000	Reserved
2	0	0	1	0	$FF0000	Reserved
3	0	0	1	1	$FF0000	Reserved
4	0	1	0	0	$FF0000	Reserved
5	0	1	0	1	$FF0000	Reserved
6	0	1	1	0	$FF0000	Reserved
7	0	1	1	1	$FF0000	Reserved
8	1	0	0	0	$008000	Expanded mode
9	1	0	0	1	$FF0000	Boot from byte-wide memory
A	1	0	1	0	$FF0000	Boot from SCI
B	1	0	1	1	$FF0000	Reserved
C	1	1	0	0	$FF0000	HI08 bootstrap in ISA mode
D	1	1	0	1	$FF0000	HI08 bootstrap in HC11 non-multiplexed mode
E	1	1	1	0	$FF0000	HI08 bootstrap in 8051 multiplexed bus mode
F	1	1	1	1	$FF0000	HI08 bootstrap in MC68302 mode

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