1Mx8 STATIC RAM CMOS, MODULE

FEATURES

- 1Mx8 bit CMOS Static RAM
  - Access Times 20 through 35ns
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- High Density Packaging
  - JEDEC Aproved, Revolutionary Pinout
  - 36 Pin DIP, No. 179
- Single +5V (±10%) Supply Operation

DESCRIPTION

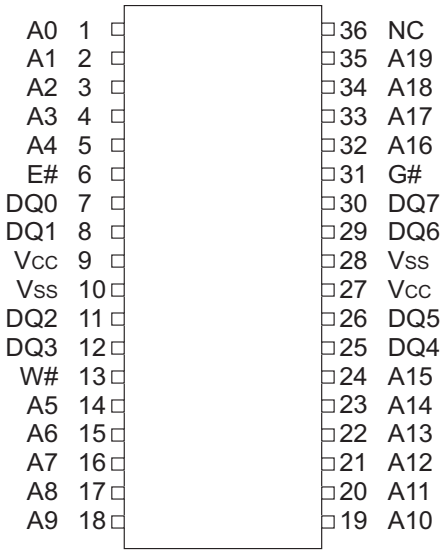
The EDI8F81026C is an 8Mb CMOS Static RAM based on two 512Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR4) substrate.

The EDI8F81026C is packaged in a 36 pin DIP and features the JEDEC approved, revolutionary pinout.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

Fully asynchronous, the EDI8F81026C requires no clocks or refreshing for operation.

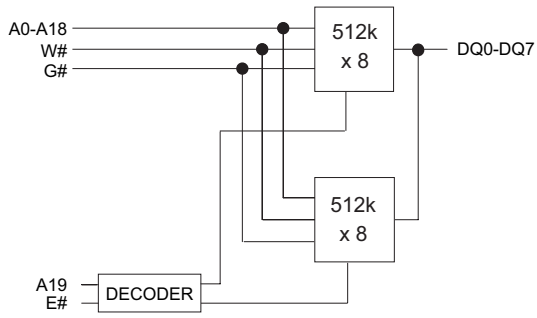
Pin Configuration



Pin Description

A0-A19	Address Inputs
E#	Chip Enable
W#	Write Enable
G#	Output Enable
DQ0-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Block Diagram



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature T_A (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	2.0 Watt
Output Current	20 mA

* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL =35pF

(Note: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL=5pF)

TRUTH TABLE

G#	E#	W#	Mode	Output	Power
X	H	X	Standby	High Z	I_{CC2}, I_{CC3}
H	L	H	Output Deselect	High Z	I_{CC1}
L	L	H	Read	D_{OUT}	I_{CC1}
X	L	L	Write	D_{IN}	I_{CC1}

CAPACITANCE

(f=1.0MHz, V_{IN}=V_{CC} or Vss)

Parameter	Sym	Max	Unit
Address Lines	CI	12	pF
Data Lines	CD/Q	43	pF
Chip Enable Line	CC	10	pF
Write and Output Enable Lines	CW	32	pF

These parameters are sampled, not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Typ*	Max	Units
Operating Power Supply Current	I_{CC1}	W#, E# = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle	—	212	120	mA
Standby (TTL) Power Supply Current	I_{CC2}	E ≥ V_{IH}, V_{IN} ≤ V_{IL}, V_{IN} ≥ V_{IH}	—	35	50	mA
Full Standby Power Supply Current (CMOS)	I_{CC3}	E ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN}≤ 0.2V	—	20	12	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	—	—	±10	µA
Output Leakage Current	I_{LO}	V I/O = 0V to V_{CC}	—	—	±10	µA
Output High Voltage	V_{OH}	I_{OH} =-4.0mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

*Typical: T_A = 25°C, V_{CC} = 5.0V

AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	20		25		35		ns
Address Access Time	t_{AVQV}	t_{AA}		20		25		35	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		20		25		35	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}		10		12		15	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	3		3		3		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		8		10		12	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{LOZ}	3		3		3		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}		8		10		12	ns

Note 1: Parameter guaranteed, but not tested

FIGURE 2 – READ CYCLE 1 - W# HIGH, G#, E# LOW

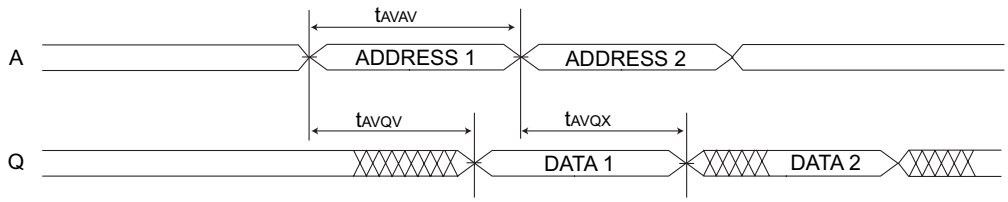
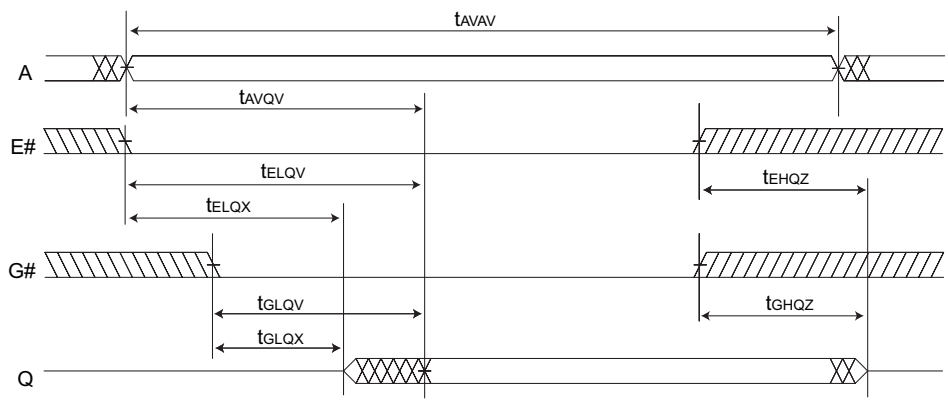


FIGURE 3 – READ CYCLE 2 - W# HIGH



AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	20		25		35		ns
Chip Enable to End of Write	t_{ELWH}	t_{CW}	15		20		30		ns
	t_{ELEH}	t_{CW}	15		20		30		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	15		15		20		ns
	t_{AVEH}	t_{AW}	15		15		20		ns
Write Pulse Width	t_{WLWH}	t_{WP}	15		20		25		ns
	t_{WLEH}	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		0		ns
	t_{EHAX}	t_{WR}	0		0		0		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
	t_{EHDX}	t_{DH}	0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	8	0	12	0	15	ns
Data to Write Time	t_{DVWH}	t_{DW}	12		15		20		ns
	t_{DVEH}	t_{DW}	12		15		20		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

FIGURE 4 – WRITE CYCLE 1 - W# CONTROLLED

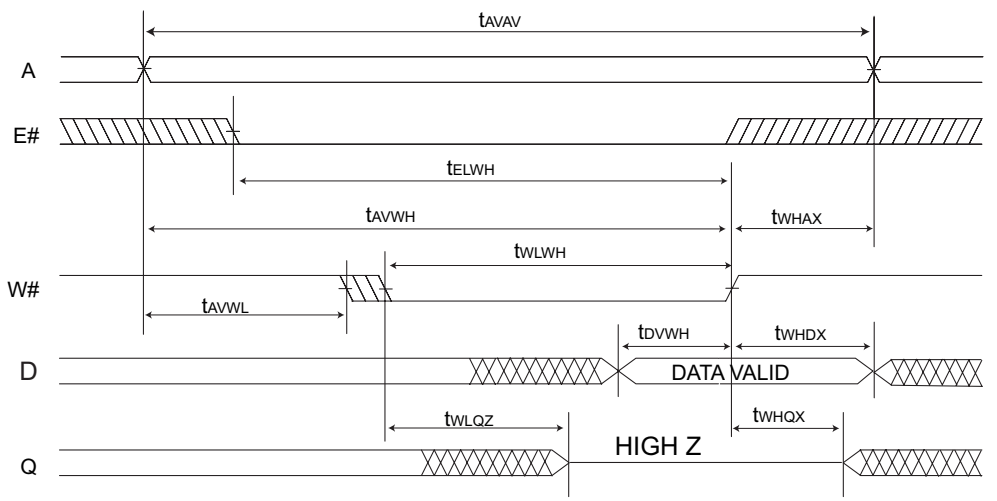
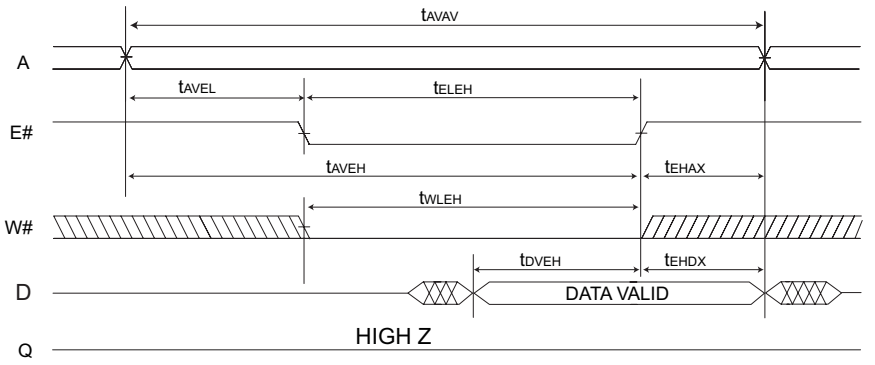


FIGURE 5 – WRITE CYCLE 2 E# CONTROLLED



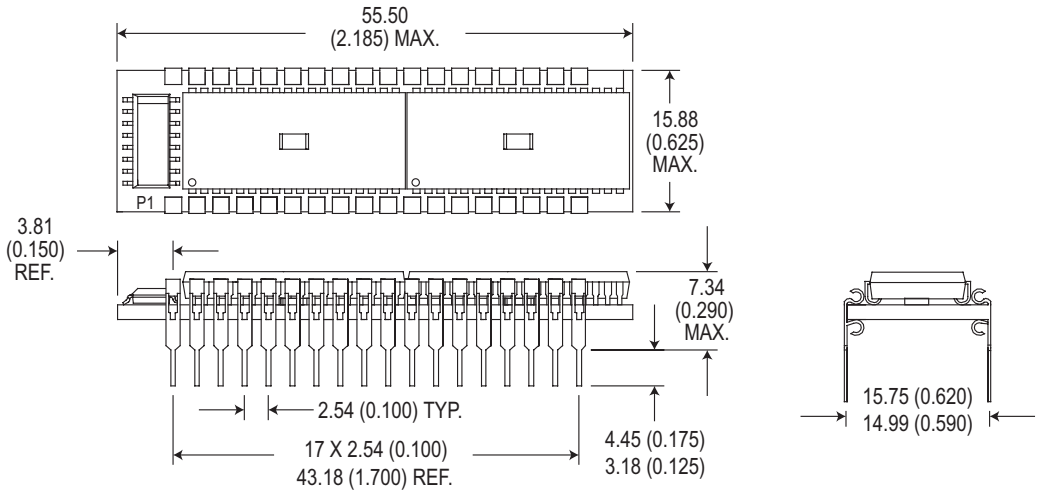
ORDERING INFORMATION

Standard Power	Speed (ns)	Package No.	Height*
EDI8F81026C20M6C	20	179	7.37 (0.290")
EDI8F81026C85M6C	25	179	7.37 (0.290")
EDI8F81026C35M6C	35	179	7.37 (0.290")

Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I,
eg. EDI8F81026C20M6C becomes EDI8F81026C20M6I.

PACKAGE DESCRIPTION

Package No. 179: 36 Pin Dual-in-line Package



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES).

Document Title

1M X 8 SRAM Module

Revision History

Rev #	History	Release Date	Status
Rev 0	0.1 Updated datasheet format	7-2004	Final
	0.2 Added package height		
	0.3 Added metric measurements		
	0.4 Added new document title page		