December 1995, Rev. G FN7020

## Low Power, 70MHz Buffer Amplifier

The EL2001 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patented buffer has a -3dB bandwidth of 70MHz, and delivers 100mA, yet draws only 1.3mA of supply current. It typically operates from ±15V power supplies but will work with as little as ±5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. A typical example is a general purpose op amp output current booster where the buffer must have sufficiently high bandwidth and low phase shift at the maximum frequency of the op amp.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: Elantec's Processing, Monolithic Integrated Circuits.

## Ordering Information

| PART NUMBER | TEMP. RANGE | PACKAGE | PKG. NO. |
|---|---|---|---|
| EL2001ACN | 0°C to +75°C | PDIP | MDP0031 |
| EL2001CM | 0°C to +75°C | 20-Pin SOL | MDP0027 |
| EL2001CN | 0°C to +75°C | PDIP | MDP0031 |

## Features

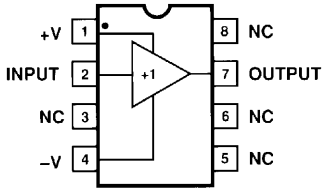
- 1.3mA supply current
- 70MHz bandwidth
- 2000V/µs slew rate
- Low bias current, 1µA typical
- 100mA output current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range ±5V to ±15V
- No thermal runaway

## Applications

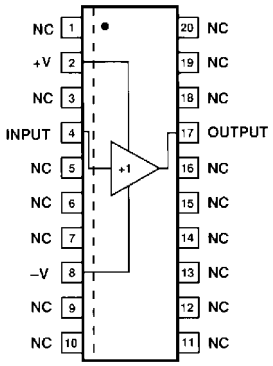
- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Low standby current systems

## Pinouts

**EL2001**
**(8-PIN PDIP, SO)**
TOP VIEW




**EL2001**
**(20-PIN SOL)**
TOP VIEW




NOTE: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,833,424, 4,827,223 U.K. Patent No. 2217134

## Absolute Maximum Ratings ($T_A$ = 25°C)

$V_S$ Supply Voltage (V+ - V-) . . . . . ±18V or 36V
$V_{IN}$ Input Voltage . . . . . ±15V or $V_S$
*If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the applications section for more information.*

$I_{IN}$ Input Current (See above note) . . . . . ±50 mA
$P_D$ Power Dissipation . . . . . See Curves
*The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.*

Output Short Circuit Duration . . . . . Continuous
*A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.*
$T_A$ Operating Temperature Range . . . . . 0°C to +75°C
$T_J$ Operating Junction Temperature. . . . . 150°C
$T_{ST}$ Storage Temperature . . . . . -65°C to +150°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## Electrical Specifications $V_S$ = ±12V, $R_S$ = 50Ω, unless otherwise specified

| PARAMETER | DESCRIPTION | TEST CONDITIONS | | | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | $V_{IN}$ | LOAD | TEMP | MIN | TYP | MAX | |
| $V_{OS}$ | Offset Voltage | 0 | ∞ | 25°C | -10 | 2 | I | mV |
| | | | | $T_{MIN}$, $T_{MAX}$ | -15 | | +15 | mV |
| | | 0 | ∞ | 25°C | -30 | 2 | +30 | mV |
| | | | | $T_{MIN}$, $T_{MAX}$ | -40 | | +40 | mV |
| $I_{IN}$ | Input Current | 0 | ∞ | 25°C | -3 | 1 | +3 | µA |
| | | | | $T_{MIN}$, $T_{MAX}$ | -6 | | +6 | µA |
| | | 0 | ∞ | 25°C | -5 | 1 | +5 | µA |
| | | | | $T_{MIN}$, $T_{MAX}$ | -10 | | +10 | µA |
| $R_{IN}$ | Input Resistance | ±12V | 100Ω | 25° | 1 | 8 | | MΩ |
| | | | | $T_{MIN}$, $T_{MAX}$ | 0.5 | | | MΩ |
| $A_{V1}$ | Voltage Gain | ±12V | ∞ | 25°C | 0.990 | 0.998 | | V/V |
| | | | | $T_{MIN}$, $T_{MAX}$ | 0.985 | | | V/V |
| $A_{V2}$ | Voltage Gain | ±10V | 100Ω | 25°C | 0.83 | 0.93 | | V/V |
| | | | | $T_{MIN}$, $T_{MAX}$ | 0.80 | | | V/V |
| $A_{V3}$ | Voltage Gain with $V_S$ = ±5V | ±3V | 100Ω | 25°C | 0.82 | 0.89 | | V/V |
| | | | | $T_{MIN}$, $T_{MAX}$ | 0.79 | | | V/V |
| $V_O$ | Output Voltage Swing | ±12V | 100Ω | 25°C | ±10 | ±11 | | V |
| | | | | $T_{MIN}$, $T_{MAX}$ | ±9.5 | | | V |
| $R_{OUT}$ | Output Resistance | ±2V | 100Ω | 25°C | | 10 | 15 | Ω |
| | | | | $T_{MIN}$, $T_{MAX}$ | | | 18 | Ω |
| $I_{OUT}$ | Output Current | ±12V | (Note 1) | 25°C | ±100 | ±160 | | mA |
| | | | | $T_{MIN}$, $T_{MAX}$ | ±95 | | | mA |
| $I_S$ | Supply Current | 0 | ∞ | 25°C | | 1.3 | 2.0 | mA |
| | | | | $T_{MIN}$, $T_{MAX}$ | | | 2.5 | mA |
| PSRR | Supply Rejection (Note 2) | 0 | ∞ | 25°C | 60 | 75 | | dB |
| | | | | $T_{MIN}$, $T_{MAX}$ | 50 | | | dB |
| $t_R$ | Rise Time | 0.5V | 100Ω | 25°C | | 4.2 | | ns |
| $t_D$ | Propagation Delay | 0.5V | 100Ω | 25°C | | 2.0 | | ns |

**Electrical Specifications** $V_S$ = ±12V, $R_S$ = 50Ω, unless otherwise specified **(Continued)**

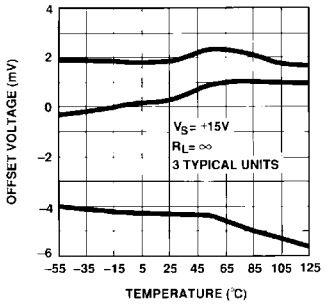
| PARAMETER | DESCRIPTION | TEST CONDITIONS | | | LIMITS | | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | $V_{IN}$ | LOAD | TEMP | MIN | TYP | MAX | |
| SR | Slew Rate (Note 3) | ±10V | 100Ω | 25°C | 1200 | 2000 | | V/µs |

NOTES:

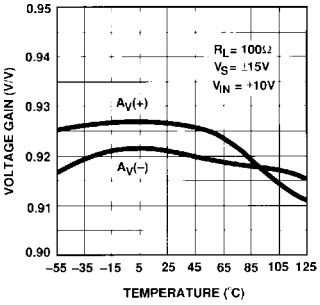
1. Force the input to +12V and the output to +10V and measure the output current. Repeat with -12 $V_{IN}$ and -10V on the output.
2. $V_{OS}$ is measured at $V_S$+ = +4.5V, $V_S$- = -4.5V and at $V_S$+ = +18V, $V_S$- = -18V. Both supplies are changed simultaneously.
3. Slew rate is measured between $V_{OUT}$ = +5V and -5V.

## *Typical Performance Curves*

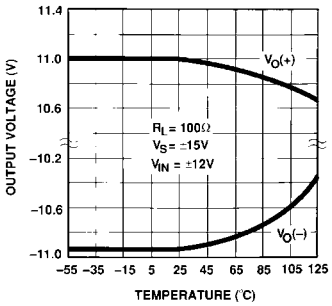
**Offset Voltage vs Temperature**



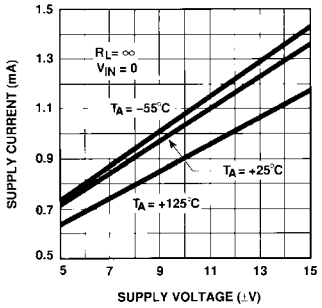

**Voltage Gain vs Temperature**



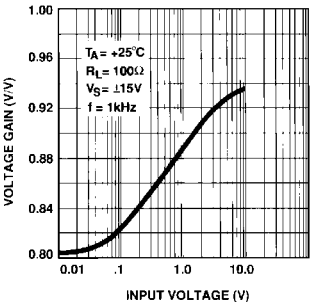

**Output Voltage Swing vs Temperature**



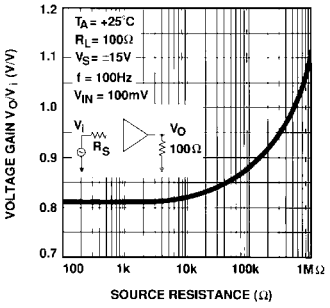

**Supply Current vs Supply Voltage**



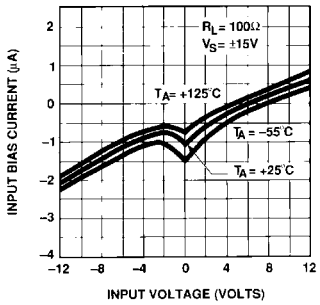

**Voltage Gain vs Input Voltage**



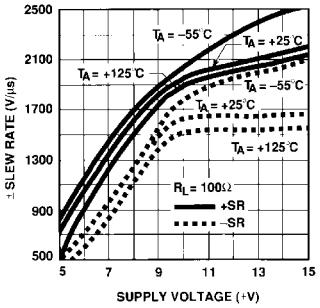

**Voltage Gain vs Source Resistance**



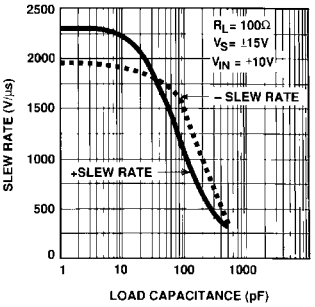

**Input Bias Current vs Input Voltage**




**±Slew Rate vs Supply Voltage**

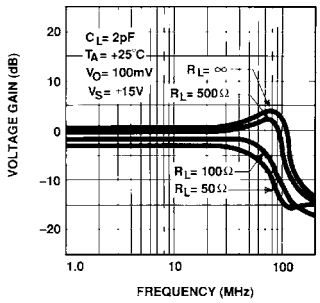



**±Slew Rate vs Capacitive Load**

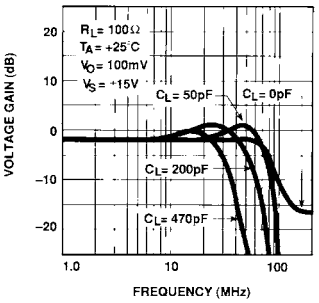


## Typical Performance Curves (Continued)

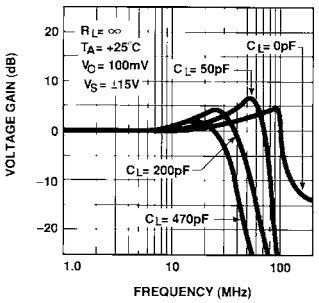
**Voltage Gain vs Frequency for Various Resistive Loads**



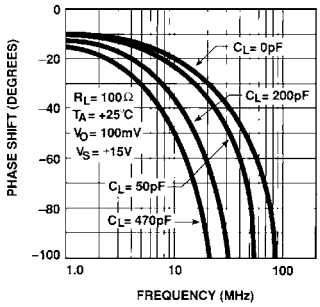

**Voltage Gain vs Frequency for Various Capacitive Loads; $R_L$ = 100Ω**



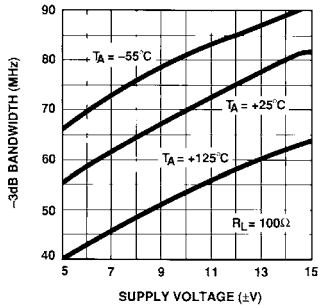

**Voltage Gain vs Frequency for Various Capacitive Loads; $R_L$ = ∞**



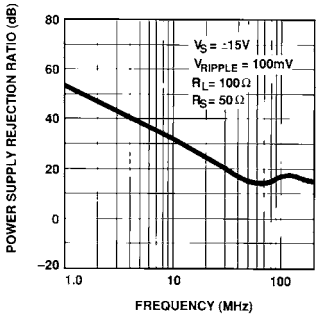

**Phase Shift vs Frequency for Various Capacitive Loads**



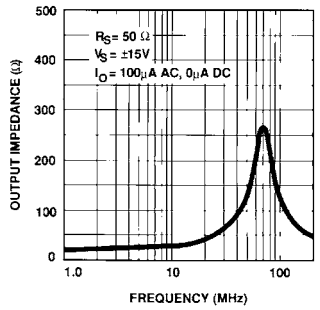

**-3dB Bandwidth vs Supply Voltage**



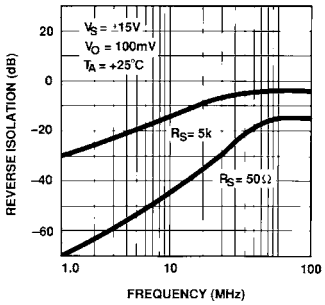

**Power Supply Rejection Ratio vs Frequency**



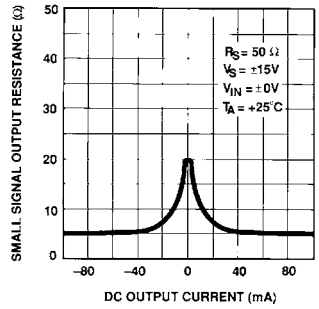

**Output Impedance vs Frequency**



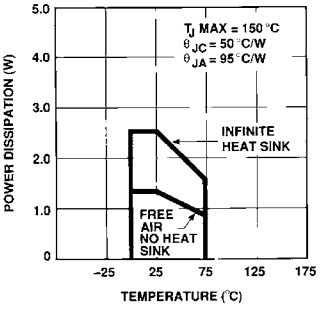

**Reverse Isolation vs Frequency**



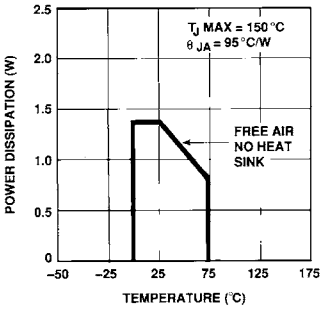

**Small Signal Output Resistance vs Output Current**



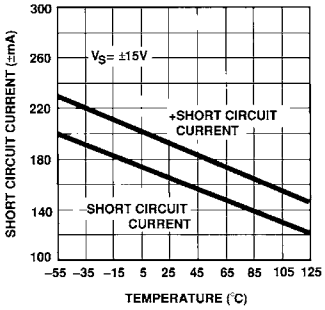

**8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature**




**20-Pin SOL Maximum Power Dissipation vs Ambient Temperature**

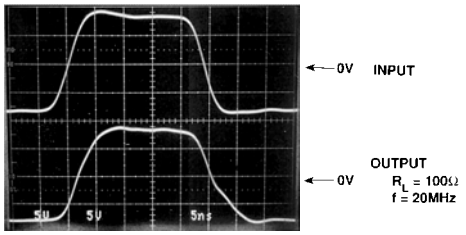



**Short Circuit Current vs Temperature**

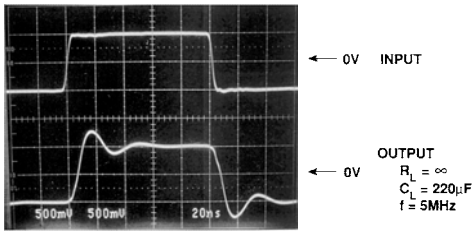


## Typical Performance Curves (Continued)

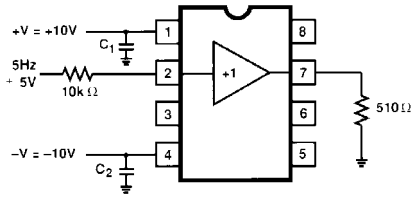
Large Signal Response



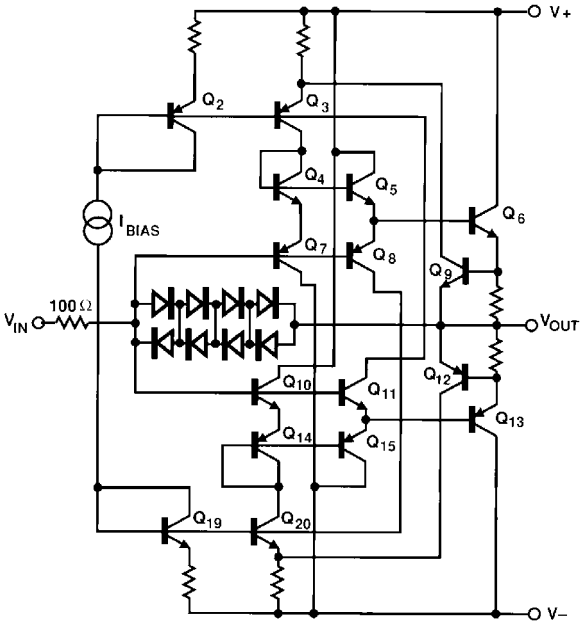

Small Signal Response




## Burn-In Circuit




## Simplified Schematic




## Application Information

The EL2001 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2001 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2001's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000V/µs slew rates with 100Ω loads possible with very low supply current.

### Power Supplies

The EL2001 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). It is not necessary to use equal split value supplies. For example -5V and +12V would be excellent for signals from -2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1µF tantalum capacitor with short pins should be used for both supplies.

### Input Characteristics

The input to the EL2001 looks like a resistance in parallel with about 3.5pF in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage ($R_{IN}$) is affected by the output load, beta and the internal boost. $R_{IN}$ can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50mA. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above ±7.5V differential input to output, additional series resistance should be added.

### Source Impedance

The EL2001 has good input to output isolation. When the buffer is not used in a feedback loop, capactive and resistive sources up to 1Mb present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances ($R_S$ > 100kΩ), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

## EL2001 Macromodel

```
*Connections:   +input
*                |     +Vsupply
*                |     |     -Vsupply
*                |     |     |     output
*                |     |     |     |
.subckt M2001  2     1     4     7
* Input Stage

el 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 9pF
rc 11 12 100
cc 12 0 4pF
e2 13 0 12 0 1.0
* Output stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 1
r3 19 7 1
i1 1 14 0.9mA
i2 15 4 0.9mA
* Bias Current
iin+ 2 0 1uA
* Models
.model qn npn(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.model qp pnp(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.ends
```