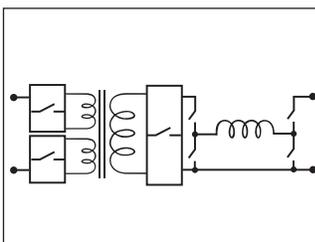


V•I Chip PFM Power Factor Module

F3D480T20A

- Input: rectified 120/240 Vac sinusoidal
- Output: 48 Vdc programmable
- Output power: Up to 200 W
- 4,242 Vdc reinforced insulation
- 90% efficiency
- 375 W/in³ power density
- Low profile: 0.25"
- Surface mount J Lead package
- Meets EN 61000-3-2 harmonic current limits



©



Actual Size

Product Description

The PFM (Power Factor Module) is a V•I Chip power component that converts a rectified 120/240 Vac line to an isolated, regulated DC voltage programmable from 26 V to 48 V. Rated at 200 W, the PFM meets EN61000-3-2 harmonic current limits and is available in a double VIC package measuring only 1.69" (43,0) x 1.26" (32,0) x 0.25" (6,2). The PFM power density is 375 W/in³.

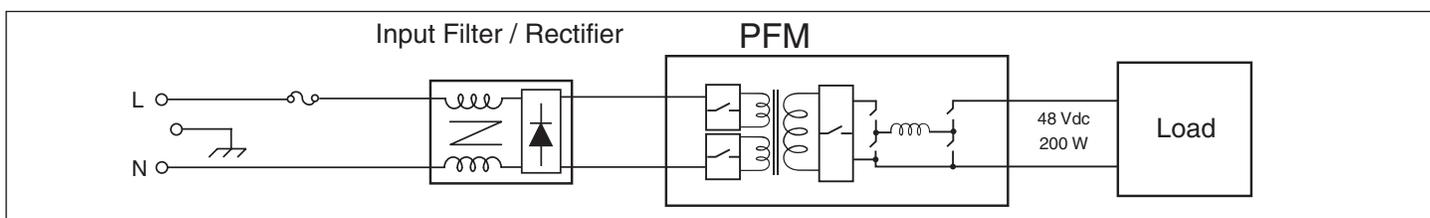
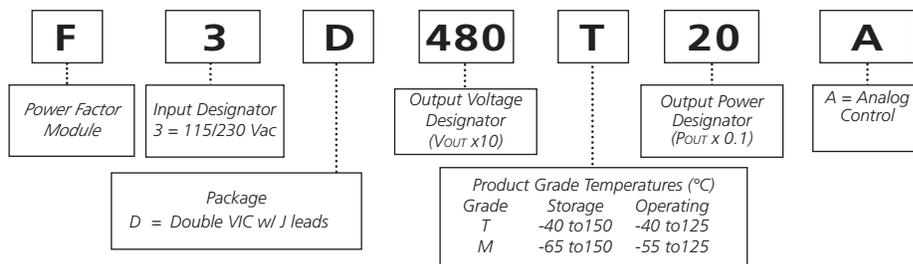
The PFM is the front-end V•I Chip for AC-DC power systems. It requires only a rectifier, input filter and an output capacitor to provide a high density, power factor corrected, 200 W power supply. The high operating frequency and soft switching allow miniaturization of power train components and make EMI filter components smaller than those required by lower frequency, hard switching converters. Output energy storage is accomplished at SELV levels providing packaging and interconnect flexibility not available with conventional AC Front Ends.

PFMs may be paralleled with power sharing for added power or redundancy in single or three phase systems. The output voltage can be programmed to meet the requirements of system loads and/or additional downstream conversion devices such as Vicor's Pre Regulator Modules (PRMs) and Voltage Transformation Modules (VTMs).

Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Input voltage (+IN to -IN)				
Operating	90	264	Vrms	Rectified AC sinusoidal
Non-operating	0	450	Vdc	100 ms
Input voltage slew rate		25	V/μs	
PC to -IN	-0.3	7	Vdc	
BV to -IN	-0.3	50	Vdc	
PR to -OUT	-0.3	7	Vdc	
SC	-0.3	1.5	Vdc	
Output voltage (+OUT to -OUT)	-0.5	55	Vdc	
Output current		6	A	
Dielectric withstand (input to output)		4,242	Vdc	Reinforced insulation 1 Min
Temperature				
Operating junction	-55	125	°C	M-Grade
Storage	-65	150	°C	M-Grade
Case peak temperature during reflow		225	°C	MSL 3
Case peak temperature during reflow		245	°C	MSL 6

Part Numbering



PRELIMINARY

Electrical characteristics (Conditions: 25°C case, 75% rated load and specified input voltage range unless otherwise specified.)

Rectified AC Input Source The PFM operates from a full bridge rectified AC line with the following characteristics:

Parameter	Min	Typ	Max	Unit	Note
Source voltage low range	90		132	Vrms	The PFM is not designed to support output load when the input is 132 to 175 Vrms
Source voltage high range	180		264	Vrms	
Source frequency range	47		63	Hz	

Input (Operating from AC input source)

Parameter	Min	Typ	Max	Unit	Note
Undervoltage shut down		82	85	Vrms	Source voltage
Overvoltage shut down	265	275		Vrms	Source voltage
Power factor	0.94				47 – 63 Hz
Inrush current			5	A pk	

Output

Parameter	Min	Typ	Max	Unit	Note
Set point	47.5	48.0	48.5	Vdc	Output may be trimmed down from factory set point via external trim resistor. See page 4, SC pin
Output voltage trim range	26	48	48.0	Vdc	
Output current	0		4.1	A	Vout = 48 Vdc
Output power	0		200	W	Vout = 48 Vdc see Fig. 22 for heat sink information
OVP set point	56		58	Vdc	
Line regulation		0.3	1	%	
Load regulation		0.5	1	%	
Efficiency	88	90		%	120 Vrms 75% load
No load power dissipation			0.75	W	Meets Energy Star no load limit
Current share accuracy		5	10	%	
Switching frequency ripple		240	300	mV pk-pk	~1.2 MHz with 10 µF ceramic bypass capacitance
Line frequency ripple		350	750	mV rms	With 10,000 µF output capacitor
		1.12	2.0	V pk-pk	
Start up time					
From application of power	2.0	2.5	5.0	S	No overshoot
Dynamic response					
Voltage deviation		6		%	Of Vout
Recovery time		500		mS	
Output capacitance	1,500	2,200	10,000	µF	Required for PFC. Output ripple is a function of output and hold-up capacitance. See Fig.8 for hold-up time.
Hold-up capacitance	1,500	2,200	10,000	µF	
Short circuit protection		5.5	6.0	A	Current limited

PRELIMINARY

Electrical (cont.) (conditions: 25°C case, 75% rated load and specified input voltage range)

Control Pins (See page 4 for pin description)

Pin	Min	Typ	Max	Unit	Note
BV (Bias Voltage)	-0.5		48	V	Referenced to -IN
PC (Primary Control)					
DC voltage	4.8	5.0	5.2	Vdc	Referenced to -IN
Module disable threshold	2.3	2.4		Vdc	
Module enable threshold		2.5	2.6	Vdc	
Disable hysteresis		100		mV	
Current limit	2.0	2.7	3.5	mA	PC pulled low
Analog control					
PR (Parallel Port)					
Voltage	0.6		7.5	V	Referenced to SG, see PR pin pg.4
Source current	1			mA	
External capacitance			100	pF	
SC (Secondary Control)					
Voltage	1.23	1.24	1.25	Vdc	Referenced to SG
Internal capacitance		1.0		nF	
External capacitance			0.7	μF	

General

Parameter	Min	Typ	Max	Unit	Note
Over temperature shut down	125	130	135	°C	Junction temperature
Junction-to-case thermal impedance		0.6		°C/W	
Case-to-ambient thermal impedance		2.3		°C/W	46 mm x 46 mm x11mm heatsink #31474 with 300 LFM
Dielectric withstand	4,242			Vdc	Input to output
Insulation resistance	10			M ohms	Input to output
Capacitance			110	pF	Input to output
Leakage current			30	μA	
Line fuse Rating	250		4	Vac A	Always ascertain and observe applicable safety, regulatory and agency specifications
Mechanical					
Weight		1.0 / 30		oz / g	
Length		1.69 / 43		in / mm	
Width		1.26 / 32		in / mm	
Height		0.25 / 6.2		in / mm	
Reflow parameters					
Resistance to cleaning	IEC 68-2-45 XA		Water		+55 ±5°C
Solvents	Method 1		Isopropyl alcohol		+35 ±5°C
Agency approvals (pending)		cTÜVus CE			UL/CSA 60950, EN 60950 Low voltage directive

Electromagnetic Compatibility (configured as illustrated in Fig. 18)

Harmonic currents	EN 61000-3-2, Amendment 14	See Fig. 11
Line disturbance / immunity	EN 61000-4-11	Interruptions and brownouts
Transient / surge immunity	EN 61000-4-5	2 kV–50 μs line or neutral to earth 1 kV–50 μs line to neutral
Conducted emissions	EN 55022, Level B	With filter (see Fig. 18)
Flicker / inrush	EN 61000-3-3	

Pin/Control Functions

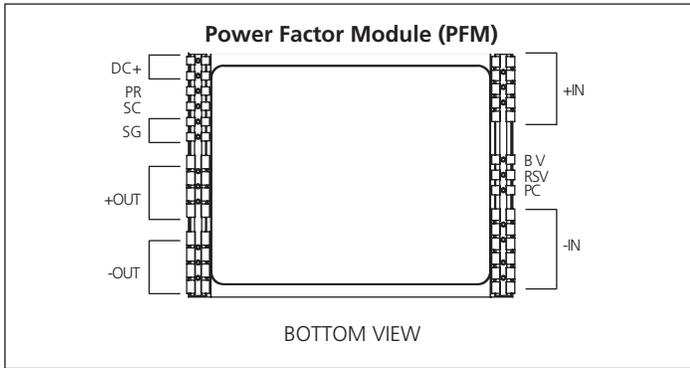


Figure 1— PFM pin out

Primary side

+IN / -IN – DC voltage

The PFM operates from a full wave rectified AC voltage within the limits shown on page 2. PFMs have internal over / undervoltage lockout functions that prevent operation outside of the specified rms input range. PFMs will turn on when the input voltage rises above its undervoltage lockout. If the input voltage exceeds the overvoltage lockout, PFMs will shut down until the overvoltage fault clears.

BV - bias voltage

A 47 μ F 50 V electrolytic capacitor must be connected between this port and -IN to provide energy storage for the primary bias circuit.

RSV – reserved

PC – primary control

The PFM voltage output is enabled when the PC pin is open circuit (floating). To disable the PFM output voltage, the PC pin is pulled to -IN. Open collector optocouplers, transistors, or relays can be used to control the PC pin. When using multiple PFMs in a high power array, the PC ports should be tied together to synchronize their turn on.

Secondary side

DC+

A hold-up capacitor should be connected between this port and SG to provide output hold-up in the event of an input power failure. For 10 ms hold-up at full load, a 2,200 μ F 50 V electrolytic capacitor is recommended. DC+ should not be back driven.

PR – parallel port (analog control models only)

The PR port signal, which is proportional to the PFM output power, supports current sharing among PFMs. To enable current sharing, PR ports should be interconnected. No bypass capacitance should be used when interconnecting PR ports and steps should be taken to minimize stray capacitance and noise coupling into this line (e.g. by minimizing the width of PR port interconnect traces that lay over, or in proximity to, signal grounds or power / ground planes). The PR port is referenced to SG.

SC – secondary control (analog control models only)

The output voltage may be programmed, margined or trimmed down by connecting a voltage source or resistor between the SC port and SG port. The slew rate of the output voltage may be reduced by controlling the rate-of-rise for the voltage at the SC port (e.g. to limit inrush into a capacitive load).

The following expression should be used to calculate the required set point resistor value. No resistor is required if the user desires a nominal 48 V output.

$$R = (V_o / (48 - V_o)) 30.1 \text{ k}\Omega$$

Where: R = the set point resistor

V_o = the desired output voltage set point

Example:

V_o	R
42 V	211 k Ω
36 V	90.3 k Ω

Table 1

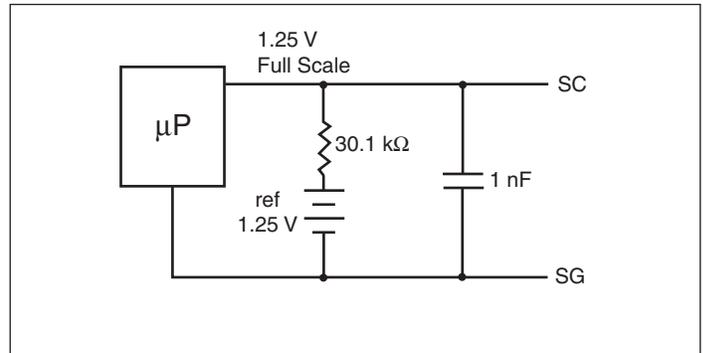


Figure 2—Functional block diagram

SG – signal return (analog control models only)

This port should be used as reference for the SC, PR, and DC+ ports. Care must be taken to insure there are no low impedance paths between -OUT and SG. Such a path could allow current to bypass the internal current sense resistor.

+ OUT / -OUT – voltage output

These ports provide the isolated DC output voltage. The -OUT pin is separated from the SG (Signal Return) pin by the internal current sensing resistor.

Safety consideration

Care must be exercised to insure appropriate spacing, clearance and creepage distances are maintained between line side terminals and secondary SELV terminals.

PFM Theory of Operation

The PFM power-processing module consists of two major functional blocks: an Adaptive Voltage Transformation Module (VTM) that interfaces directly to the rectified line followed by a microprocessor controlled Post Regulator Module (PRM). In contrast to offline power factor correction topologies, input current shaping and energy storage are accomplished on the secondary side of the isolation boundary.

Adaptive VTM

The Adaptive VTM acts as a nearly ideal DC-to-DC transformer. It accepts the rectified AC input from the power source, configures its step down ratio, or K factor, based on the magnitude of the input voltage, and produces an isolated DC output that instantaneously tracks the input. The Adaptive VTM configures itself by paralleling input cells in low voltage input mode or by series configuration of input cells in high voltage input mode. Operating over the worldwide AC mains, the Adaptive VTM reduces the voltage variation applied to the PRM stage from 3 to1 to 1.5 to1. This reduction in voltage range allows greater performance and economy than would be possible without Adaptive Transformation, which is enabled by Vicor's proprietary class of Cascaded Topologies.

The PFM uses a Sine Amplitude Converter (SAC) Cascaded Topology providing zero-voltage/zero-current switching through a low Q resonant circuit to eliminate switching losses. The SAC can be operated efficiently at high frequencies, typically in the 3 MHz range. The high operating frequency allows miniaturization of power train components with a commensurate increase in converter power density. High operating frequency and soft switching makes EMI filtering components smaller than those required by lower frequency, hard switching converters.

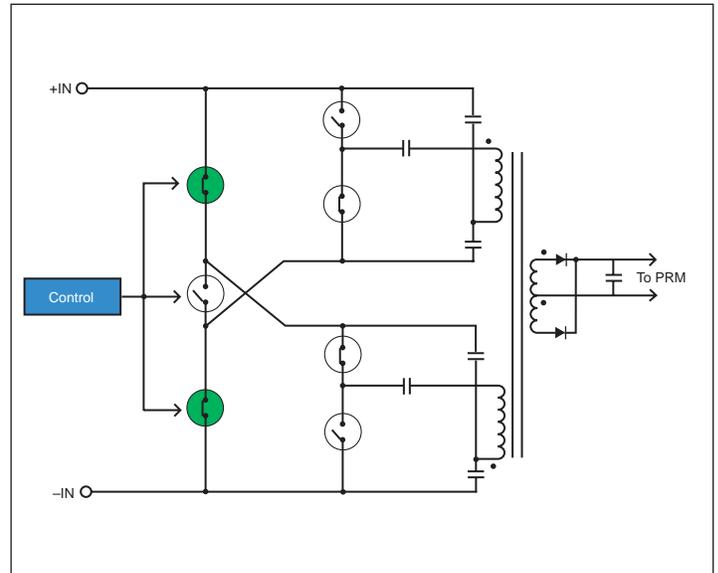


Figure 3— 120 Vac input configuration

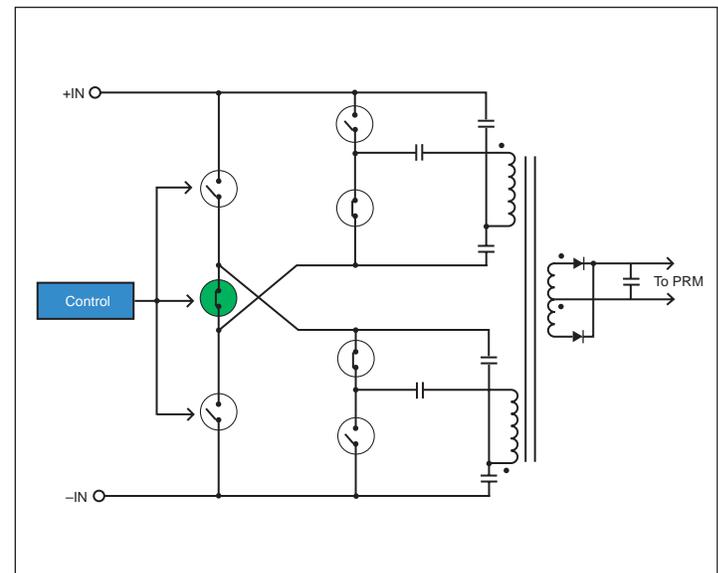


Figure 4— 240 Vac input configuration

PFM Theory of Operation cont.

PRM with PFC

The output of the VTM drives the PFC/PRM. The PFC/PRM (Figure 5) is a microprocessor controlled, high-efficiency, zero-voltage switching buck-boost regulator providing output voltage regulation and input current shaping. The input voltage, isolated and adaptively transformed by the VTM, and the PRM's output voltage and output current are sampled by the microprocessor. The processor uses a digital algorithm to develop a control signal used to simultaneously regulate the output voltage and shape the module input current, providing harmonic current reduction. This control signal is fed to the switch management ASIC. This provides proper switch timing, maintaining zero-voltage switching under all operating conditions. Energy storage is accomplished outside the PFM by means of an output capacitor that may be sized to meet the user's hold up requirements.

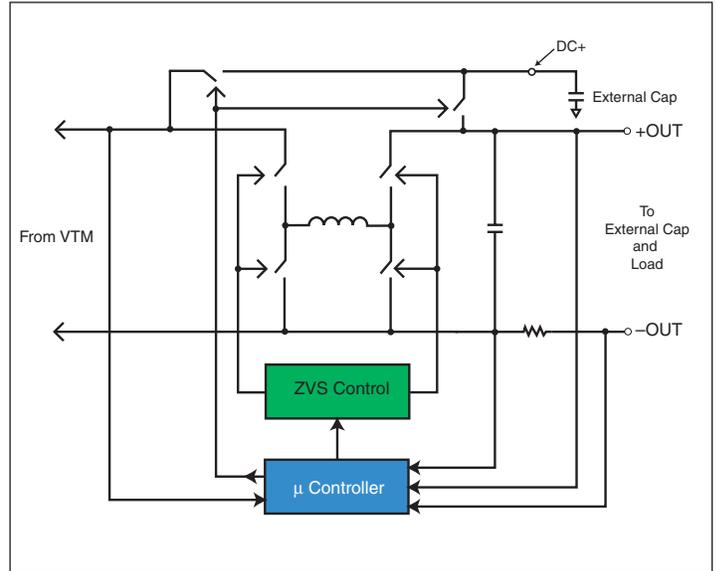


Figure 5 — The PRM with PFC

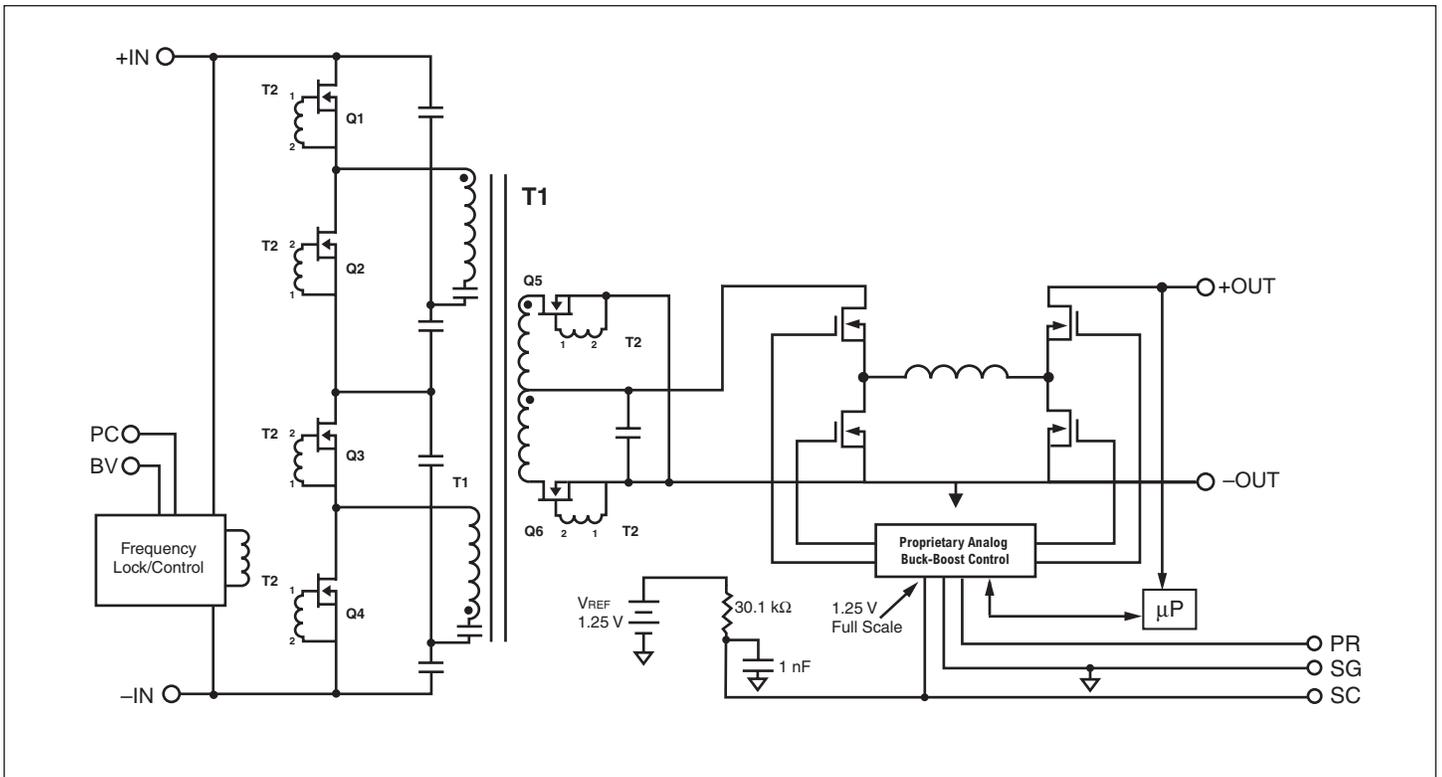


Figure 6 — Functional block diagram of the PFM

PRELIMINARY

Electrical (conditions: 25°C case, 75% rated load and specified input voltage range)

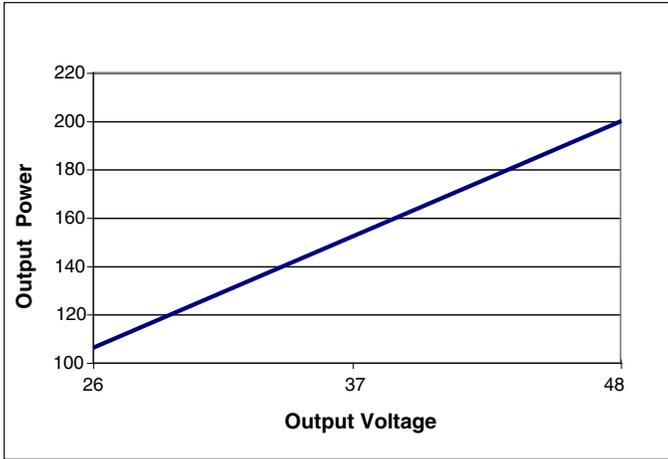


Figure 7 — Output power rating vs. trimmed output voltage

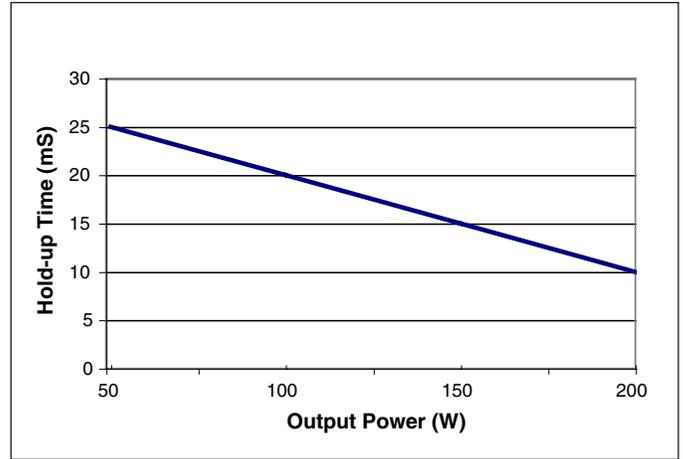


Figure 8 — Hold up time with 2,200 µF output and hold-up capacitors with 48 Vdc output

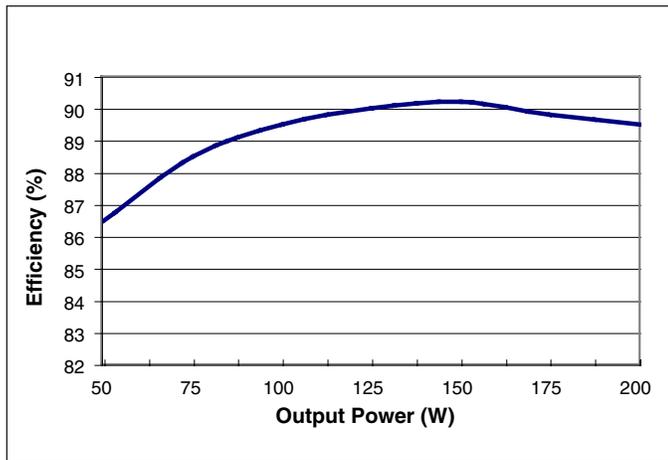


Figure 9 — Efficiency vs. Output Power (120 Vrms, 48 Vdc)

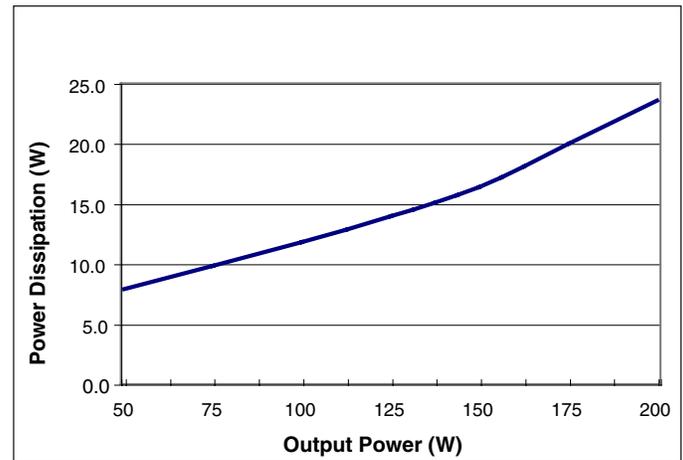


Figure 10 — Power Dissipation vs. Output Power (120 Vrms, 48 Vdc)

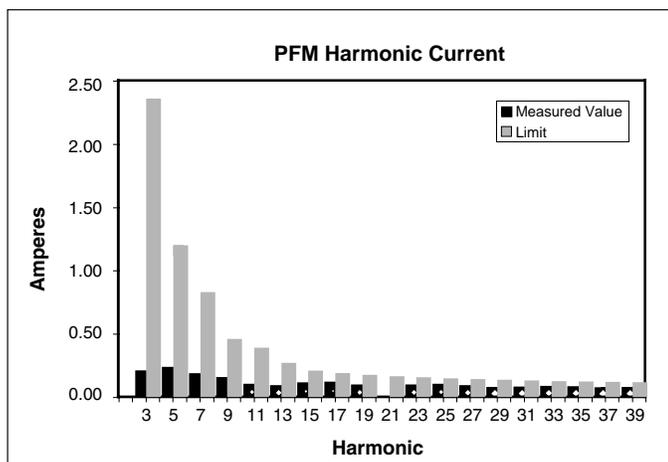


Figure 11 — Harmonic Current vs. EN61000-3-2 limits (115 Vrms 180 W Out)

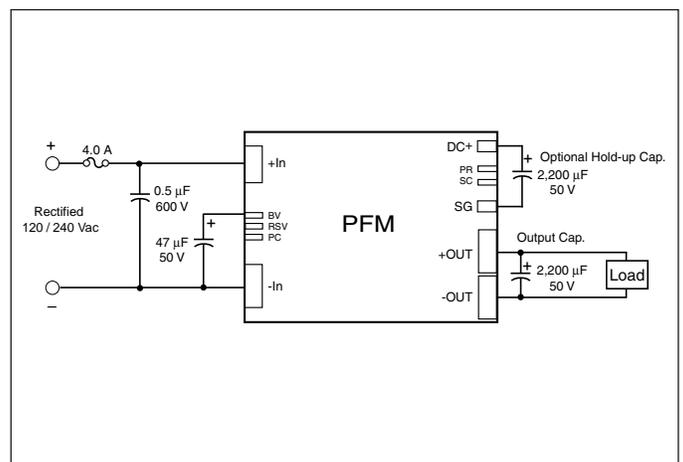


Figure 12 — PFM test circuit

Electrical (cont.)

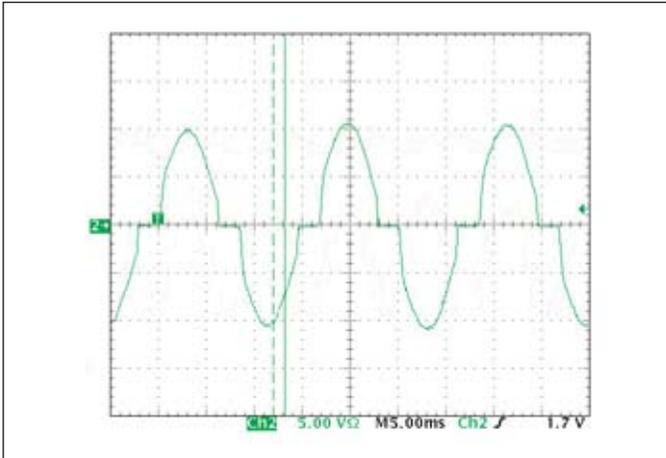


Figure 13 — Typical Input Current (230 Vrms 200 W Out)

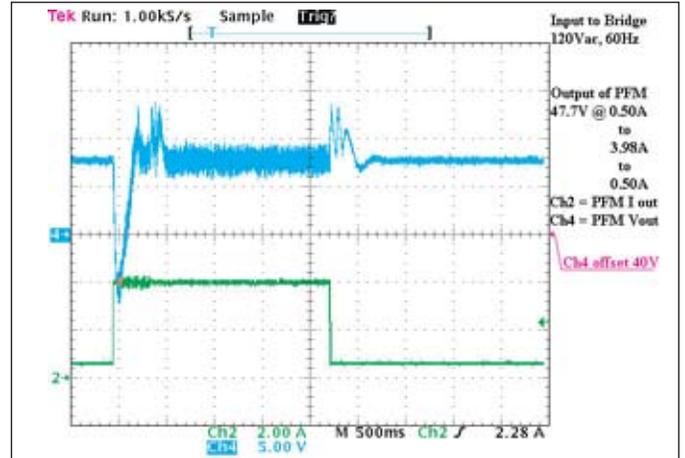


Figure 14 — Transient Response Input: 120 Vac, 60 Hz
Output step load: 10% to 90% to 10%

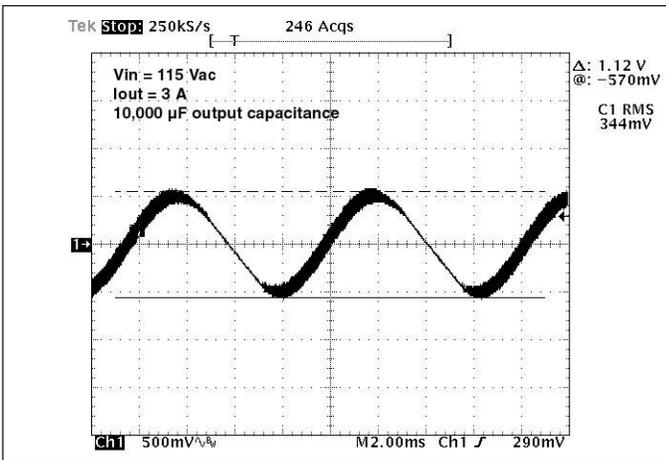


Figure 15 — Output Ripple (Line frequency)

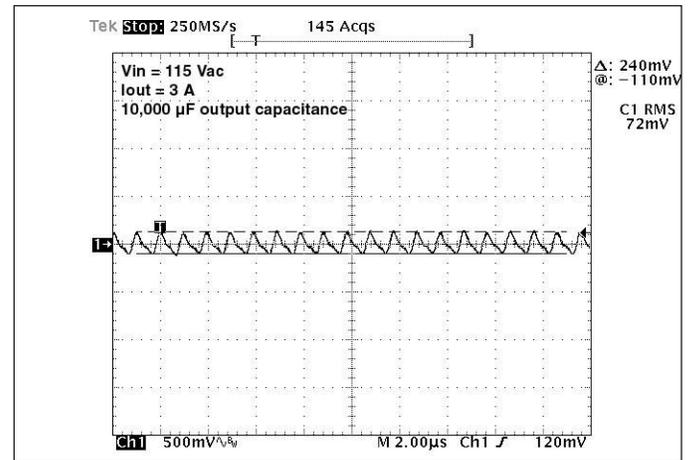


Figure 16 — Output Ripple (Switching frequency)

Electrical (cont.)

PFM Applications

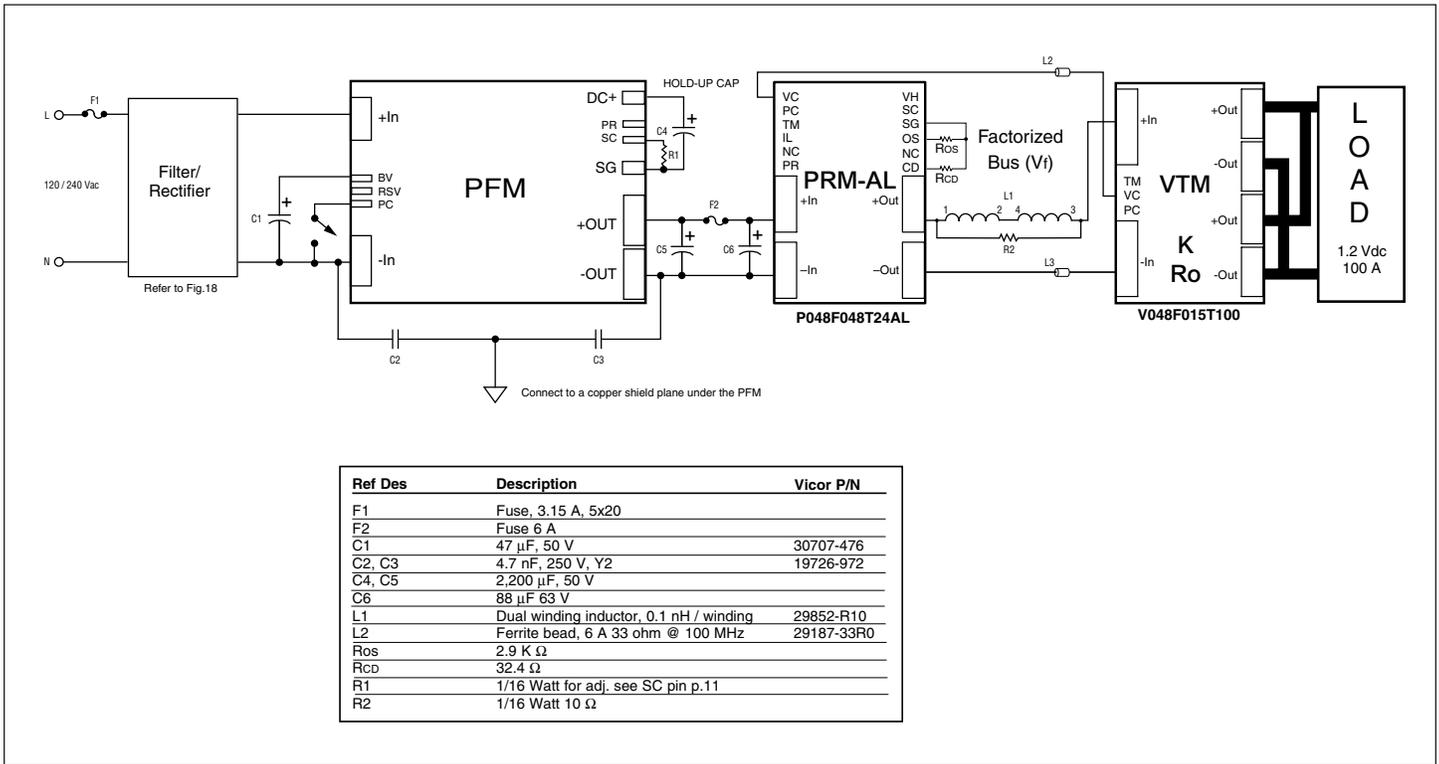


Figure 17 — Typical FPA (Factorized Power Architecture) from the wall plug to the point of load. See PRM data sheet (P048F048T24AL) for other output voltage / current options.

Electrical (cont.)

Input Filter and Rectifier

The circuit shown below provides AC line rectification, transient suppression, and conducted emissions filtering to comply with standards imposed by the EMC (Electromagnetic Compatibility) directive. These include the transient immunity standard EN 61000-4-5, and the conducted emissions standard EN 55022, level B.

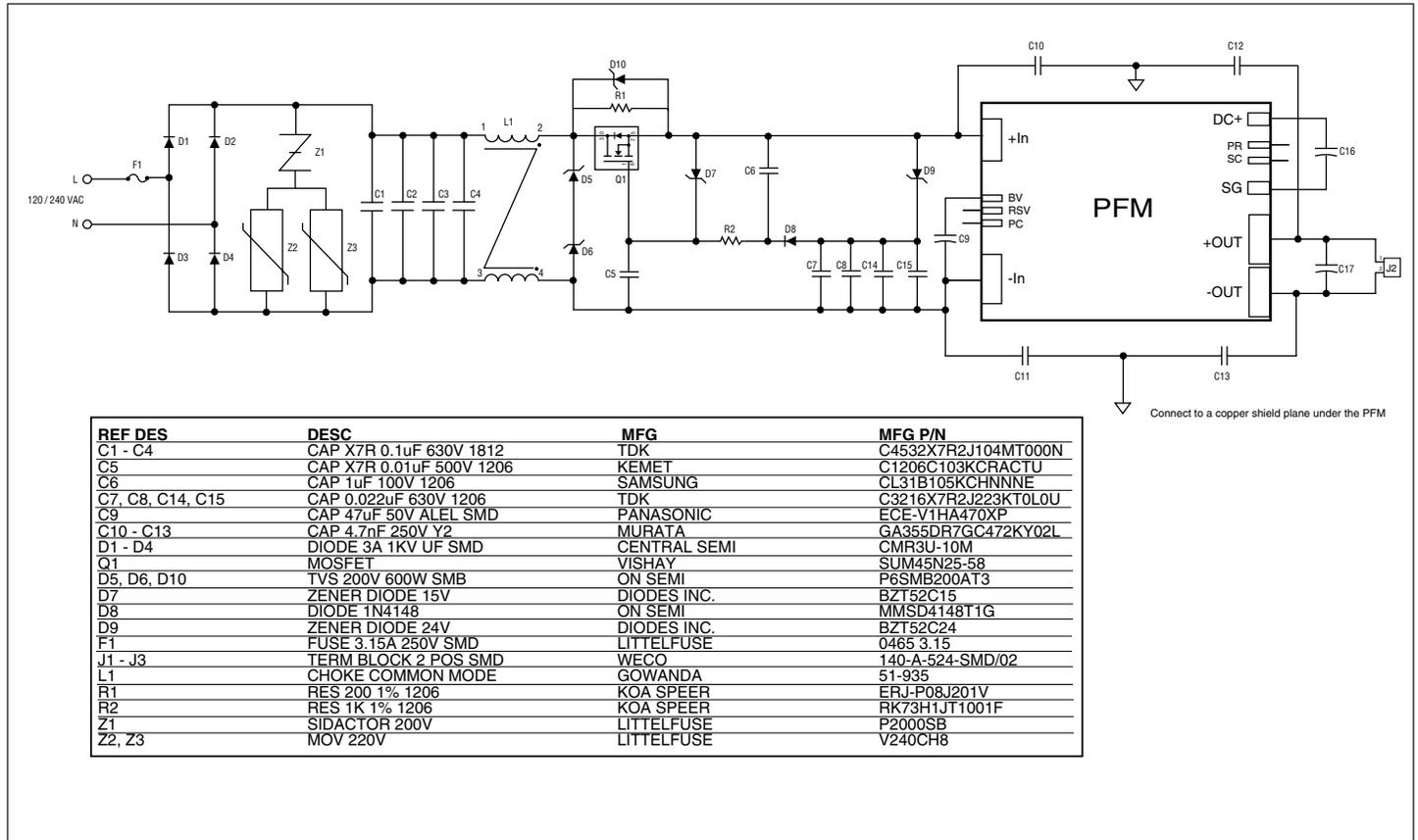


Figure 18 — Typical application circuit

PFM Evaluation Board

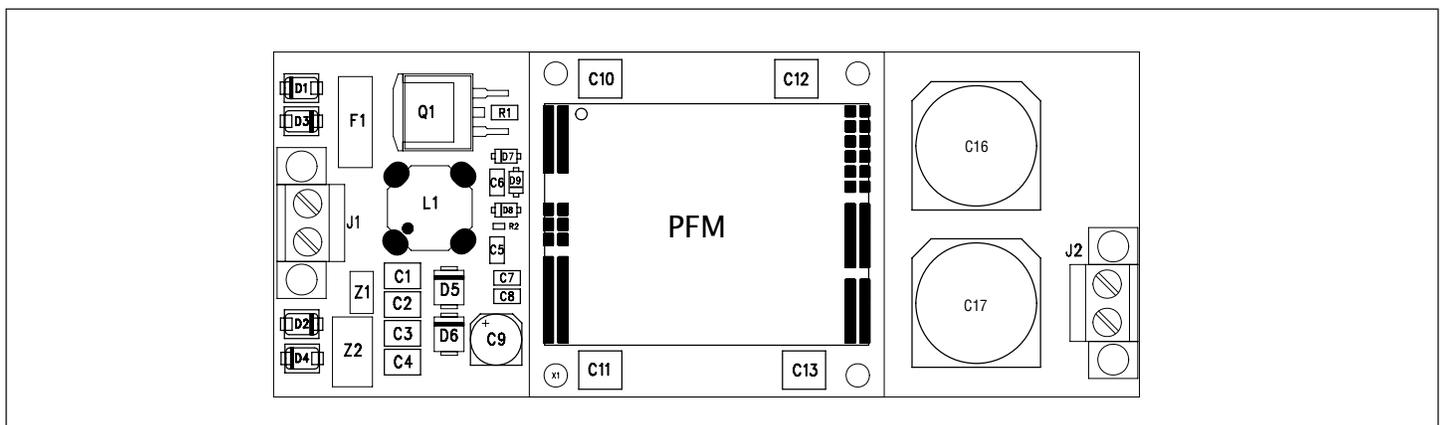


Figure 19 — The PFM evaluation board shown (actual size) above illustrates the layout and compact size of a complete AC to 48 Vdc, 200 Watt front end power supply using the PFM.

Electrical (cont.)

PFM Applications

The block diagram below shows an example of a Factorized Power system from the wall plug to the point-of-load. The PFM directly regulates a primary high power output through a VTM to provide voltage division. A secondary output is independently regulated with a PRM. Auxiliary outputs are derived through a V•I Chip Bus Converter Module (BCM) and non-isolated POL converters.

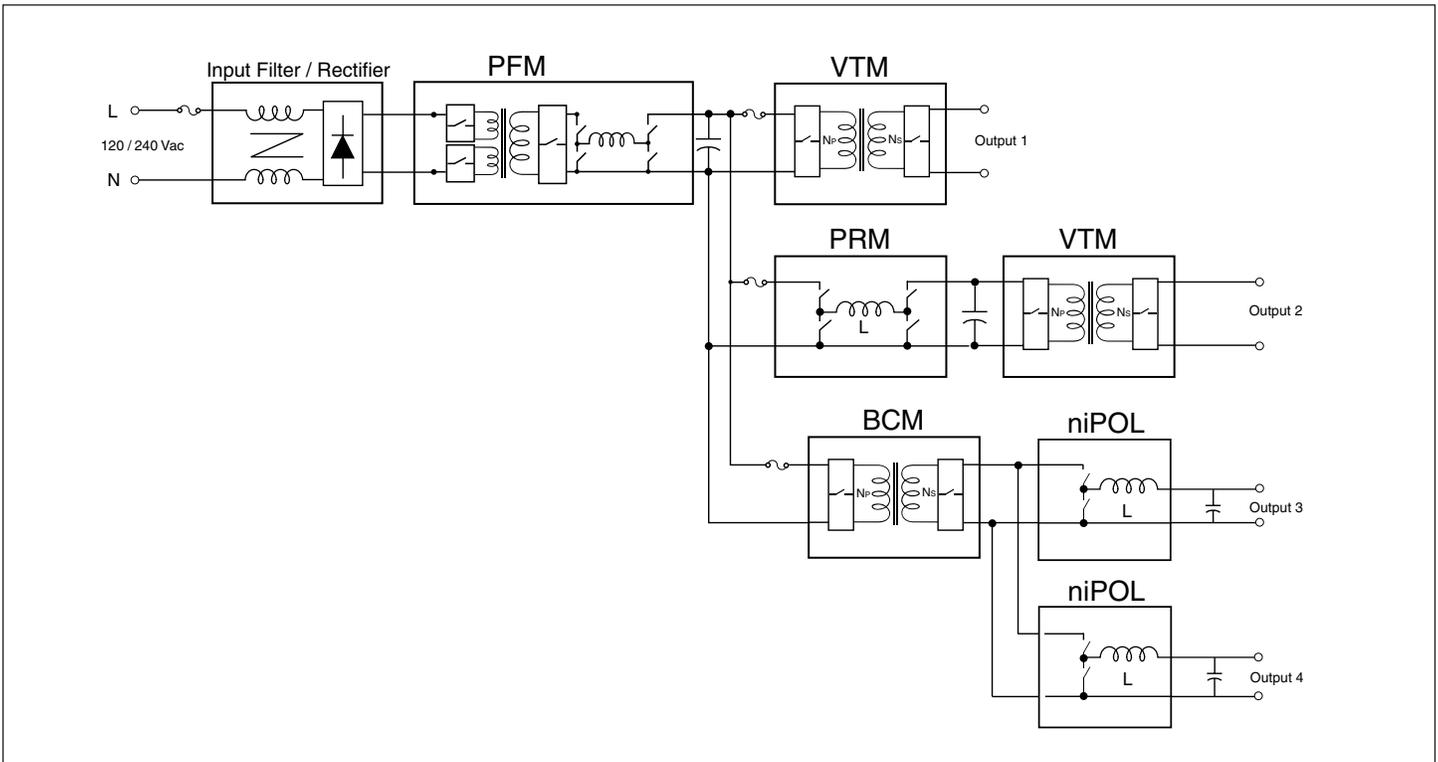


Figure 20 — Typical application using Factorized Power Architecture (FPA)

The block diagram below shows a 400 Watt PFC front end with two PFMs in a parallel configuration. Higher power can be achieved by adding additional PFMs.

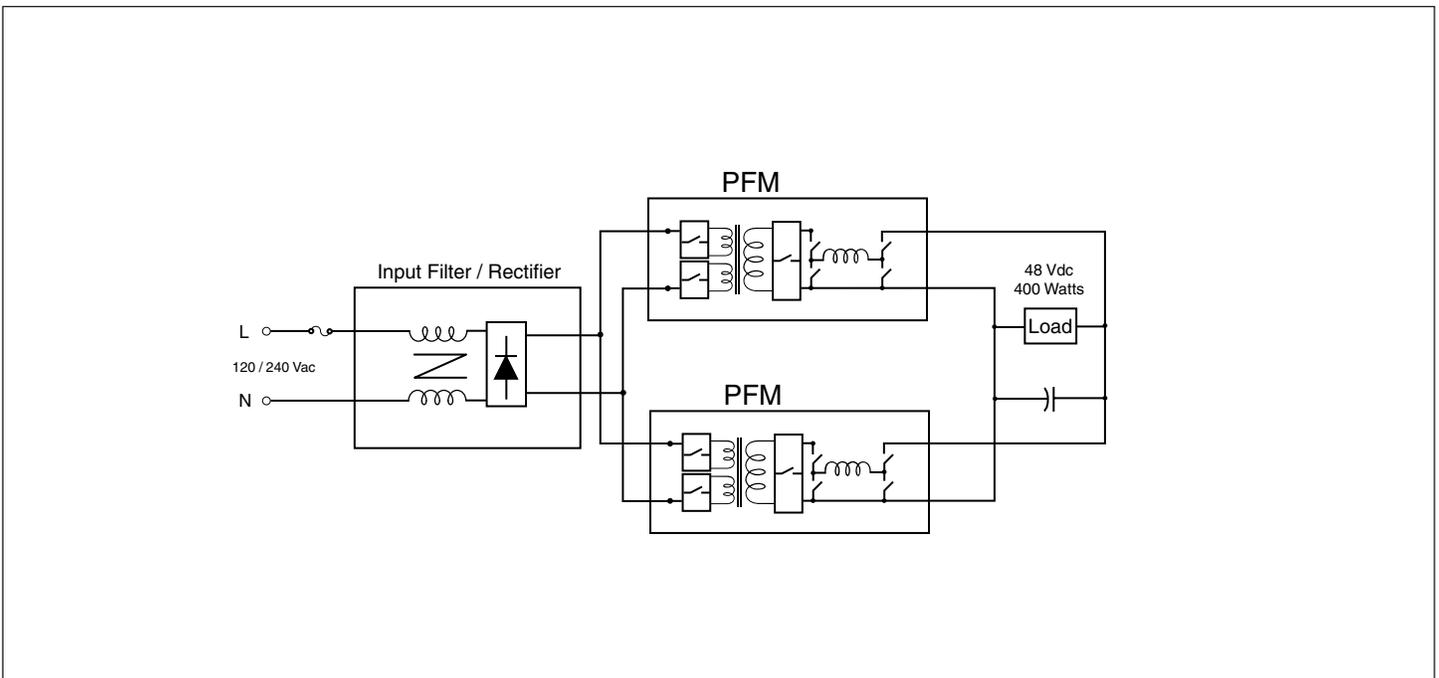


Figure 21 — Two PFMs operated in parallel for additional power.

Thermal Management

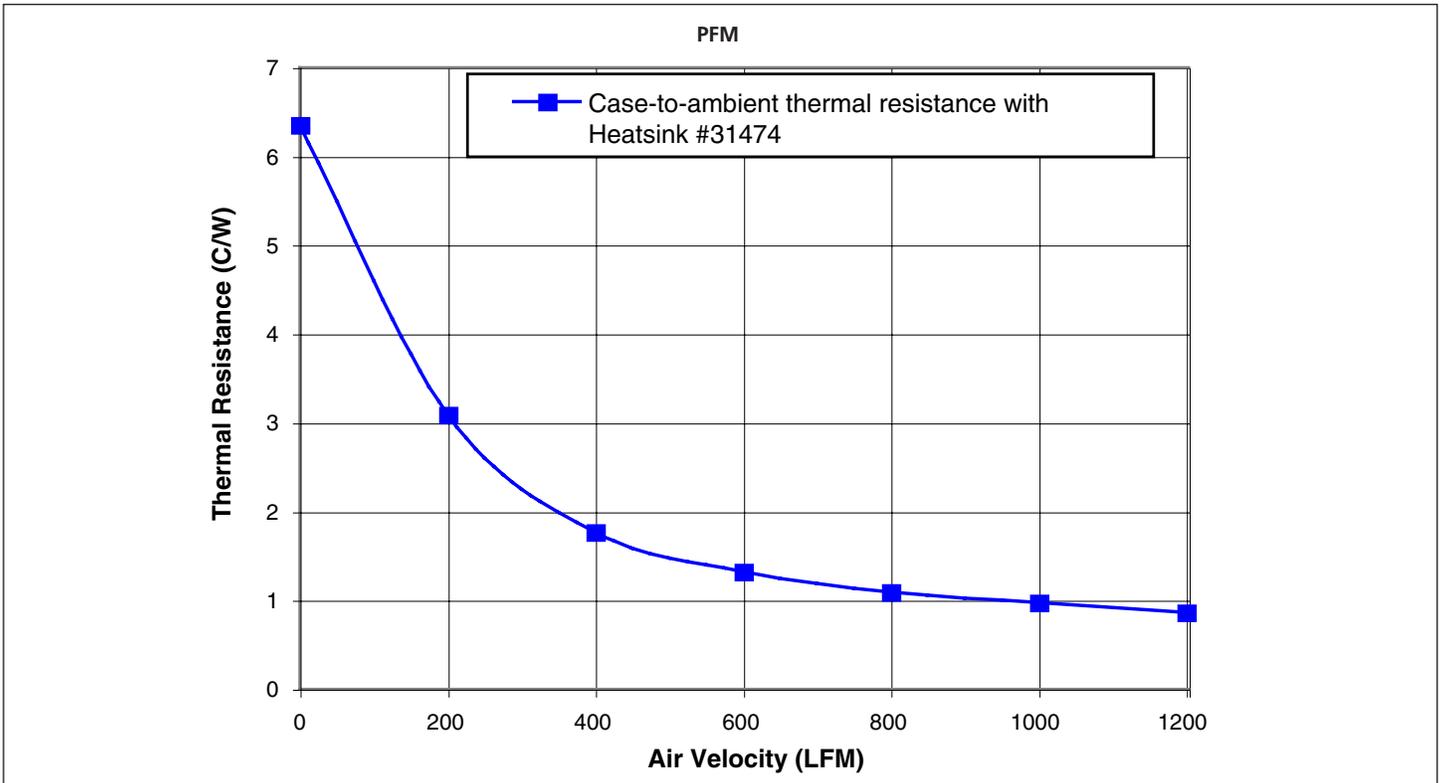


Figure 22 — Case to ambient thermal resistance vs. airflow using heatsink #31474 (46mm x 46mm x 11mm) with MCMStrate 2 mil interface

Mechanical Drawings

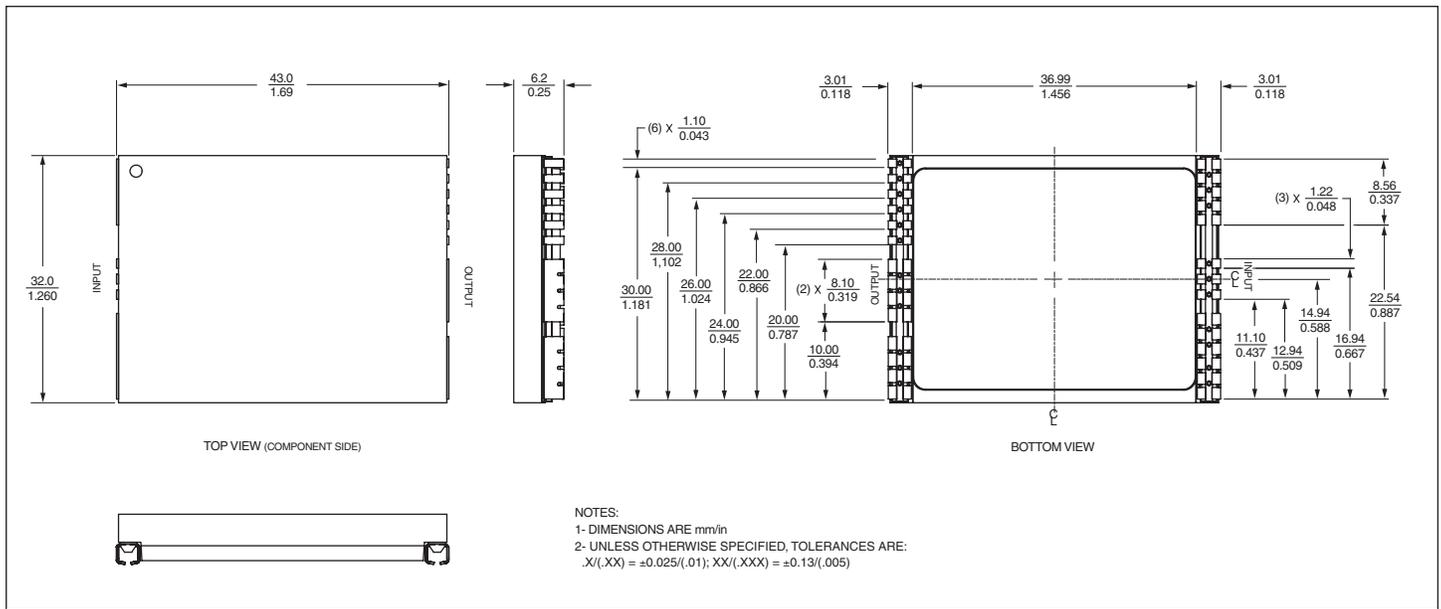


Figure 23 — PFM outline drawing

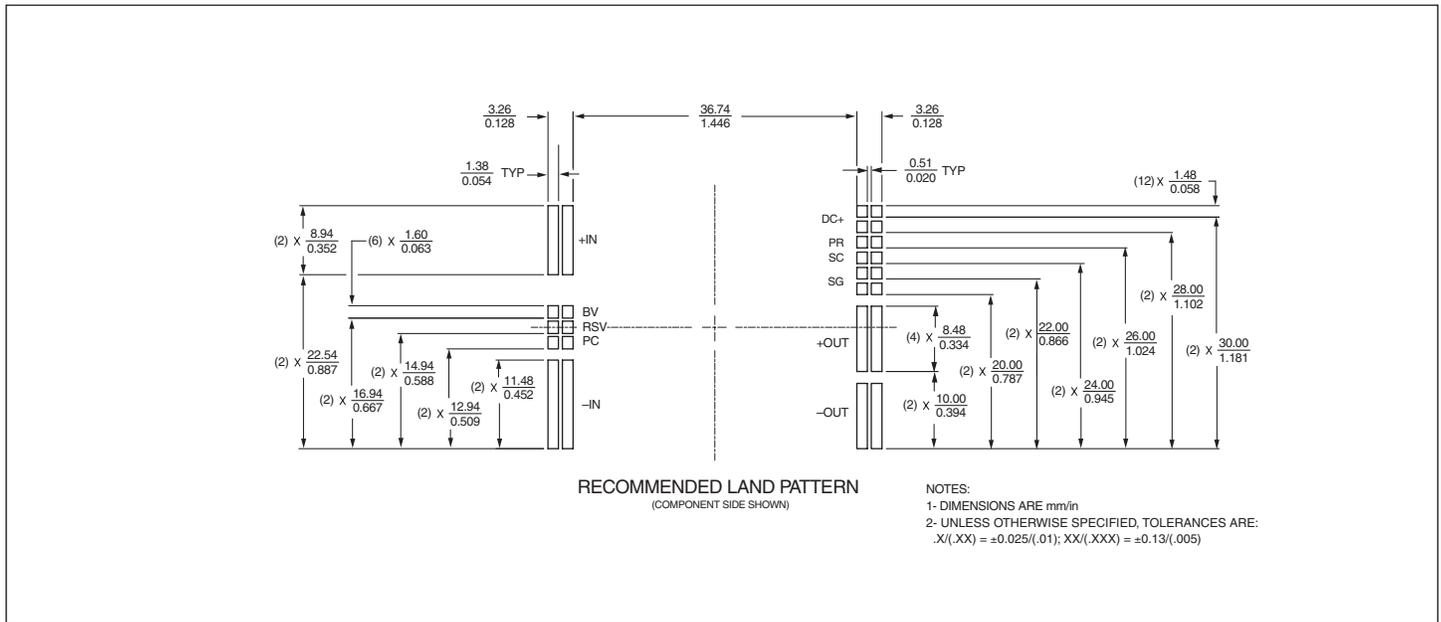


Figure 24 — PFM PCB land and layout information

PRELIMINARY

Warranty

Vicor products are guaranteed for two years from date of shipment against defects in material or workmanship when in normal use and service. This warranty does not extend to products subjected to misuse, accident, or improper application or maintenance. Vicor shall not be liable for collateral or consequential damage. This warranty is extended to the original purchaser only.

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Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

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