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# FIN3385 • FIN3383 • FIN3384 • FIN3386
## Low Voltage 28-Bit Flat Panel Display Link Serializers/Deserializers

## General Description

The FIN3385 and FIN3383 transform 28 bit wide parallel LVTTL (Low Voltage TTL) data into 4 serial LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data stream over a separate LVDS link. Every cycle of transmit clock 28 bits of input LVTTL data are sampled and transmitted.

The FIN3386 and FIN3384 receive and convert the 4/3 serial LVDS data streams back into 28/21 bits of LVTTL data. Refer to Table 1 for a matrix summary of the Serializers and Deserializers available. For the FIN3385, at a transmit clock frequency of 85MHz, 28 bits of LVTTL data are transmitted at a rate of 595Mbps per LVDS channel.

These chipsets are an ideal solution to solve EMI and cable size problems associated with wide and high-speed TTL interfaces.

## Features

- Low power consumption
- 20 MHz to 85 MHz shift clock support
- ±1V common-mode range around 1.2V
- Narrow bus reduces cable size and cost
- High throughput (up to 2.38 Gbps throughput)
- Internal PLL with no external component
- Compatible with TIA/EIA-644 specification
- Devices are offered 56-lead TSSOP packages

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| FIN3383MTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |
| FIN3384MTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |
| FIN3385MTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |
| FIN3386MTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

**TABLE 1. Display Panel Link Serializers/Deserializers Chip Matrix**

| Part | CLK Frequency | LVTTL IN | LVDS OUT | LVDS IN | LVTTL OUT | Package |
|---|---|---|---|---|---|---|
| FIN3385 | 85 | 28 | 4 | | | 56 TSSOP |
| FIN3383 | 66 | 28 | 4 | | | 56 TSSOP |
| FIN3386 | 85 | | | 4 | 28 | 56 TSSOP |
| FIN3384 | 66 | | | 4 | 28 | 56 TSSOP |

# Block Diagrams

### Functional Diagram for FIN3385 and FIN3383

LVTTL Inputs

LVDS Outputs

RED 8
GRN 8
BLU 8
Hsync
Vsync
Enable
Cntl
PwrDn

LVTTL Input Register

28

Parallel to Serial Converter

TxOut+
TxOut-
TxOut+
TxOut-
TxOut+
TxOut-
TxOut+
TxOut-

TxCLKIn

PLL

TxCLKOut+
TxCLKOut-
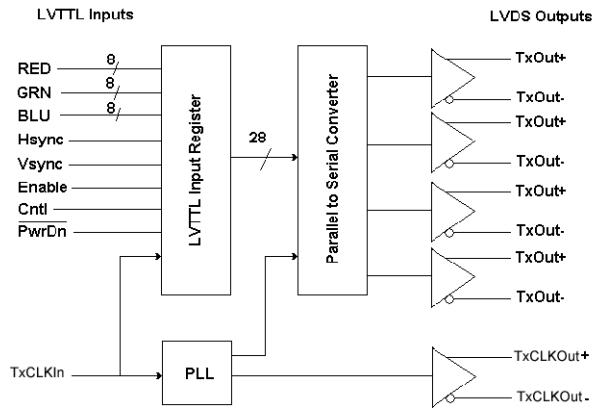
### Receiver Functional Diagram for FIN3386 and FIN3384

LVDS Inputs

LVTTL Outputs

Rxin+
Rxin-
Rxin+
Rxin-
Rxin+
Rxin-
Rxin+
Rxin-

Serial to Parallel Converter

28

LVTTL output Registers

RED 8
GRN 8
BLU 8
Hsync
Vsync
Enable
Cntl
PwrDn
(LVTTL Input)

RxCLKIn+
RxCLKIn-

PLL

RxCLKOut
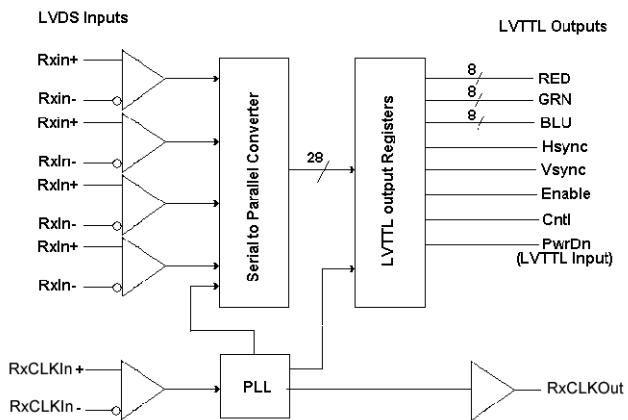
## TRANSMITTERS

## Pin Descriptions

| Pin Names | I/O Type | Number of Pins | Description of Signals |
|---|---|---|---|
| TxIn | I | 28/21 | LVTTL Level Input |
| TxCLKIn | I | 1 | LVTTL Level Clock Input<br>The rising edge is for data strobe. |
| TxOut+ | O | 4/3 | Positive LVDS Differential Data Output |
| TxOut− | O | 4/3 | Negative LVDS Differential Data Output |
| TxCLKOut+ | O | 1 | Positive LVDS Differential Clock Output |
| TxCLKOut− | O | 1 | Negative LVDS Differential Clock Output |
| R_FB | I | 1 | Rising Edge Clock (HIGH), Falling Edge Clock (LOW) |
| $\overline{\text{PwrDn}}$ | I | 1 | LVTTL Level Power-Down Input<br>Assertion (LOW) puts the outputs in High Impedance state. |
| PLL $V_{CC}$ | I | 1 | Power Supply Pin for PLL |
| PLL GND | I | 2 | Ground Pins for PLL |
| LVDS $V_{CC}$ | I | 1 | Power Supply Pin for LVDS Output |
| LVDS GND | I | 3 | Ground Pins for LVDS Output |
| $V_{CC}$ | I | 3 | Power Supply Pins for LVTTL Input |
| GND | I | 5 | Ground pins for LVTTL Input |
| NC | | | No Connect |

## Connection Diagram

**FIN3383 and FIN3385 (28:4 Transmitter)
Pin Assignment for TSSOP**

| | | | |
|---|---|---|---|
| $V_{CC}$ | 1 | 56 | TxIn4 |
| TxIn5 | 2 | 55 | TxIn3 |
| TxIn6 | 3 | 54 | TxIn2 |
| TxIn7 | 4 | 53 | GND |
| GND | 5 | 52 | TxIn1 |
| TxIn8 | 6 | 51 | TxIn0 |
| TxIn9 | 7 | 50 | TxIn27 |
| TxIn10 | 8 | 49 | LVDS GND |
| $V_{CC}$ | 9 | 48 | TxOut0- |
| TxIn11 | 10 | 47 | TxOut 0+ |
| TxIn12 | 11 | 46 | TxOut 1- |
| TxIn13 | 12 | 45 | TxOut1+ |
| GND | 13 | 44 | LVDS $V_{CC}$ |
| TxIn14 | 14 | 43 | LVDS GND |
| TxIn15 | 15 | 42 | TxOut2- |
| TxIn16 | 16 | 41 | TxOut2+ |
| R_FB | 17 | 40 | TxCLKOut- |
| TxIn17 | 18 | 39 | TxCLKOut+ |
| TxIn18 | 19 | 38 | TxOut3- |
| TxIn19 | 20 | 37 | TxOut 3+ |
| GND | 21 | 36 | LVDS GND |
| TxIn20 | 22 | 35 | PLL GND |
| TxIn21 | 23 | 34 | PLL $V_{CC}$ |
| TxIn22 | 24 | 33 | PLL GND |
| TxIn23 | 25 | 32 | $\overline{\text{PwrDn}}$ |
| $V_{CC}$ | 26 | 31 | TxCLKIn |
| TxIn24 | 27 | 30 | TxIn26 |
| TxIn25 | 28 | 29 | GND |

## Truth Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| TxIn | TxCLKIn | $\overline{\text{PwrDn}}$<br>(Note 1) | TxOut± | TxCLKOut± |
| Active | Active | H | L/H | L/H |
| Active | L/H/Z | H | L/H | X (Note 2) |
| F | Active | H | L | L/H |
| F | F | H | L | X (Note 2) |
| X | X | L | Z | Z |

H = HIGH Logic Level
L = LOW Logic Level
X = Don't Care
Z = High Impedance
F = Floating

**Note 1:** The outputs of the transmitter or receiver will remain in a High Impedance state until $V_{CC}$ reaches 2V.

**Note 2:** TxCLKOut± will settle at a free running frequency when the part is powered up, $\overline{\text{PwrDn}}$ is HIGH and the TxCLKIn is a steady logic level (L/H/Z).

## RECEIVERS

## Pin Descriptions

| Pin Names | I/O Type | Number of Pins | Description of Signals |
|---|---|---|---|
| RxIn– | I | 4/3 | Negative LVDS Differential Data Input |
| RxIn+ | I | 4/3 | Positive LVDS Differential Data Input |
| RxCLKIn– | I | 1 | Negative LVDS Differential Clock Input |
| RxCLKIn+ | I | 1 | Positive LVDS Differential Clock Input |
| RxOut | O | 28/21 | LVTTL Level Data Output<br>Goes HIGH for PwrDn LOW |
| RxCLKOut | O | 1 | LVTTL Clock Output |
| $\overline{\text{PwrDn}}$ | I | 1 | LVTTL Level Input<br>Refer to Transmitter and Receiver Power-Up and Power-Down Operation Truth Table |
| PLL $V_{CC}$ | I | 1 | Power Supply Pin for PLL |
| PLL GND | I | 2 | Ground Pins for PLL |
| LVDS $V_{CC}$ | I | 1 | Power Supply Pin for LVDS Input |
| LVDS GND | I | 3 | Ground Pins for LVDS Input |
| $V_{CC}$ | I | 4 | Power Supply for LVTTL Output |
| GND | I | 5 | Ground Pin for LVTTL Output |
| NC | | | No Connect |

## Connection Diagram

**FIN3386 and FIN3384 (4:28 Receiver)**
**Pin Assignment for TSSOP**

| Left | Pin | | Pin | Right |
|---|---|---|---|---|
| RxOut22 | 1 | | 56 | $V_{CC}$ |
| RxOut23 | 2 | | 55 | RxOut21 |
| RxOut24 | 3 | | 54 | RxOut20 |
| GND | 4 | | 53 | RxOut19 |
| RxOut25 | 5 | | 52 | GND |
| RxOut26 | 6 | | 51 | RxOut18 |
| RxOut27 | 7 | | 50 | RxOut17 |
| LVDS GND | 8 | | 49 | RxOut16 |
| RxIn0- | 9 | | 48 | $V_{CC}$ |
| RxIn 0+ | 10 | | 47 | RxOut15 |
| RxIn 1- | 11 | | 46 | RxOut14 |
| RxIn 1+ | 12 | | 45 | RxOut13 |
| LVDS $V_{CC}$ | 13 | | 44 | GND |
| LVDS GND | 14 | | 43 | RxOut12 |
| RxIn 2- | 15 | | 42 | RxOut11 |
| RxIn 2+ | 16 | | 41 | RxOut10 |
| RxCLK In - | 17 | | 40 | $V_{CC}$ |
| RxCLK In + | 18 | | 39 | RxOut9 |
| RxIn 3- | 19 | | 38 | RxOut8 |
| RxIn 3+ | 20 | | 37 | RxOut7 |
| LVDS GND | 21 | | 36 | GND |
| PLL GND | 22 | | 35 | RxOut 6 |
| PLL $V_{CC}$ | 23 | | 34 | RxOut 5 |
| PLL GND | 24 | | 33 | RxOut 4 |
| PwrDn | 25 | | 32 | RxOut 3 |
| RxCLK | 26 | | 31 | $V_{CC}$ |
| RxOut0 | 27 | | 30 | RxOut2 |
| GND | 28 | | 29 | RxOut 1 |

# Transmitter and Receiver Power-Up/Power-Down Operation Truth Table

The outputs of the transmitter remain in the High-Impedance state until the power supply reaches 2V. The following table shows the operation of the transmitter during power-up and power-down and operation of the PwrDn pin.

| Transmitter | | | PwrDn | Normal | | | |
|---|---|---|---|---|---|---|---|
| | $V_{CC}$ | <2V | >2V | >2V | >2V | >2V | >2V |
| | TxIn | X | X | Active | Active | | |
| | TxOut | Z | Z | Active | X | | |
| | TxCLKIn | X | X | Active | H/L/Z | | |
| | TxCLKOut± | Z | Z | Active | (Note 3) | | |
| | PwrDn | L | L | H | H | H | H |
| Receiver | | | PwrDn | | | | |
| | RxIn± | X | X | Active | Active | (Note 4) | (Note 4) |
| | RxOut | Z | L | L/H | P | H | P |
| | RxCLKIn± | X | X | Active | (Note 4) | Active | (Note 4) |
| | RxCLKOut | Z | (Note 5) | Active | (Note 5) | (Note 5) | (Note 5) |
| | PwrDn | L | L | H | H | H | H |
| | $V_{CC}$ | <2V | <2V | <2V | <2V | <2V | <2V |

H = HIGH Logic Level
L = LOW Logic Level
P = Last Valid State
X = Don't Care
Z = High-Impedance

**Note 3:** If the transmitter is powered up and PwrDn is inactive HIGH and the clock input goes to any state LOW, HIGH, or Z then the internal PLL will go to a known low frequency and stay until the clock starts normal operation again.

**Note 4:** If the input is terminated and un-driven (Z) or shorted or open. (fail safe condition)

**Note 5:** For PwrDn or fail safe condition the RxCLKOut pin will go LOW for Panel Link devices and HIGH for Channel Link devices.

**Note 6:** Shorted here means (± inputs are shorted to each other, or ± inputs are shorted to each other and Ground or $V_{CC}$, or either ± inputs are shorted to Ground or $V_{CC}$) with no other Current/Voltage sources (noise) applied. If the $V_{ID}$ is still in the valid range (greater than 100mV) and VCM is in the valid range (0V to 2.4V) then the input signal is still recognized and the part will respond normally.

## Absolute Maximum Ratings(Note 7)

| | |
|---|---|
| Power Supply Voltage ($V_{CC}$) | -0.3V to +4.6V |
| TTL/CMOS Input/Output Voltage | −0.5V to +4.6V |
| LVDS Input/Output Voltage | -0.3V to +4.6V |
| LVDS Output Short Circuit Current ($I_{OSD}$) | Continuous |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Maximum Junction Temperature ($T_J$) | 150°C |
| Lead Temperature ($T_L$) | |
| (Soldering, 4 seconds) | 260°C |
| ESD Rating (HBM, 1.5 kΩ, 100 pF) | |
| I/O to GND | >10.0 kV |
| All Pins | >6.5 kV |
| ESD Rating (MM, 0Ω, 200 pF) | >400V |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 3.0V to 3.6V |
| Operating Temperature ($T_A$)(Note 7) | −10°C to +70°C |
| Maximum Supply Noise Voltage | |
| ($V_{CCNPP}$) | 100 m$V_{P-P}$ (Note 8) |

**Note 7:** Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

**Note 8:** 100mV $V_{CC}$ noise should be tested for frequency at least up to 2 MHz. All the specification below should be met under such a noise.

## Transmitter DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Note 9)

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Transmitter LVTTL Input Characteristics** | | | | | | | |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage | | | GND | | 0.8 | V |
| $V_{IK}$ | Input Clamp Voltage | $I_{IK} = −18$ mA | | | −0.79 | −1.5 | V |
| $I_{IN}$ | Input Current | $V_{IN} = 0.4V$ to 4.6V | | | 1.8 | 10.0 | μA |
| | | $V_{IN} = $ GND | | −10.0 | 0 | | |
| **Transmitter LVDS Output Characteristics (Note 10)** | | | | | | | |
| $V_{OD}$ | Output Differential Voltage | $R_L = 100$ Ω, See Figure 1 | | 250 | TBD | 450 | mV |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change from Differential LOW-to-HIGH | | | | | 35.0 | mV |
| $V_{OS}$ | Offset Voltage | | | 1.125 | 1.25 | 1.375 | V |
| $\Delta V_{OS}$ | Offset Magnitude Change from Differential LOW-to-HIGH | | | | | | mV |
| $I_{OS}$ | Short Circuit Output Current | $V_{OUT} = 0V$ | | | −3.5 | −5.0 | mA |
| $I_{OZ}$ | Disabled Output Leakage Current | DO = 0V to 4.6V, $\overline{PwrDn} = 0V$ | | | ±1.0 | ±10.0 | μA |
| **Transmitter Supply Current** | | | | | | | |
| $I_{CCWT}$ | 28:4 Transmitter Power Supply Current for Worst Case Pattern (With Load) (Note 11) | $R_L = 100$ Ω, See Figure 3 | 32.5 MHz | | 31.0 | 49.5 | mA |
| | | | 40.0 MHz | | 32.0 | 55.0 | |
| | | | 66.0 MHz | | 37.0 | 60.5 | |
| | | | 85.0 MHz | | 42.0 | 66.0 | |
| $I_{CCPDT}$ | Powered Down Supply Current | $\overline{PwrDn} = 0.8V$ | | | 10.0 | 55.0 | μA |
| $I_{CCGT}$ | 28:4 Transmitter Supply Current for 16 Grayscale (Note 11) | See Figure 21 (Note 12) | 32.5 MHz | | 29.0 | 41.8 | mA |
| | | | 40.0 MHz | | 30.0 | 44.0 | |
| | | | 65.0 MHz | | 35.0 | 49.5 | |
| | | | 85.0 MHz | | 39.0 | 55.0 | |

**Note 9:** All Typical values are at $T_A = 25$°C and with $V_{CC} = 3.3V$.

**Note 10:** Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltage are referenced to ground unless otherwise specified (except $\Delta V_{OD}$ and $V_{OD}$).

**Note 11:** The power supply current for both transmitter and receiver can be different with the number of active I/O channels.

**Note 12:** The 16-grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

## Transmitter AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
| $t_{TCP}$ | Transmit Clock Period | | 11.76 | T | 50.0 | ns |
| $t_{TCH}$ | Transmit Clock (TxCLKIn) HIGH Time | See Figure 5 | 0.35 | 0.5 | 0.65 | T |
| $t_{TCL}$ | Transmit Clock Low Time | | 0.35 | 0.5 | 0.65 | T |
| $t_{CLKT}$ | TxCLKIn Transition Time (Rising and Failing) | (10% to 90%) See Figure 6 | 1.0 | | 6.0 | ns |
| $t_{JIT}$ | TxCLKIn Cycle-to-Cycle Jitter | | | | 3.0 | ns |
| $t_{XIT}$ | TxIn Transition Time | | 1.5 | | 6.0 | ns |
| **LVDS Transmitter Timing Characteristics** | | | | | | |
| $t_{TLH}$ | Differential Output Rise Time (20% to 80%) | See Figure 4 | | 0.75 | 1.5 | ns |
| $t_{THL}$ | Differential Output Fall Time (80% to 20%) | | | 0.75 | 1.5 | ns |
| $t_{STC}$ | TxIn Setup to TxCLNIn | See Figure 5 (f = 85 MHz) | 2.5 | | | ns |
| $t_{HTC}$ | TxIn Holds to TCLKIn | | 0 | | | ns |
| $t_{TPDD}$ | Transmitter Power-Down Delay | See Figure 12, (Note 13) | | | 100 | ns |
| $t_{TCCD}$ | Transmitter Clock Input to Clock Output Delay | ($T_A$ = 25°C and with $V_{CC}$ = 3.3V) | | | 5.5 | ns |
| | Transmitter Clock Input to Clock Output Delay | See Figure 9 | 2.8 | | 6.8 | |
| **Transmitter Output Data Jitter (f = 40 MHz) (Note 14)** | | | | | | |
| $t_{TPPB0}$ | Transmitter Output Pulse Position of Bit 0 | | −0.25 | 0 | 0.25 | ns |
| $t_{TPPB1}$ | Transmitter Output Pulse Position of Bit 1 | See Figure 16 | a−0.25 | a | a+0.25 | ns |
| $t_{TPPB2}$ | Transmitter Output Pulse Position of Bit 2 | $a = \dfrac{1}{f \times 7}$ | 2a−0.25 | 2a | 2a+0.25 | ns |
| $t_{TPPB3}$ | Transmitter Output Pulse Position of Bit 3 | | 3a−0.25 | 3a | 3a+0.25 | ns |
| $t_{TPPB4}$ | Transmitter Output Pulse Position of Bit 4 | | 4a−0.25 | 4a | 4a+0.25 | ns |
| $t_{TPPB5}$ | Transmitter Output Pulse Position of Bit 5 | | 5a−0.25 | 5a | 5a+0.25 | ns |
| $t_{TPPB6}$ | Transmitter Output Pulse Position of Bit 6 | | 6a−0.25 | 6a | 6a+0.25 | ns |
| **Transmitter Output Data Jitter (f = 65 MHz) (Note 14)** | | | | | | |
| $t_{TPPB0}$ | Transmitter Output Pulse Position of Bit 0 | | −0.2 | 0 | 0.2 | ns |
| $t_{TPPB1}$ | Transmitter Output Pulse Position of Bit 1 | See Figure 16 | a−0.2 | a | a+0.2 | ns |
| $t_{TPPB2}$ | Transmitter Output Pulse Position of Bit 2 | $a = \dfrac{1}{f \times 7}$ | 2a−0.2 | 2a | 2a+0.2 | ns |
| $t_{TPPB3}$ | Transmitter Output Pulse Position of Bit 3 | | 3a−0.2 | 3a | 3a+0.2 | ns |
| $t_{TPPB4}$ | Transmitter Output Pulse Position of Bit 4 | | 4a−0.2 | 4a | 4a+0.2 | ns |
| $t_{TPPB5}$ | Transmitter Output Pulse Position of Bit 5 | | 5a−0.2 | 5a | 5a+0.2 | ns |
| $t_{TPPB6}$ | Transmitter Output Pulse Position of Bit 6 | | 6a−0.2 | 6a | 6a+0.2 | ns |
| **Transmitter Output Data Jitter (f = 85 MHz) (Note 14)** | | | | | | |
| $t_{TPPB0}$ | Transmitter Output Pulse Position of Bit 0 | | −0.2 | 0 | 0.2 | ns |
| $t_{TPPB1}$ | Transmitter Output Pulse Position of Bit 1 | See Figure 16 | a−0.2 | a | a+0.2 | ns |
| $t_{TPPB2}$ | Transmitter Output Pulse Position of Bit 2 | $a = \dfrac{1}{f \times 7}$ | 2a−0.2 | 2a | 2a+0.2 | ns |
| $t_{TPPB3}$ | Transmitter Output Pulse Position of Bit 3 | | 3a−0.2 | 3a | 3a+0.2 | ns |
| $t_{TPPB4}$ | Transmitter Output Pulse Position of Bit 4 | | 4a−0.2 | 4a | 4a+0.2 | ns |
| $t_{TPPB5}$ | Transmitter Output Pulse Position of Bit 5 | | 5a−0.2 | 5a | 5a+0.2 | ns |
| $t_{TPPB6}$ | Transmitter Output Pulse Position of Bit 6 | | 6a−0.2 | 6a | 6a+0.2 | ns |
| $t_{JCC}$ | FIN3385 Transmitter Clock Out Jitter | f = 40 MHz | | 350 | 370 | |
| | (Cycle-to-Cycle) | f = 65 MHz | | 210 | 230 | ps |
| | See Figure 20 | f = 85 MHz | | 110 | 150 | |
| $t_{TPLLS}$ | Transmitter Phase Lock Loop Set Time (Note 15) | See Figure 22, (Note 14) | | | 10.0 | ms |

**Note 13:** Outputs of all transmitters stay in 3-STATE until power reaches 2V. Both clock and data output begins to toggle 10ms after $V_{CC}$ reaches 3V and Power-Down pin is above 1.5V.

**Note 14:** This output data pulse position works for TTL inputs except the LVDS output bit mapping difference (see Figure 14). Figure 16 shows the skew between the first data bit and clock output. Also 2-bit cycle delay is guaranteed when the MSB is output from transmitter.

**Note 15:** This jitter specification is based on the assumption that PLL has a ref clock with cycle-to-cycle input jitter less than 2ns.

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## Receiver DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Note 16)

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **LVTTL/CMOS DC Characteristics** | | | | | | | |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input Low Voltage | | | GND | | 0.8 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH} = -0.4$ mA | | 2.7 | 3.3 | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 2$mA | | | 0.06 | 0.3 | V |
| $V_{IK}$ | Input Clamp Voltage | $I_{IK} = -18$ mA | | | −0.79 | −1.5 | V |
| $I_{IN}$ | Input Current | $V_{IN} = 0$V to 4.6V | | −10.0 | | 10.0 | μA |
| $I_{OFF}$ | Input/Output Power Off Leakage Current | $V_{CC} = 0$V, All LVTTL Inputs/Outputs 0V to 4.6V | | | | ±10.0 | μA |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT} = 0$V | | | −60.0 | −120 | mA |
| **Receiver LVDS Input Characteristics** | | | | | | | |
| $V_{TH}$ | Differential Input Threshold HIGH | Figure 2, Table 2 | | | | 100 | mV |
| $V_{TL}$ | Differential Input Threshold LOW | Figure 2, Table 2 | | −100 | | | mV |
| $V_{ICM}$ | Input Common Mode Range | Figure 2, Table 2 | | 0.05 | | 2.35 | V |
| $I_{IN}$ | Input Current | $V_{IN} = 2.4$V, $V_{CC} = 3.6$V or 0V | | | | ±10.0 | μA |
| | | $V_{IN} = 0$V, $V_{CC} = 3.6$V or 0V | | | | ±10.0 | μA |
| **Receiver Supply Current** | | | | | | | |
| $I_{CCWR}$ | 4:28 Receiver Power Supply Current for Worst Case Pattern (With Load) (Note 17) | $C_L = 8$ pF, See Figure 3 | 32.5 MHz | | | 70.0 | mA |
| | | | 40.0 MHz | | | 75.0 | |
| | | | 66.0 MHz | | | 114 | |
| | | | 85.0 MHz | | | 135 | |
| $I_{CCWR}$ | 3:21 Receiver Power Supply Current for Worst Case Pattern (With Load) (Note 17) | $C_L = 8$ pF, See Figure 3 | 32.5 MHz | | 49.0 | 60.0 | mA |
| | | | 40.0 MHz | | 53.0 | 65.0 | |
| | | | 66.0 MHz | | 78.0 | 100 | |
| | | | 85.0 MHz | | 90.0 | 115 | |
| $I_{CCPDT}$ | Powered Down Supply Current | $\overline{PwrDn} = 0.8$V (RxOut stays LOW) | | | NA | 55.0 | μA |
| $t_{RCOP}$ | Receiver Clock Output (RxCLKOut) Period | | | 11.76 | T | 50.0 | |
| $t_{RCOL}$ | RxCLKOut LOW Time | See Figure 8 | | 4.0 | 5.0 | 6.0 | ns |
| $t_{RCOH}$ | RxCLKOut HIGH Time | (f = 85MHz) | | 4.5 | 5.0 | 6.5 | ns |
| $t_{RSRC}$ | RxOut Valid Prior to RxCLKOut | (Rising Edge Strobe) | | 3.5 | | | ns |
| $t_{RHRC}$ | RxOut Valid After RxCLKOut | | | 3.5 | | | ns |
| $t_{ROLH}$ | Output Rise Time (20% to 80%) | $C_L = 8$ pF, See Figure 4 | | | 2.0 | 3.5 | ns |
| $t_{ROHL}$ | Output Fall Time (80% to 20%) | | | | 1.8 | 3.5 | ns |
| $t_{RCCD}$ | Receiver Clock Input to Clock Output Delay | See Figure 20, (Note 18) $T_A = 25°C$ and $V_{CC} = 3.3$V | | 3.5 | 5.0 | 7.5 | ns |
| $t_{RPDD}$ | Receiver Power-Down Delay | See Figure 13 | | | | 1.0 | μs |
| $t_{RSPB0}$ | Receiver Input Strobe Position of Bit 0 | | | 0.49 | 0.84 | 1.19 | ns |
| $t_{RSPB1}$ | Receiver Input Strobe Position of Bit 1 | | | 2.17 | 2.52 | 2.87 | ns |
| $t_{RSPB2}$ | Receiver Input Strobe Position of Bit 2 | | | 3.85 | 4.20 | 4.55 | ns |
| $t_{RSPB3}$ | Receiver Input Strobe Position of Bit 3 | See Figure 17 (f = 85MHz) | | 5.53 | 5.88 | 6.23 | ns |
| $t_{RSPB4}$ | Receiver Input Strobe Position of Bit 4 | | | 7.21 | 7.56 | 7.91 | ns |
| $t_{RSPB5}$ | Receiver Input Strobe Position of Bit 5 | | | 8.89 | 9.24 | 9.59 | ns |
| $t_{RSPB6}$ | Receiver Input Strobe Position of Bit 6 | | | 10.57 | 10.92 | 11.27 | ns |
| $t_{RSKM}$ | RxIN Skew Margin | See Figure 17, (Note 19) | | 290 | | | ps |
| $t_{RPLLS}$ | Receiver Phase Lock Loop Set Time | See Figure 11 | | | | 10.0 | ms |

**Note 16:** All Typical values are at $T_A = 25°C$ and with $V_{CC} = 3.3$V. Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltage are referenced to ground unless otherwise specified (except $\Delta V_{OD}$ and $V_{OD}$).

**Note 17:** The power supply current for the receiver can be different with the number of active I/O channels.

**Note 18:** Total channel latency from Sewrializer to deserializer is (T + $t_{TCCD}$). There is the clock period.

**Note 19:** Receiver skew margin is defined as the valid sampling window after considering potential setup/hold time and minimum/maximum bit position.

## Receiver AC Electrical Characteristics (66MHz)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{RCOP}$ | Receiver Clock Output (RxCLKOut) Period | See Figure 8 | 15.0 | T | 50.0 | ns |
| $t_{RCOL}$ | RxCLKOut LOW Time | | 10.0 | 11.0 | | ns |
| $t_{RCOH}$ | RxCLKOut HIGH Time | See Figure 8 | 10.0 | 12.2 | | ns |
| $t_{RSRC}$ | RxOut Valid Prior to RxCLKOut | (Rising Edge Strobe) | 6.5 | 11.6 | | ns |
| $t_{RHRC}$ | RxOut Valid After RxCLKOut | (f = 40 MHz) | 6.0 | 11.6 | | ns |
| $t_{RCOL}$ | RxCLKOut LOW Time | | 5.0 | 6.3 | 9.0 | ns |
| $t_{RCOH}$ | RxCLKOut HIGH Time | See Figure 8, (Note 20) | 5.0 | 7.6 | 9.0 | ns |
| $t_{RSRC}$ | RxOut Valid Prior to RxCLKOut | (Rising Edge Strobe) | 4.5 | 7.3 | | ns |
| $t_{RHRC}$ | RxOut Valid After RxCLKOut | (f = 66 MHz) | 4.0 | 6.3 | | ns |
| $t_{ROLH}$ | Output Rise Time (20% to 80%) | $C_L$ = 8 pF, (Note 20) | | 2.0 | 5.0 | ns |
| $t_{ROHL}$ | Output Fall Time (80% to 20%) | See Figure 8 | | 1.8 | 5.0 | ns |
| $t_{RCCD}$ | Receiver Clock Input to Clock Output Delay | See Figure 10, (Note 21) $T_A$ = 25°C and $V_{CC}$ = 3.3V | 3.5 | 5.0 | 7.5 | ns |
| $t_{RPDD}$ | Receiver Power-Down Delay | See Figure 13 | | | 1.0 | μs |
| $t_{RSPB0}$ | Receiver Input Strobe Position of Bit 0 | | 1.0 | 1.4 | 2.15 | ns |
| $t_{RSPB1}$ | Receiver Input Strobe Position of Bit 1 | | 4.5 | 5.0 | 5.8 | ns |
| $t_{RSPB2}$ | Receiver Input Strobe Position of Bit 2 | See Figure 17 | 8.1 | 8.5 | 9.15 | ns |
| $t_{RSPB3}$ | Receiver Input Strobe Position of Bit 3 | (f = 40 MHz) | 11.6 | 11.9 | 12.6 | ns |
| $t_{RSPB4}$ | Receiver Input Strobe Position of Bit 4 | | 15.1 | 15.6 | 16.3 | ns |
| $t_{RSPB5}$ | Receiver Input Strobe Position of Bit 5 | | 18.8 | 19.2 | 19.9 | ns |
| $t_{RSPB6}$ | Receiver Input Strobe Position of Bit 6 | | 22.5 | 22.9 | 23.6 | ns |
| $t_{RSPB0}$ | Receiver Input Strobe Position of Bit 0 | | 0.7 | 1.1 | 1.4 | ns |
| $t_{RSPB1}$ | Receiver Input Strobe Position of Bit 1 | | 2.9 | 3.3 | 3.6 | ns |
| $t_{RSPB2}$ | Receiver Input Strobe Position of Bit2 | See Figure 17 | 5.1 | 5.5 | 5.8 | ns |
| $t_{RSPB3}$ | Receiver Input Strobe Position of Bit 3 | (f = 65 MHz) | 7.3 | 7.7 | 8.0 | ns |
| $t_{RSPB4}$ | Receiver Input Strobe Position of Bit 4 | | 9.5 | 9.9 | 10.2 | ns |
| $t_{RSPB5}$ | Receiver Input Strobe Position of Bit 5 | | 11.7 | 12.1 | 12.4 | ns |
| $t_{RSPB6}$ | Receiver Input Strobe Position of Bit 6 | | 13.9 | 14.3 | 14.6 | ns |
| $t_{RSKM}$ | RxIn Skew Margin | f = 40 MHz | 490 | | | ps |
| | See Figure 17, (Note 22) | f = 66 MHz | 400 | | | |
| $t_{RPLLS}$ | Receiver Phase Lock Loop Set Time | See Figure 11 | | | 10.0 | ms |

**Note 20:** For the receiver with falling-edge strobe, the definition of setup/hold time will be slightly different from the one with rising-edge strobe. The clock reference point is the time when the clock falling edge passes through 2V. For hold time $t_{RHRC}$, the clock reference point is the time when falling edge passes through +0.8V.

**Note 21:** Total channel latency from Sewrializer to deserializer is (T + $t_{TCCD}$) + (2*T + $t_{RCCD}$). There is the clock period.

**Note 22:** Receiver skew margin is defined as the valid sampling window after considering potential setup/hold time and minimum/maximum bit position.

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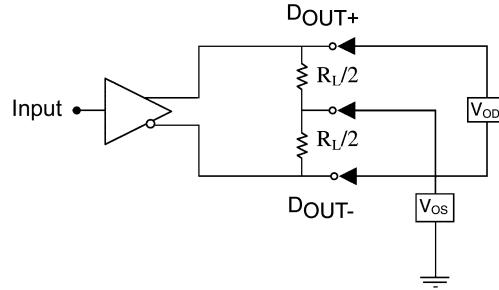
**FIGURE 1. Differential LVDS Output DC Test Circuit**
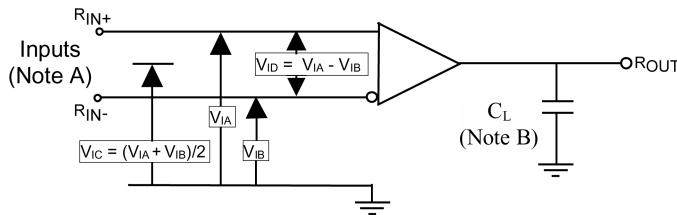


**Note A:** For all input pulses, $t_R$ or $t_F <= 1$ ns.
**Note B:** $C_L$ includes all probe and jig capacitance.

**FIGURE 2. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit**

**TABLE 2. Receiver Minimum and Maximum Input Threshold Test Voltages**

| Applied Voltages (V) | | Resulting Differential Input Voltage (mV) | Resulting Common Mode Input Voltage (V) |
|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ |
| 1.25 | 1.15 | 100 | 1.2 |
| 1.15 | 1.25 | −100 | 1.2 |
| 2.4 | 2.3 | 100 | 2.35 |
| 2.3 | 2.4 | −100 | 2.35 |
| 0.1 | 0 | 100 | 0.05 |
| 0 | 0.1 | −100 | 0.05 |
| 1.5 | 0.9 | 600 | 1.2 |
| 0.9 | 1.5 | −600 | 1.2 |
| 2.4 | 1.8 | 600 | 2.1 |
| 1.8 | 2.4 | −600 | 2.1 |
| 0.6 | 0 | 600 | 0.3 |
| 0 | 0.6 | −600 | 0.3 |

# AC Loading and Waveforms
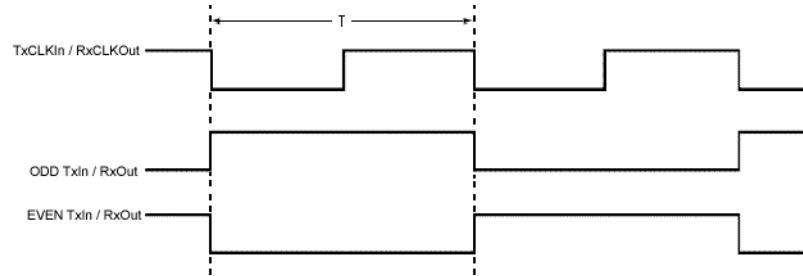
**Note:** The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and LVTTL/CMOS I/O. Depending on the valid strobe edge of transmitter, the TxCLKIn can be either rising or falling edge data strobe.

**FIGURE 3. "Worst Case" Test Pattern**

$V_{DIFF} = (TxOut+) - (TxOut-)$
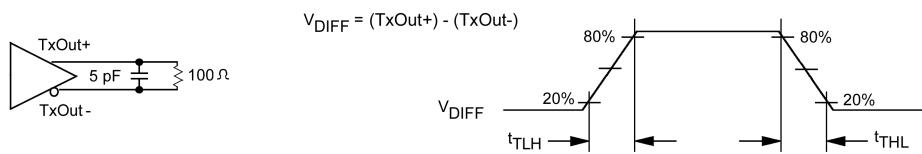


**FIGURE 4. Transmitter LVDS Output Load and Transition Times**
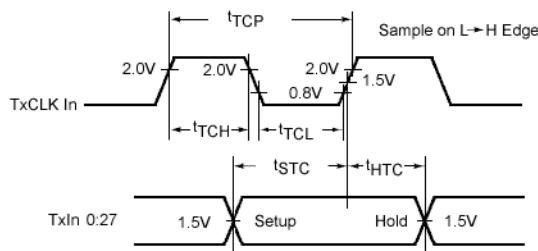


**FIGURE 5. Transmitter Setup/Hold and HIGH/LOW Times (Rising Edge Strobe)**
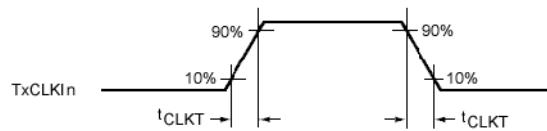


**FIGURE 6. Transmitter Input Clock Transition Time**

# AC Loading and Waveforms (Continued)
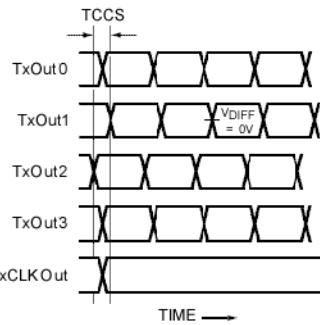


**FIGURE 7. Transmitter Outputs Channel-to-Channel Skew**
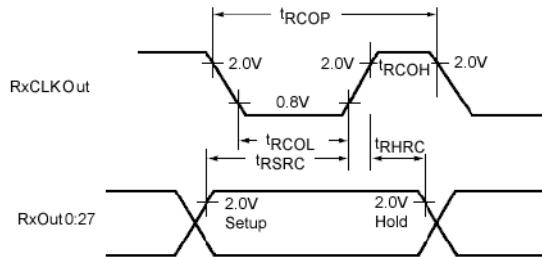


Note: For the receiver with falling-edge strobe, the definition of setup/hold time will be slightly different from the one with rising-edge strobe. The clock reference point is the time when the clock falling edge passes through 2V. For hold time $t_{RHRC}$, the clock reference point is the time when falling edge passes through +0.8V.

**FIGURE 8. (Receiver) Setup/Hold and HIGH/LOW Times**
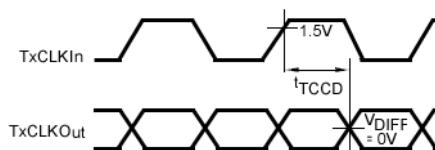


**FIGURE 9. Transmitter Clock In to Clock Out Delay (Rising Edge Strobe)**
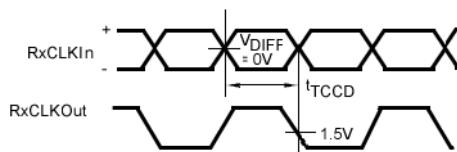


**FIGURE 10. Receiver Clock In to Clock Out Delay (Falling Edge Strobe)**

## AC Loading and Waveforms (Continued)
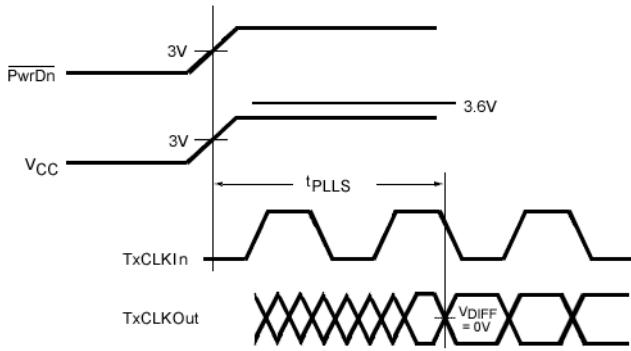
**FIGURE 11. Receiver Phase Lock Loop Set Time**
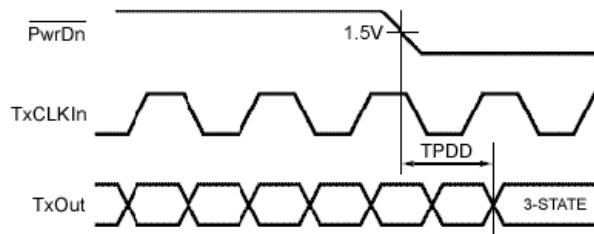


**FIGURE 12. Transmitter Power-Down Delay**
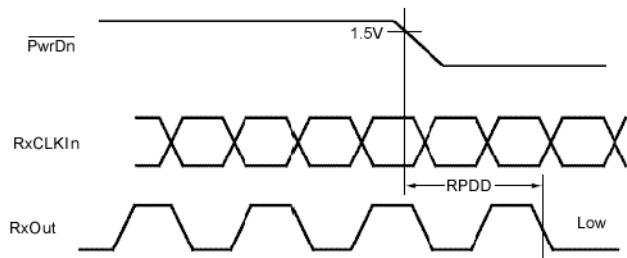


**FIGURE 13. Receiver Power-Down Delay**

## AC Loading and Waveforms (Continued)
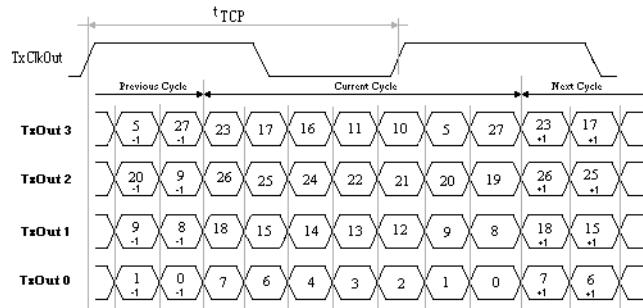


**Note:** The information in this diagram shows the relationship between clock out and the first data bit. A 2-bit cycle delay is guaranteed when the MSB is output from the transmitter.

**FIGURE 14. 28 Parallel LVTTL Inputs Mapped to 4 Serial LVDS Outputs**
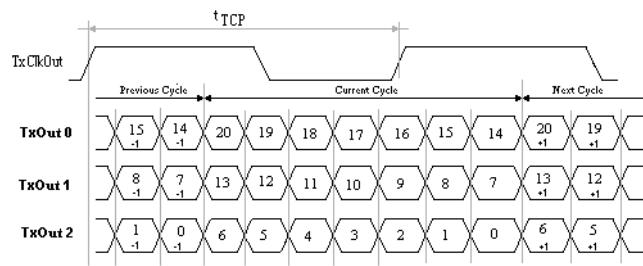


**Note:** This output data pulse position works for both transmitter with 28 or 21 TTL inputs except the LVDS output bit mapping difference. All the information in this diagram tells that the skew between the first data bit and clock output. Also 2-bit cycle delay is guaranteed when the MSB is output from transmitter.

**FIGURE 15. 21 Parallel LVTTL Inputs Mapped to 3 Serial LVDS Outputs**

## AC Loading and Waveforms (Continued)
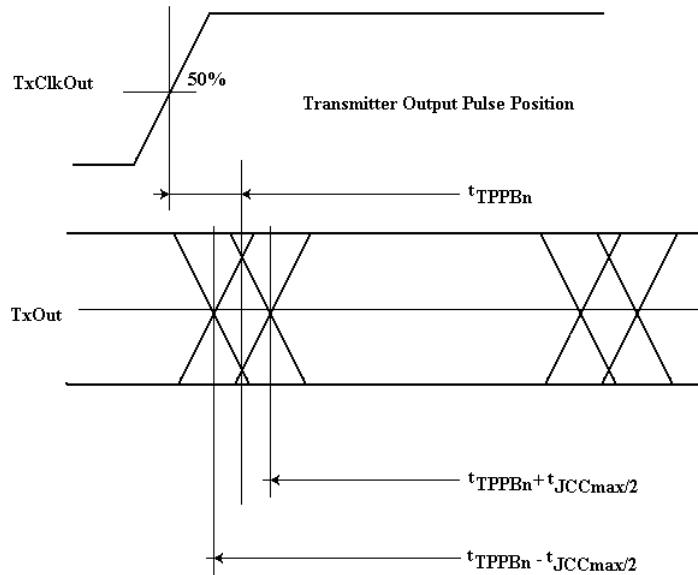
**FIGURE 16. Transmitter Output Pulse Bit Position**
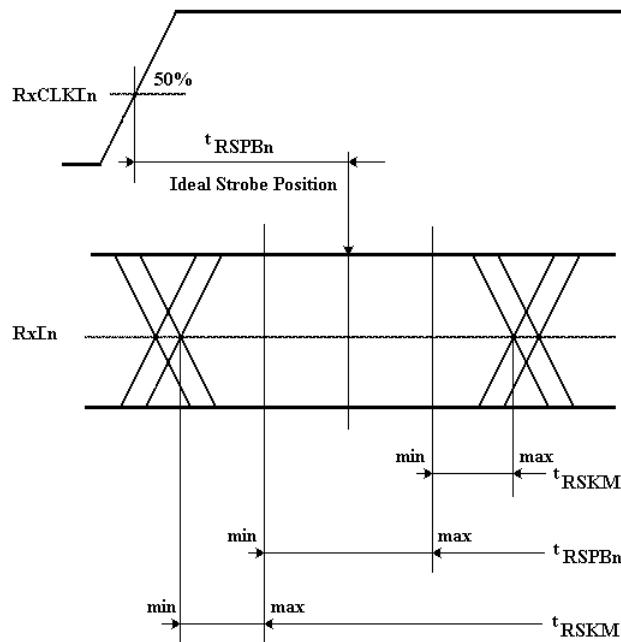


**FIGURE 17. Receiver Input Bit Position**

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# AC Loading and Waveforms (Continued)
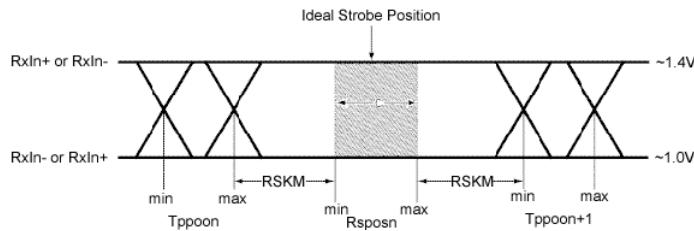


**Note:** $t_{RSKM}$ is the budget for the cable skew and source clock skew plus ISI (Inter-Symbol Interference).

**Note:** The minimum and maximum pulse position values are based on the bit position of each of the 7 bits within the LVDS data stream across PVT (Process, Voltage Supply, and Temperature).

**FIGURE 18. Receiver LVDS Input Skew Margin**
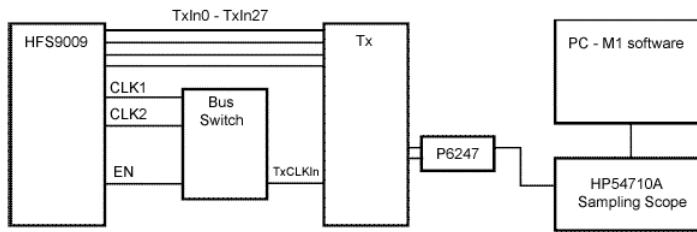


**Note:** Test setup used considers no requirement for separation of RMS and deterministic jitter. Other hardware setup such as Wavecrest boxes can be used if no M1 software is available, but the test methodology in Figure 20 should be followed.

**FIGURE 19. Transmitter Clock Out Jitter Measurement Setup**



32.5 MHz - N Cycle =  66
40   MHz - N Cycle =  80
65   MHz - N Cycle = 132
85   MHz - N Cycle = 170
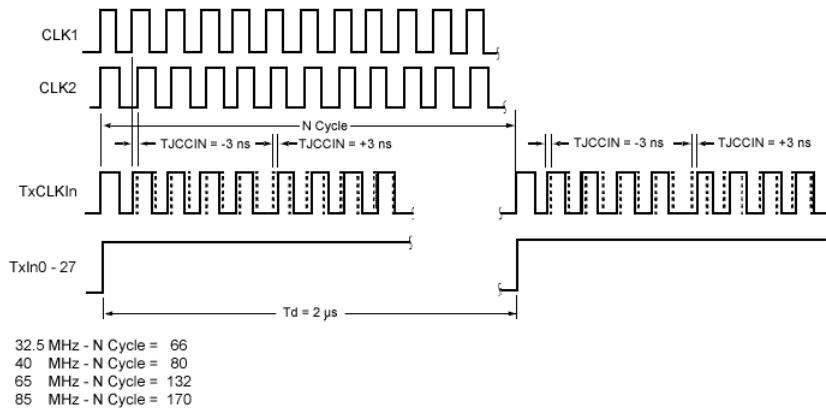
**Note:** This jitter pattern is used to test the jitter response (Clock Out) of the device over the power supply range with worst jitter ±3ns (cycle-to-cycle) clock input. The specific test methodology is as follows:

• Switching input data TxIn0 to TxIn20 at 0.5 MHz, and the input clock is shifted to left −3ns and to the right +3ns when data is HIGH.

• The ±3 ns cycle-to-cycle input jitter is the static phase error between the two clock sources. Jumping between two clock sources to simulate the worst case of clock edge jump (3 ns) from graphical controllers. Cycle-to-cycle jitter at TxCLK out pin should be measured cross $V_{CC}$ range with 100mV noise ($V_{CC}$ noise frequency <2 MHz).

**FIGURE 20. Timing Diagram of Transmitter Clock Input with Jitter**

# AC Loading and Waveforms (Continued)

| Divice Pin Name | Signal | Signal Pattern | Signal Frequency |
|---|---|---|---|
| TxCLKIn / RxCLKOut | Dot CLK | | $f$ |
| TxIn0 / RxOut0 | R0 | | $f / 16$ |
| TxIn1 / RxOut1 | R1 | | $f / 8$ |
| TxIn2 / RxOut2 | R2 | | $f / 4$ |
| TxIn3 / RxOut3 | R3 | | $f / 2$ |
| TxIn4 / RxOut4 | R4 | | Steady State, LOW |
| TxIn5 / RxOut5 | R5 | | Steady State, LOW |
| TxIn6 / RxOut6 | G0 | | $f / 16$ |
| TxIn7 / RxOut7 | G1 | | $f / 8$ |
| TxIn8 / RxOut8 | G2 | | $f / 4$ |
| TxIn9 / RxOut9 | G3 | | $f / 2$ |
| TxIn10 / RxOut10 | G4 | | Steady State, LOW |
| TxIn11 / RxOut11 | G5 | | Steady State, LOW |
| TxIn12 / RxOut12 | B0 | | $f / 16$ |
| TxIn13 / RxOut13 | B1 | | $f / 8$ |
| TxIn14 / RxOut14 | B2 | | $f / 4$ |
| TxIn15 / RxOut15 | B3 | | $f / 2$ |
| TxIn16 / RxOut16 | B4 | | Steady State, LOW |
| TxIn17 / RxOut17 | B5 | | Steady State, LOW |
| TxIn18 / RxOut18 | HSYNC | | Steady State, HIGH |
| TxIn19 / RxOut19 | VSYNC | | Steady State, HIGH |
| TxIn20 / RxOut20 | ENA | | Steady State, HIGH |

**Note:** The 16-grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

**FIGURE 21. "16 Grayscale" Test Pattern**
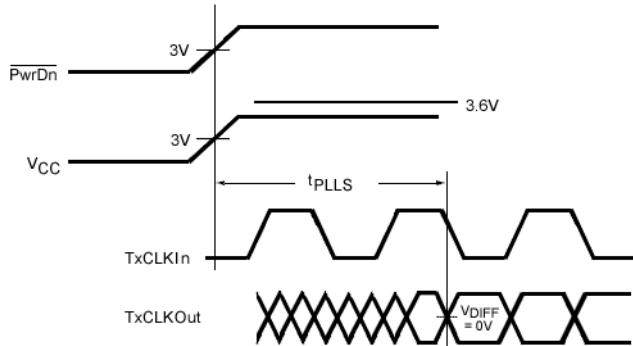


**FIGURE 22. Transmitter Phase Lock Loop Time**

## Physical Dimensions inches (millimeters) unless otherwise noted

14.0 ± 0.1
−A−
56
29
8.1
4.05
6.1 ± 0.1
−B−
1
28
⌓ 0.2 C B A
ALL LEAD TIPS

SYMM ℄
SYMM ℄
(9.2 TYP)
(5.6 TYP)
(1.8 TYP)
(0.3 TYP)
(0.5 TYP)

LAND PATTERN RECOMMENDATION

⌓ 0.1 C
ALL LEAD TIPS
−C−
0.5 TYP
0.17 − 0.27 TYP
(0.90)
1.1 MAX
0.10 ± 0.05 TYP
⊕ 0.13 Ⓜ A BⓈ CⓈ

SEE DETAIL A
0.09−0.20 TYP

GAGE PLANE
0.25
SEATING PLANE
0°−8°
0.60 +0.15 −0.10

DETAIL A
TYPICAL

MTD56 (REV B)

**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD56**

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